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Mitigation of Voltage Sags for Balance And Unbalanced Voltage in Low Voltage Distribution System

This paper proposes a mitigation of different types of voltage sags in low voltage distribution system using an effective series compensator or Dynamic Voltage Restorer (DVR) with new configuration of its topology. The main function of the DVR is to maintain the voltage at the sensitive load from balance and unbalance voltage sags. The developed system can compensate voltage sags in the grid and at the end can be used for the protection of sensitive loads in the network. DVR under various load conditions and different types of fault in both single phase and three phases were investigated. A prototype of the proposed scheme was built and tested in order to test its feasibility through extensive experimental studies.

Keywords: Dynamic Voltage Restorer (DVR), voltage sag, power injected, low voltage, custom device

1. Nomenclature

d, q	Two-axis synchronous frame quantities.
α, β	Two-axis stationary frame quantities.
v_d, v_q	d- and q-axis components of the synchronous frame variables.
d-q-o	Park's transformation technique
V_1,V_2 ,V_o	Positive, negative and zero sequence voltage.
PWM	Pulse Width Modulation.
THD_V	Total Harmonics Distortion for voltage
θ	Angle of the source voltage.
VSC	Voltage Source Converter
V_{sag}	Voltage Sagging
P_{CC}	Point of Common Coupling
V_{inj}	Voltage Injection
S_{inj}	Apparent power injection
S_{supply}	Apparent power supply
S_{load}	Apparent power load
V_{grid}	Grid Voltage
V_{load}	Load Voltage
LPF	Low Pass Filter
V_{dc}	Energy Storage DC
P_{LL}	Phase Lock Loop
I_{supply}	Supply Current
I_{inj}	Injection Current
I_{load}	Load Current
V_{sa},V_{sb},V_{sc}	Voltage Supply

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2. Introduction

Nowadays the developments in digital electronics and process control had increased the number of sensitive loads which is one of the important factors in the degradation of power quality. The degradation is in term of ac supply system in both utility and industrial power system. The grid voltage parameters such as frequency variation, voltage variation, voltage fluctuations and unbalance in the three phase voltages, flicker and harmonic distortion are among the characteristics of the power quality steady state.

Most of the obvious power quality problems in the distribution systems are voltage sags, transient, voltage swells, harmonics and interruptions. The voltage sags as defined by IEEE Standard 1159, IEEE Recommended Practice for Monitoring Electric Power Quality, is “a decrease in RMS voltage or current at the power frequency for durations from 0.5 cycles to 1 minute, reported as the remaining voltage”. Typical values are between 0.1 p.u. and 0.9 p.u., and typical fault clearing times range from three to thirty cycles depending on the fault current magnitude and the type of over current detection and interruption. Voltage sags can cause damaged product, lost of production, and problem of breakdown [1-3].

Normally different types of voltage sags are occur in the grid. The faults in the grid can be summarized as three phase faults, three phase with ground connection, two phase faults with ground connection, and single phase faults. The survey made by the EPRI stated that most of the voltage sags which has been recorded in the distribution system are non symmetrical. The summary of the survey can be concluded that single phase faults are the most frequent occur in the distribution system which is about 68% from all the events. 19% from two-phase faults and only 13% from three phase faults. So it is very clear that non symmetrical faults are very dominant faults in the distribution power system.

There are many types of mitigation technique has been used in order to improve power quality problems. One of the famous techniques is using a DVR. The DVR is a custom power electronics device that is connected in series with the distribution systems as shown in Figure 1. Among the main importance function of a DVR is can detect voltage sags very fast, flexible and efficient [4-6].

This paper proposes a new configuration of DVR for mitigating balance and unbalance voltages. The proposed configuration is integrated with the controller using d-q-o transformation technique. A DSP board based on TMS320F2812 was used and a 5KVA DVR prototype has been built to validate the proposed configuration. Voltages can be sensed on the grid or the load side. The proposed topology together with the controller can ride through various kinds of voltage faults. Furthermore, voltage harmonics can also be reduced.

2. The Principle of Dynamic Voltage Restorer

Dynamic Voltage Restorer (DVR) is one of the effective custom power devices that can be used to improve power quality from any disturbances in the distribution line. The DVR can acts as a protection, and recovery or restore the quality of voltage to the sensitive load. A set of three-phase voltages with an appropriate magnitude and duration can be injected through injection transformer and must be in phase with the grid voltage. [7-9]:

Figure 1 shows the basic block diagram of a DVR for single-phase representation. The main components of DVR are [10]

- Voltage Source Converter (VSC)
- DC energy storage
- Control system

A relatively small capacitor is present on dc side of the PWM solid state inverter and the voltage over this capacitor is kept constant, by exchanging energy with the energy storage reservoir. The required output voltage is obtained by using pulse-width modulation switching pattern. As the controller will have to supply active as well as reactive power, some kind of energy storage is needed. In the DVRs that are commercially available now large capacitors are used as a source of energy [8]. Other potential sources are being considered are [7]: battery banks, superconducting coils, and flywheels.

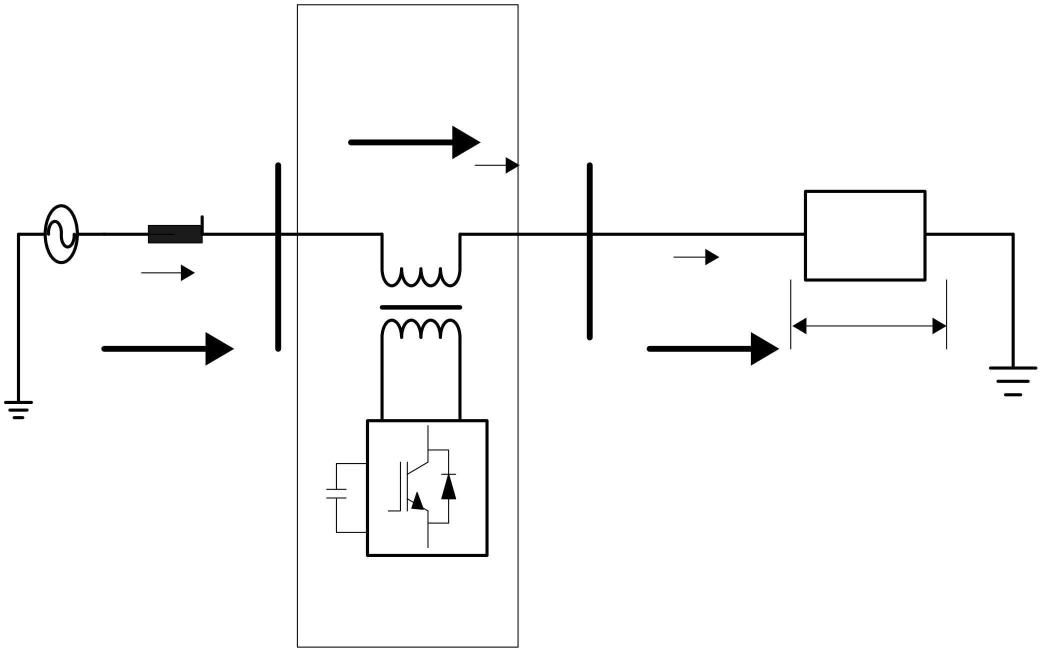

Figure 1: Typical DVR circuit topology (single-phase representation).

3. Determination Of Fault Concept in the Distribution System.

The magnitude of the voltage sag is defined as the minimum rms value obtained during the event and its duration is the time interval between the instant when rms voltage crosses the voltage sag threshold (usually 90% of normal voltage) and the instant when it returns to normal level. The rms value of voltage sag can be described as shown in Figure 2. From the Figure, since the voltage drop to threshold voltage 0.9 p.u at time T_1 the voltage sags occur, this situation will continous until the voltage recover at its nominal value (at 1.0 p.u)

. V_{sag} is the magnitude of the voltage sags and the voltage sags occur at the duration of T_2 to T_1 [11].

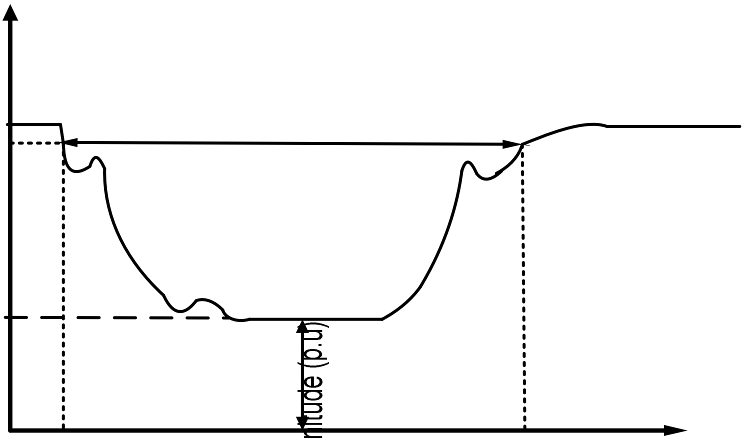

Figure 2: Voltage sag

Normally voltage divider model is used to describe the origin of voltage sags and the shifting of phase angle when the fault occur in the power system. Figure 3, shows where the magnitude and phase of the faulted voltage sag during the sag at the point of common coupling (PCC) are determined by the fault and supply impedances using the equation:

$$V_{sag}=\frac{Z_F}{Z_F + Z_s} \qquad (1)$$

Where ;

$\overline{Z_F}$ is the impedance between the fault and the Point-of-Common Coupling (PCC) of the fault and the load.

$\overline{Z_S}$ is the source impedance at the pcc, the pre-event voltage is considered equal to 1 pu, and all load is assumed to be of the constant-impedance type[3,4,5,6].

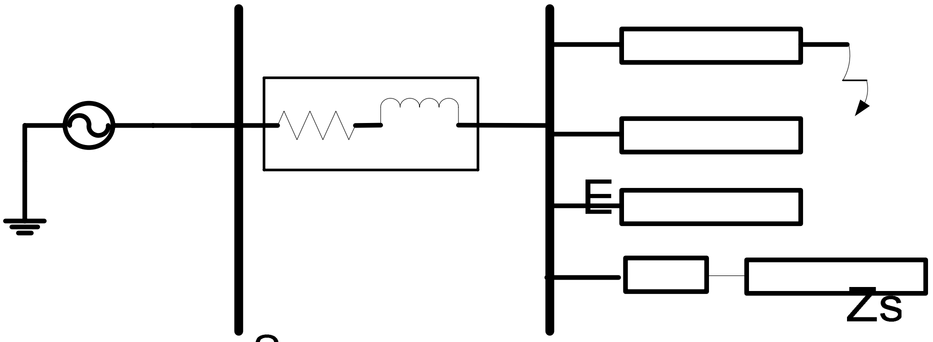

Figure 3: A simple radial circuit of Voltage Sag

$$V_{sag} = \frac{\mu}{\mu + e^{j\varphi}} \tag{2}$$

Where $\mu = \left| \frac{\overline{Z_F}}{\overline{Z_S}} \right|$ and $\varphi = \arg\left\{ \frac{\overline{Z_F}}{\overline{Z_S}} \right\}$

The voltage-divider model gives the so-called "characteristic voltage" for the voltages in the three phases. The model can be applied directly to study the effect of voltage sags on three-phase equipment [4, 5, 6,7].

A. Balance Voltage Sags

Balance voltage sags are due to three phases and three phase to ground faults. All three phase voltage magnitudes are equal and lower than the sag threshold with no phase shift.

B. Three Phase Unbalance Voltage Sag

Unbalance describes a situation in which the voltages of a three-phase voltage source are not identical in magnitude, or the phase differences between them are not 120 electrical degrees, or both. Symmetrical components consists of Positive-sequence voltage V_1 , negative-sequence voltage V_2, and zero-sequence voltage Vo are calculated from the complex phase voltages V_a ,V_b and V_c

$$\begin{bmatrix} V_o \\ V_1 \\ V_2 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3}$$

$$a = -\frac{1}{2} + \frac{1}{2} j\sqrt{3}$$

Due to different kinds of faults in power systems, different types of voltage sag can be produced most faults in power systems are single phase or three phases. Different types of faults lead to different types of voltage sags. Normally, voltage sag is characterized by a magnitude and duration. In some cases phase-angle jumps are also included. Voltage sag are divided in to seven groups as type A, B, C, D, E, F and G as explained in [8-11]. Type A is symmetrical and the other types are known as unsymmetrical voltage sag. Phasor diagram of three phase voltages with balance voltage sags of type A is illustarated in Figure 4. The characterizing three phase unbalanced voltage sags are discussed in [10]. As mentioned earlier most of unbalanced sags derived from line-to-line and single-line to ground faults, Figure 4(b) and (c) show the phasor diagram of type B and C respectively.

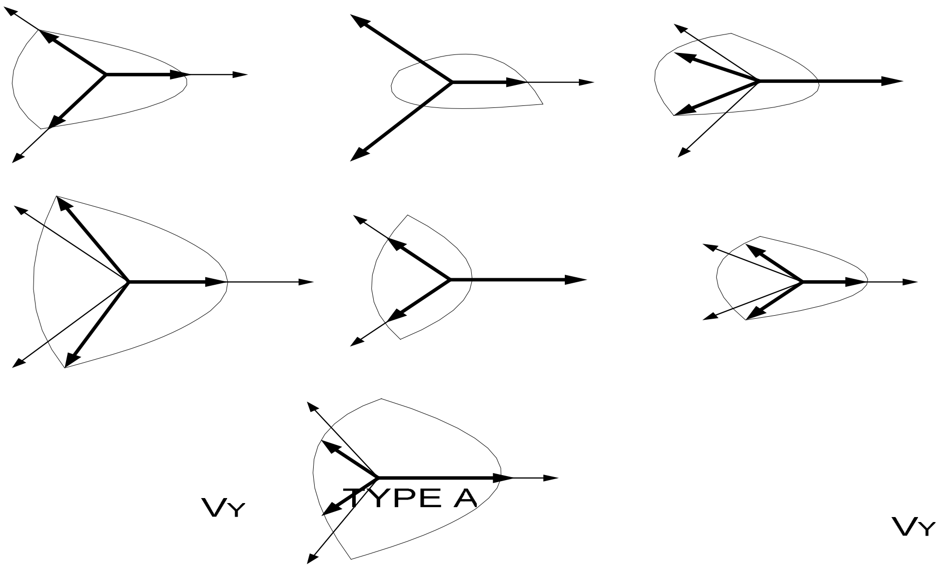

Figure 4: Phasor diagram of balance and unbalanced voltage sags.

4. Control System Of A DVR

There are so many types of control techniques available of the DVR. A DVR can be controlled by using either feed forward or feedback modes. The grid voltage, Vgrid and load voltage, Vload can be sensed through feed forward control technique; normally this type of control is easier to apply rather than using feedback mode technique. However this technique may arise phase jump and transformer saturation. A feedback control technique is applied when both Vgrid and Vload are sensing together in order to minimize the error, normally this technique is more difficult to control as compared to the feed forward method.

The controller in a DVR must capable to detect any disturbances events in the distribution system. The converter, which is connected in series with the network compensates the missing voltage when unbalance voltage occurs[11]. Once the disturbances have been detected by the controller, DC-AC converter will generates trigger pulses to the sinusoidal PWM. The trigger pulses produced by the DC-AC converter may be used to correct any anomalies in the series voltage injection. When there were no disturbances events appears within the distribution system the converter will stop immediately of the trigger pulses

5. Proposed New Scheme Configuration Of DVR

Figure 5 shows that the proposed configuration model of the DVR. The DVR consists of a 3-leg inverter, three LC output filters, and three phase injection transformers. The 3-leg inverter has 6 IGBT switches and dc power supply in the dc link. In this proposed designed of DVR, the filtering scheme is installed for both on the low and high voltages. The filter inductor, capacitor and resistor are installed on low voltage side between the series converter and the transformer and the high voltage side.

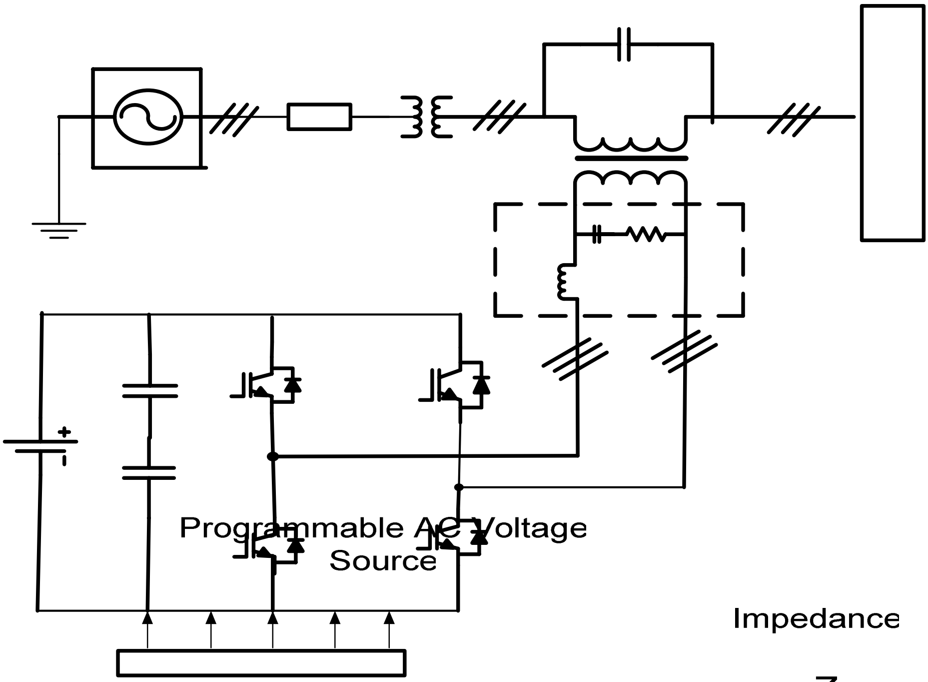

Figure 5 :New Configuration Of the Proposed Scheme for DVR

When it is place in low voltage side, high order harmonics from the three phase voltage source PWM inverter is by pass by the filtering scheme and its impact on the injection current rating can be ignored [15]. The type of this filtering configuration can also eliminate switching ripples produced by the converter. As for the filtering scheme is placed in the high voltage side in this case, high order harmonic currents will penetrates through the injection and it will carry the harmonic voltages. When compensate the voltage sag/swell at the critical load, DVR produce a harmonics distortion fed from series transformer as an injection voltage to the critical load. Using the FFT analysis to analyze the total harmonic distortion (THD) for the voltage signal, for the proposed of the filtering scheme configuration result that the THD is about (1.44%).

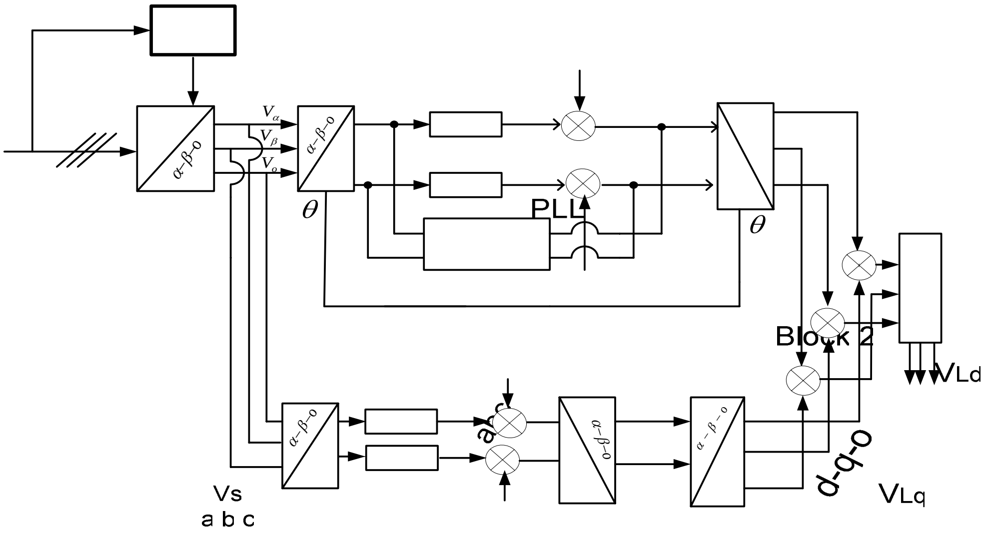

Figure 6: Block Diagram Control Scheme of DVR for Unbalance Voltage

Figure 6 show the main components of the control system using d-q-o Park's transformation technique. The control system consists of 6 blocks and each, block has its function and can be described as following:

- Block 1 is used to convert the three phase load voltages (V_{sa}, V_{sb}, V_{sc}) into the α-β-o coordinates as in equation (4)

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_o \end{bmatrix} = T \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \qquad (4)$$

$$\text{Where } T = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix}$$

- Block 2 and block 3 is the α-β-o to d-q-o transformation blocks which are used to convert the three phase load voltages reference components $V_{\alpha\text{-ref,}}$ $V_{\alpha\text{-ref}}$ and Vo $_{ref}$ to $V_{d\,ref}$, $V_{q\,ref}$ and $V_{o\,ref}$ by using equation (5), (6),(7) and (8)

$$V_d = \frac{2}{3}\left[V_a \cos\theta \quad V_b \cos\left(\theta - \frac{2\pi}{3}\right) \quad V_c \cos\left(\theta + \frac{2\pi}{3}\right) \right] \qquad (5)$$

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$$V_q = \frac{2}{3}\left[-V_a \sin\theta \; - V_b \sin\left(\theta - \frac{2\pi}{3}\right) \; - V_c \sin\left(\theta + \frac{2\pi}{3}\right)\right] \tag{6}$$

$$V_o = \frac{1}{3}\left[V_a \; + \; V_b \; + \; V_c\right] \tag{7}$$

$$\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} \tag{9}$$

- Block 4 is used to convert the d-q-o to α-β-o and the transformation of the α-β-o to a-b-c has been done by block 5. The angle θ of the source voltage can be obtained using three-phase PLL. The information extracted from the PLL is used for detection and reference voltage generation.

- Block 6 is the detection scheme for the voltage unbalance compensator. From Figure 5, it shows that the synchronous frame variables - V_d and V_q - are used as inputs for low pass filters to generate voltage references in the synchronous frame.

- Block 7 receives the components of the load voltage vectors Vd ref and Vq ref and transforms them to three-phase coordinates using equation (9) where the generation voltages are used as the voltage reference. The DC link error in Figure 5 is used to get optimized controller output signal because the energy on the DC link will be changed during the unbalance voltage.

- Block 8 is the PWM block. This block provides the firing for the Inverter switches (PWM1 to PWM6). The injection voltage is generated according to the difference between the reference load voltage and the injection voltage is generated according to the difference between the reference load voltage and the supply voltage and is then applied to the voltage source converter (VSC).

5. Experimental Results

In order to verify the effectiveness of the proposed system, a 6KVA prototype of DVR has been built based on the system depicted in Figure 5. Experimental system parameters have been introduced in Table 1.The experimental results obtained based on type A, B and E of voltage sags. The grid terminal voltages V_{sa}, V_{sb} and V_{sc} are measured by the voltage sensor, then the voltages signal are entered into the DSP TMS320F2812. The output currents of the inverter is measured by using current sensor and then sensed by the DSP board to boost up the voltage response of the DVR. All these signals are processed by the DSP board at sampling period of 100us. The prototype is rated to protect a 5KVA load a 40% voltage sags.

Balanced Voltage Sags

The three phase voltages of balance sags are shown in Figure7 (a) .In the no distortion case and before the faults occur in the distribution line, the system is in steady state and the voltage magnitude of the grid is stable. In Figure 4(a) , the faults start at t = 60ms, the grid voltage decrease to 40% of its nominal value, the faults duration is 100ms, the faults are supposed to be cleared at 160ms, and the grid voltage recovers to its initial value. The grid, the injection and the load voltages are illustrated in Figures 7(a), 7(b) and 7(c). In case of there is no faults occur, the load voltage is equal to the grid voltage and the output of the DVR is assumed to be zero. As the voltage sags occur, the grid voltage will drop and the DVR injection voltage will inject the missing voltage in order to keep the load voltage maintain at the same value before the faults.

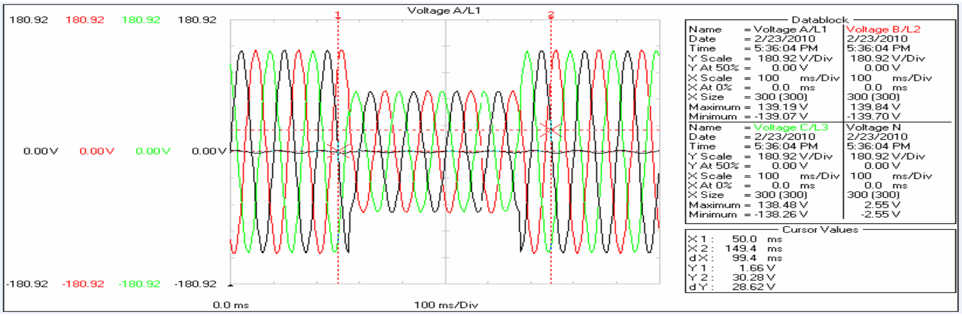
Table 1: Experimental System Parameters

Main Supply Voltage per phase	230 V
Line Impedance	Ls =0.7 mH Rs = 0.3 Ω
Series transformer turns ratio	1:1
DC Bus Voltage	120V
Filter Inductance	220uH
Filter capacitance	40uF
Load resistance	40 Ω
Load inductance	60mH
Line Frequency	50Hz
Switching Frequency	10kHz

Unbalance Voltage Sags

Most of the faults in distribution system are due to unbalance voltage sag. Single phase and line to line faults are identified as the most frequent types of faults and 95% of the faults in the distribution come from unbalance faults.

Unbalance voltage sags can occur when one of the phases in supply voltage decreases from its nominal value, this can be seen in Figure 8(a). From the figure showed that one phase voltage magnitude is lower than two other phase voltages. Figure 8(b) shows the DVR compensates for the type B of voltage sags. At the end of the faults in Figure 8(a), the load terminal voltages are in phase with the source voltage. Load terminal voltages are restored through the compensation by DVR as shown in Figure 8(c). Next, the performance of DVR for two phases to ground fault is also investigated. Figure 9 (a) shows the series of voltages components for unbalanced conditions in two phases to ground fault. Similar to the case of voltage sag for this type, the DVR reacts very fast to inject the appropriate voltage in order to correct the supply voltage as shown in Figure 9(b). Figure 9(c) shows load voltage after compensation. According to this figure load voltages in unbalanced voltage sags are successfully compensated. This phenomena show that the proposed control system is capable to mitigate voltage unbalance of the supply voltage.



Datablock

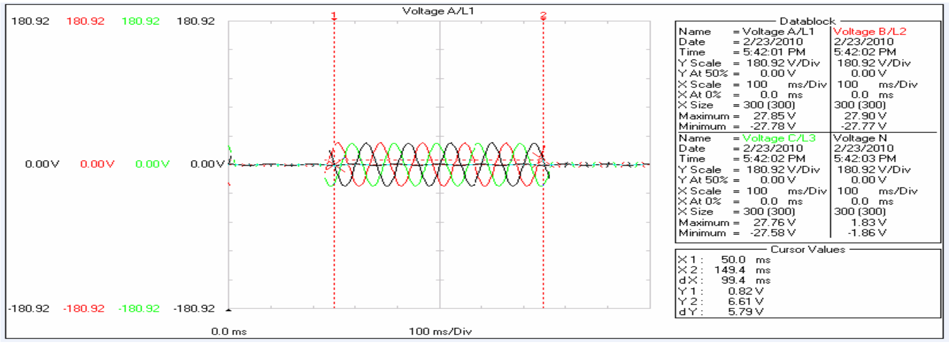
Name	= Voltage A/L1	Voltage B/L2
Date	= 2/23/2010	2/23/2010
Time	= 5:36:04 PM	5:36:04 PM
Y Scale	= 180.92 V/Div	180.92 V/Div
Y At 50%	= 0.00 V	0.00 V
X Scale	= 100 ms/Div	100 ms/Div
X At 0%	= 0.0 ms	0.0 ms
X Size	= 300 (300)	300 (300)
Maximum	= 139.19 V	139.84 V
Minimum	= -139.07 V	-139.70 V
Name	= Voltage C/L3	Voltage N
Date	= 2/23/2010	2/23/2010
Time	= 5:36:04 PM	5:36:04 PM
Y Scale	= 180.92 V/Div	180.92 V/Div
Y At 50%	= 0.00 V	0.00 V
X Scale	= 100 ms/Div	100 ms/Div
X At 0%	= 0.0 ms	0.0 ms
X Size	= 300 (300)	300 (300)
Maximum	= 138.48 V	2.55 V
Minimum	= -138.26 V	-2.55 V

Cursor Values

X 1 :	50.0 ms
X 2 :	149.4 ms
d X :	99.4 ms
Y 1 :	1.66 V
Y 2 :	30.28 V
d Y :	28.62 V

(a)

Figure 7(a): Three phase fault Supply Voltages



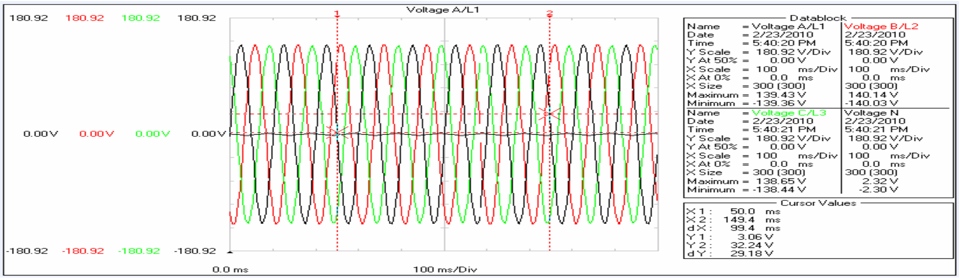
Datablock

Name	= Voltage A/L1	Voltage B/L2
Date	= 2/23/2010	2/23/2010
Time	= 5:42:01 PM	5:42:02 PM
Y Scale	= 180.92 V/Div	180.92 V/Div
Y At 50%	= 0.00 V	0.00 V
X Scale	= 100 ms/Div	100 ms/Div
X At 0%	= 0.0 ms	0.0 ms
X Size	= 300 (300)	300 (300)
Maximum	= 27.85 V	27.90 V
Minimum	= -27.78 V	-27.77 V
Name	= Voltage C/L3	Voltage N
Date	= 2/23/2010	2/23/2010
Time	= 5:42:02 PM	5:42:03 PM
Y Scale	= 180.92 V/Div	180.92 V/Div
Y At 50%	= 0.00 V	0.00 V
X Scale	= 100 ms/Div	100 ms/Div
X At 0%	= 0.0 ms	0.0 ms
X Size	= 300 (300)	300 (300)
Maximum	= 27.76 V	1.83 V
Minimum	= -27.58 V	-1.86 V

Cursor Values

X 1 :	50.0 ms
X 2 :	149.4 ms
d X :	99.4 ms
Y 1 :	0.82 V
Y 2 :	6.61 V
d Y :	5.79 V

Figure 7(b): Injection Voltage by DVR



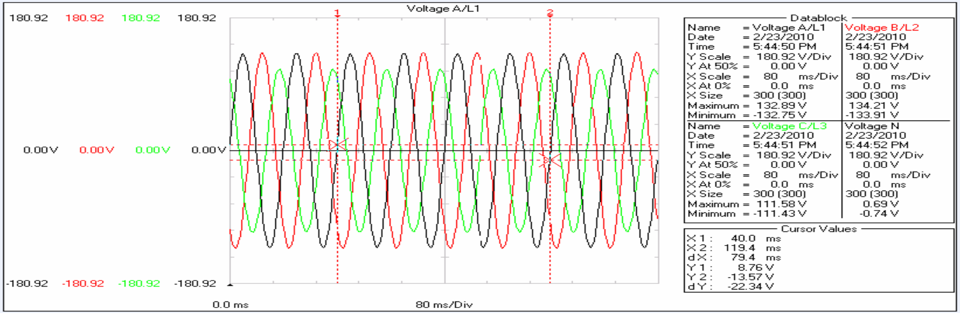
Datablock

Name	= Voltage A/L1	Voltage B/L2
Date	= 2/23/2010	2/23/2010
Time	= 5:40:20 PM	5:40:20 PM
Y Scale	= 180.92 V/Div	180.92 V/Div
Y At 50%	= 0.00 V	0.00 V
X Scale	= 100 ms/Div	100 ms/Div
X At 0%	= 0.0 ms	0.0 ms
X Size	= 300 (300)	300 (300)
Maximum	= 139.43 V	140.14 V
Minimum	= -139.36 V	-140.03 V
Name	= Voltage C/L3	Voltage N
Date	= 2/23/2010	2/23/2010
Time	= 5:40:21 PM	5:40:21 PM
Y Scale	= 180.92 V/Div	180.92 V/Div
Y At 50%	= 0.00 V	0.00 V
X Scale	= 100 ms/Div	100 ms/Div
X At 0%	= 0.0 ms	0.0 ms
X Size	= 300 (300)	300 (300)
Maximum	= 138.65 V	2.32 V
Minimum	= -138.44 V	-2.30 V

Cursor Values

X 1 :	50.0 ms
X 2 :	149.4 ms
d X :	99.4 ms
Y 1 :	3.06 V
Y 2 :	32.24 V
d Y :	29.18 V

Figure 7(c): Load Voltages Restoration



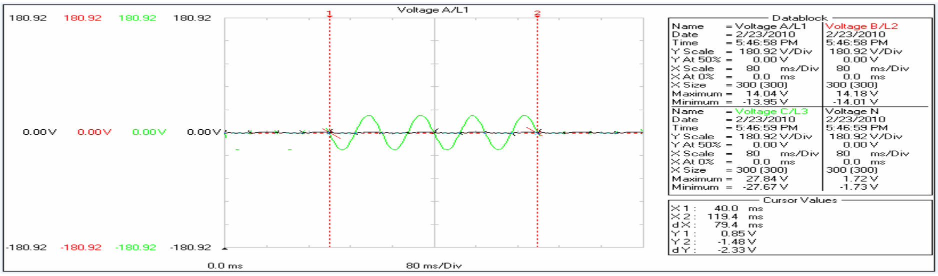
Datablock

Name	= Voltage A/L1	Voltage B/L2
Date	= 2/23/2010	2/23/2010
Time	= 5:44:50 PM	5:44:51 PM
Y Scale	= 180.92 V/Div	180.92 V/Div
Y At 50%	= 0.00 V	0.00 V
X Scale	= 80 ms/Div	80 ms/Div
X At 0%	= 0.0 ms	0.0 ms
X Size	= 300 (300)	300 (300)
Maximum	= 132.89 V	134.21 V
Minimum	= -132.75 V	-133.91 V
Name	= Voltage C/L3	Voltage N
Date	= 2/23/2010	2/23/2010
Time	= 5:44:51 PM	5:44:52 PM
Y Scale	= 180.92 V/Div	180.92 V/Div
Y At 50%	= 0.00 V	0.00 V
X Scale	= 80 ms/Div	80 ms/Div
X At 0%	= 0.0 ms	0.0 ms
X Size	= 300 (300)	300 (300)
Maximum	= 111.58 V	0.69 V
Minimum	= -111.43 V	-0.74 V

Cursor Values

X 1 :	40.0 ms
X 2 :	119.4 ms
d X :	79.4 ms
Y 1 :	8.76 V
Y 2 :	-13.57 V
d Y :	-22.34 V

Figure 8(a): Single phase fault Supply Voltages



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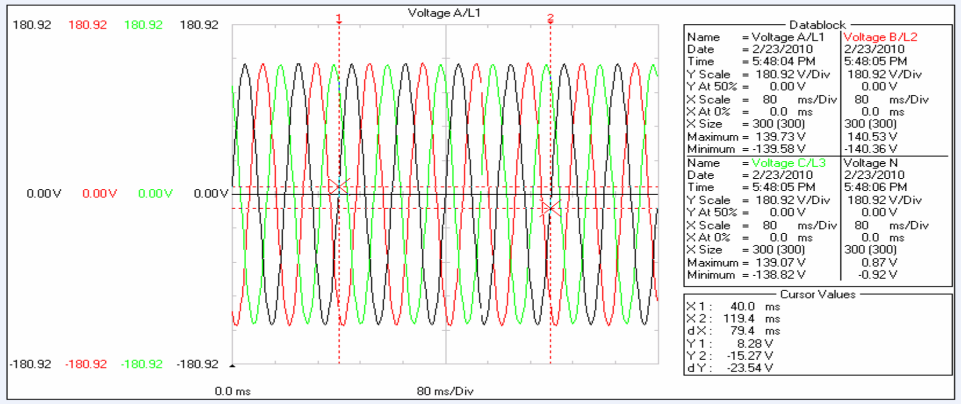
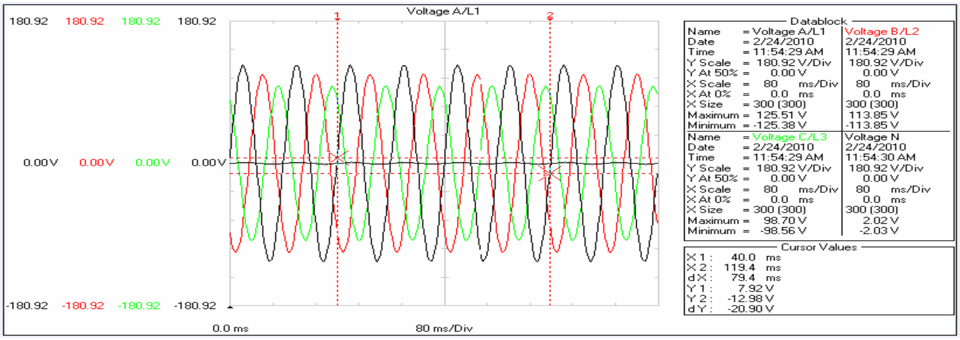
Date      = 2/23/2010      2/23/2010
Time      = 5:46:58 PM     5:46:58 PM
Y Scale   =  180.92 V/Div   180.92 V/Div
Y At 50% =      0.00 V         0.00 V
X Scale   =    80     ms/Div   80     ms/Div
X At 0%   =      0.0   ms        0.0   ms
X Size    = 300 (300)      300 (300)
Maximum =    14.04 V        14.18 V
Minimum  =   -13.95 V       -14.01 V
Name      = Voltage C/L3   Voltage N
Date      = 2/23/2010      2/23/2010
Time      = 5:46:59 PM     5:46:59 PM
Y Scale   =  180.92 V/Div   180.92 V/Div
Y At 50% =      0.00 V         0.00 V
X Scale   =    80     ms/Div   80     ms/Div
X At 0%   =      0.0   ms        0.0   ms
X Size    = 300 (300)      300 (300)
Maximum =    27.84 V         1.72 V
Minimum  =   -27.67 V        -1.73 V
Cursor Values
X 1 :    40.0   ms
X 2 :   119.4   ms
dX :     79.4   ms
Y 1 :     0.85 V
Y 2 :    -1.48 V
dY :     -2.33 V
```

Figure 8(b): Injection Voltages by DVR



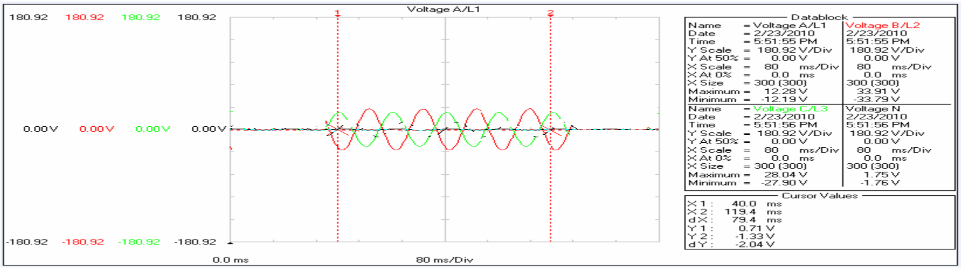
```
Datablock
Name      = Voltage A/L1   Voltage B/L2
Date      = 2/23/2010      2/23/2010
Time      = 5:48:04 PM     5:48:05 PM
Y Scale   =  180.92 V/Div   180.92 V/Div
Y At 50% =      0.00 V         0.00 V
X Scale   =    80     ms/Div   80     ms/Div
X At 0%   =      0.0   ms        0.0   ms
X Size    = 300 (300)      300 (300)
Maximum =  139.73 V        140.53 V
Minimum  = -139.58 V       -140.36 V
Name      = Voltage C/L3   Voltage N
Date      = 2/23/2010      2/23/2010
Time      = 5:48:05 PM     5:48:06 PM
Y Scale   =  180.92 V/Div   180.92 V/Div
Y At 50% =      0.00 V         0.00 V
X Scale   =    80     ms/Div   80     ms/Div
X At 0%   =      0.0   ms        0.0   ms
X Size    = 300 (300)      300 (300)
Maximum =  139.07 V          0.87 V
Minimum  = -138.82 V         -0.92 V
Cursor Values
X 1 :    40.0   ms
X 2 :   119.4   ms
dX :     79.4   ms
Y 1 :     8.28 V
Y 2 :   -15.27 V
dY :    -23.54 V
```

Figure 8(c): Load Voltages Restoration



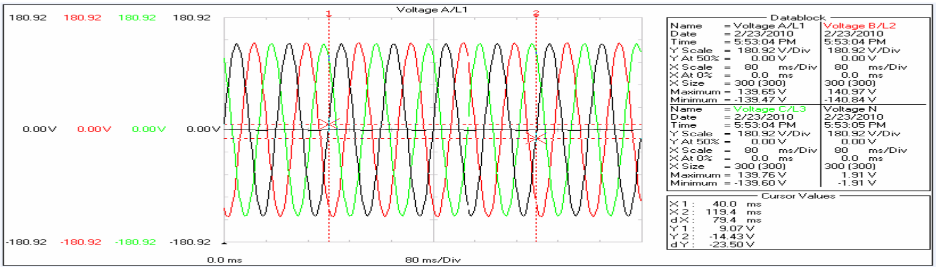
```
Datablock
Name      = Voltage A/L1   Voltage B/L2
Date      = 2/24/2010      2/24/2010
Time      = 11:54:29 AM    11:54:29 AM
Y Scale   =  180.92 V/Div   180.92 V/Div
Y At 50% =      0.00 V         0.00 V
X Scale   =    80     ms/Div   80     ms/Div
X At 0%   =      0.0   ms        0.0   ms
X Size    = 300 (300)      300 (300)
Maximum =  125.51 V        113.85 V
Minimum  = -125.38 V       -113.85 V
Name      = Voltage C/L3   Voltage N
Date      = 2/24/2010      2/24/2010
Time      = 11:54:29 AM    11:54:30 AM
Y Scale   =  180.92 V/Div   180.92 V/Div
Y At 50% =      0.00 V         0.00 V
X Scale   =    80     ms/Div   80     ms/Div
X At 0%   =      0.0   ms        0.0   ms
X Size    = 300 (300)      300 (300)
Maximum =    98.70 V         2.02 V
Minimum  =   -98.56 V        -2.03 V
Cursor Values
X 1 :    40.0   ms
X 2 :   119.4   ms
dX :     79.4   ms
Y 1 :     7.92 V
Y 2 :   -12.98 V
dY :    -20.90 V
```

Figure 9(a): Two phases fault Supply Voltages



```
Datablock
Name      = Voltage A/L1   Voltage B/L2
Date      = 2/23/2010      2/23/2010
Time      = 5:51:55 PM     5:51:55 PM
Y Scale   =  180.92 V/Div   180.92 V/Div
Y At 50% =      0.00 V         0.00 V
X Scale   =    80     ms/Div   80     ms/Div
X At 0%   =      0.0   ms        0.0   ms
X Size    = 300 (300)      300 (300)
Maximum =    12.28 V        33.91 V
Minimum  =   -12.19 V       -33.79 V
Name      = Voltage C/L3   Voltage N
Date      = 2/23/2010      2/23/2010
Time      = 5:51:56 PM     5:51:56 PM
Y Scale   =  180.92 V/Div   180.92 V/Div
Y At 50% =      0.00 V         0.00 V
X Scale   =    80     ms/Div   80     ms/Div
X At 0%   =      0.0   ms        0.0   ms
X Size    = 300 (300)      300 (300)
Maximum =    28.04 V         1.75 V
Minimum  =   -27.90 V        -1.76 V
Cursor Values
X 1 :    40.0   ms
X 2 :   119.4   ms
dX :     79.4   ms
Y 1 :     0.71 V
Y 2 :    -1.33 V
dY :     -2.04 V
```

Figure 9(b): Injection Voltages by DVR



```
Datablock
Name      = Voltage A/L1    Voltage B/L2
Date      = 2/23/2010       2/23/2010
Time      = 5:53:04 PM      5:53:04 PM
Y Scale   =  180.92 V/Div    180.92 V/Div
Y At 50% =      0.00 V          0.00 V
X Scale   =    80     ms/Div   80     ms/Div
X At 0%  =      0.0   ms        0.0   ms
X Size    = 300 (300)       300 (300)
Maximum =  139.65 V         140.97 V
Minimum  = -139.47 V        -140.84 V
Name      = Voltage C/L3    Voltage N
Date      = 2/23/2010       2/23/2010
Time      = 5:53:04 PM      5:53:05 PM
Y Scale   =  180.92 V/Div    180.92 V/Div
Y At 50% =      0.00 V          0.00 V
X Scale   =    80     ms/Div   80     ms/Div
X At 0%  =      0.0   ms        0.0   ms
X Size    = 300 (300)       300 (300)
Maximum =  139.76 V           1.91 V
Minimum  = -139.60 V          -1.91 V
Cursor Values
X 1 :    40.0   ms
X 2 :   119.4   ms
d X :    79.4   ms
Y 1 :     9.07 V
Y 2 :   -14.43 V
d Y :   -23.50 V
```

Figure 9(c): Load Voltages restoration

6. Conclusion

This paper analyzes the compensation technique of a DVR for mitigating for several types of voltage sags such as type A, B and E in low voltage distribution system. The new configuration of the DVR and application of its proposed controller promising quick response and high reliability to protect unbalance voltage sags in the distribution system. The conclusion is that the DVR is an effective apparatus to protect sensitive loads from short duration voltage sags. The DVR can be inserted both at the low voltage and medium voltage level. The proposed theory has been verified by an experimental DVR system that shows very good performance as predicted by the analysis.

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