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Comparison of different control strategy based on pole placement for cascade multilevel inverter based dynamic voltage restorer

This paper proposes a robust linear Controller for cascade inverter-type dynamic voltage restorer (DVR) to compensate voltage sags in utility voltages in power distribution network. The proposed control strategy is implemented for DVR using multilevel inverter topology with isolated DC energy storages. The phase shifted PWM technique is described to generate firing pulses to cascaded inverter. PI and RST controllers are compared in terms of disturbance rejection, DC energy storage requirement and harmonics suppression at the load end. The proposed concept is simulated using MATLAB Simulink environment. The simulation results are presented to verify the performance of the proposed multilevel dynamic voltage restorer.

Keywords: DVR, Multilevel, Disturbance, Cascade Inverter, Mitigation.

1. INTRODUCTION

Voltage sags are one of the power quality assets which dragged the attention of many researchers especially in developing countries like India as the sensitivity of loads are increasing due extensive usage of power electronics devices. Faults at distribution level, sudden increase of load, motor starting are some of the causes of the voltage sags. Such sudden variations of voltage are undesirable for sensitive loads.

A dynamic voltage restorer is one such device having capability of protecting sensitive loads from all supply side disturbances. Fig. 1 shows the series connection of a dynamic voltage restorer (DVR) [1], [2] between the utility source and loads through a coupling transformer. During normal operating conditions, DVR is switched off or controlled to compensate for any injected harmonic voltages in the utility. During sag period, the DVR operates in boost mode and injects voltage of sufficient magnitude to maintain constant voltage throughout the sag period. However, phase of the load can be either be shifted or remain unchanged depending on the compensation technique adopted.

Many topologies are proposed for DVR [3] in past, most common being two-three-level three phase converter with dc capacitor connected alternatively to all phases. H-bridge cascade inverter [4] is the one such popularly used converter topology. Multilevel topology offers the following advantages.

1) Simple structure and requires fewer components.
2) Packaging layout is much easier because of simplicity of structure and lower component count.
3) Each bridge can be controlled independently permitting efficient single-phase voltage compensation.
4) Ability to reach high voltage and reduce harmonics by their own structures without any transformers
5) Generates multi step staircase voltage waveform similar to pure sinusoidal output voltage by increasing the number of levels.

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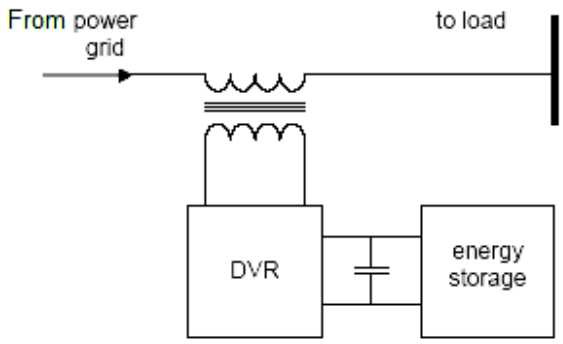

Fig 1: Configuration of DVR

Because of performance of the overall control system largely depends on the quality of the applied control strategy, a high performance-controller with fast transient response and good steady state characteristics is required. Various control strategies have been proposed for voltage source PWM converters [5]-[12]. Some of them are ramp comparison regulator, synchronous PI regulator; state feedback regulator, hysteresis regulator, neural network and fuzzy logic regulator etc. Nonlinear controller is more suitable than the linear since the converter is truly a nonlinear system.

Non-linear systems are linearized either by using some small classical techniques or by using small perturbations. To have zero steady state error and better transient response, PI controller is widely used. The PI controller though capable of making steady state error zero, does not have disturbance rejection capability and moreover tuning the gain values is difficult sometimes. Since PI controller is placed in feed-forward path, it is said have one degree of freedom. Robust controller is the best solution for the PI controller which employs two degree of freedom. There are many robust controllers like IMC, $H\infty$, H_2 and LQG etc. This paper presents RST controller, where R, S & T are three polynomials placed in feed-forward and feedback path. Since two controllers are placed in closed loop, RST controller attains two degree of freedom. RST controller has been applied on the indirect-rotor-field-oriented-control (IRFOC) of a double star induction machine (DSIM) [14]. A comparison between conventional RST polynomial control by poles placement and RST flatness-based control is proposed in [15].Basically RST are three individual polynomials chosen so as to reduce the effect of disturbance in reference signal tracking. Diophantine equation is very well used to obtain these polynomials. Moreover RST controller is based on shaping of its sensitivity functions. In this context, three sensitivity functions are defined namely output-to-output, measure to output and control-to-output sensibility functions. Constraints or disturbance rejections are naturally expressed in terms of frequency sensitivity shapes. For a given controller, the sensitivity functions allow to evaluate the controller behavior in relation to the desired attenuation constraints.

Power quality improvement through series active power filter is presented in this paper. This paper focuses on the modeling of PI controller with pole placement technique considering reference and disturbance signals as step signals. Later RST controller is modeled and tested with same signals. These two controllers are applied in DVR application. This design of PI controller with pole placement technique and RST controller for DVR application is described in this paper. The PI & RST controllers are compared briefly in terms of disturbance rejection and dc voltage energy storage requirements.

The paper structure as follows: Section II presents basic concepts of the DVR; modulation strategy of multilevel inverter is described in section III. Section IV depicts the design of PI controller. Section V & VI describes design of RST controller briefly and proposed test system. Section VII depicts the simulation results. Finally conclusions are presented in section VIII.

2. DVR OPERATION

The series voltage controller is connected in series with the protected load as shown in Fig.1. Usually the connection is made via a transformer, but configurations with direct connection via power electronics also exist. The resulting voltage at the load bus bar equals the sum of the grid voltage and the injected voltage from the DVR. The converter generates the reactive power needed while the active power is taken from the energy storage.

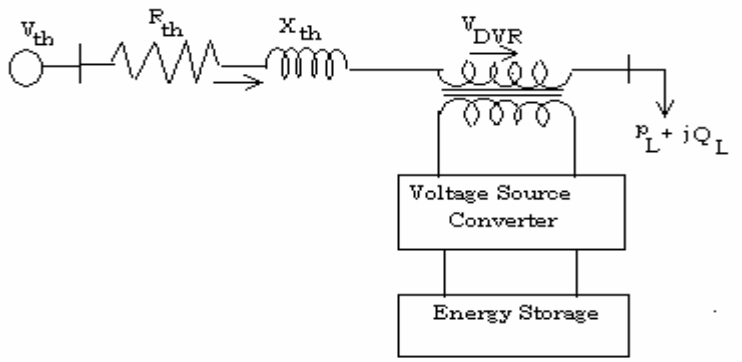

Fig 2: Schematic diagram of DVR

The energy storage can be different depending on the needs of compensating. The DVR often has limitations on the depth and duration of the voltage dip that it can compensate. The fig 2 represents the Thevenin equivalent circuit of the system. The system impedance Z_{th} depends on the fault level of the load bus. When the system voltage (V_{th}) drops, the DVR injects a series voltage V_{DVR} through the injection transformer so that the desired load voltage magnitude V_L can be maintained. The series injected voltage of the DVR can be written as,

$$V_{DVR} = V_L + Z_{th}I_L - V_{th} \quad (1)$$

Where

V_L is the desired load voltage magnitude
Z_{Th} is the load impedance
I_L is the load current
V_{th} is the system voltage during fault condition
The load current I_L is given by,

$$I_L = \frac{(P_L - J*Q_L)^*}{V_L} \quad \ldots\ldots \quad (2)$$

When V_L is considered as a reference, eqn. (1) can be rewritten as,

$$V_{DVR}\angle\alpha = V_L\angle 0 + Z_{th}I_L\angle(\beta - \theta) - V_{th}\angle\delta \quad \ldots\ldots \quad (3)$$

Here α, β and δ are the angle of V_{DVR}, Z_{th} and V_{th}, respectively, and θ is the load power factor angle,

The complex power injection of the DVR can be written as,

$$S_{DVR} = V_{DVR}I_L^* \quad \ldots\ldots\ldots\ldots \quad (4)$$

It may be mentioned here that when the injected voltage V_{DVR} is kept in quadrature with I_L, no active power injection by the DVR is required to correct the voltage. It requires the injection of only reactive power and the DVR itself is capable of generating the reactive power. Note that DVR can be kept in quadrature with I_L only up to a certain value of voltage sag and beyond which the quadrature relationship cannot be maintained to correct the voltage sag. For such a case, injection of active power into the system is essential. The injected active power must be provided by the energy storage system of the DVR.

3. MODULATION STRATEGY

Usually stair case modulation is commonly used for cascaded H-bridge converters. For SCM, the switching instants of each module are calculated offline to attenuate certain harmonics In that case dc link voltage has to be varied in accordance to the desired ac output voltage. Due to bulk dc link voltage dynamic response slows down. As the voltage sag duration ranges from half cycle to 30 cycles, fast dynamic response is required for the

DVR application. Based on this consideration, Phase shifted PWM modulation scheme is adopted to maintain a relatively constant dc link voltage while achieving the fast dynamic response required of the output voltage by varying modulation index.

Multilevel inverters require carrier based modulation schemes due to higher levels. The carrier-based modulation schemes for multilevel inverters are classified as phase-shifted and level-shifted modulations. Multilevel inverter with m voltage levels requires (m-1) triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the peak-peak amplitude with phase shift between any two adjacent carrier waves given by

$$\phi_{cr} = \frac{360^{\circ}}{(m-1)} \quad \text{……..} \quad (5)$$

The sinusoidal signal $V_{control}$ is phase-modulated by means of the angle α.
i.e.,

$$V_A = \sin(\omega t + \delta) \quad \text{……} \quad (6)$$

$$V_B = \sin(\omega t + \delta - 2\pi/3) \quad \text{……} \quad (7)$$

$$V_C = \sin(\omega t + \delta + 2\pi/3) \quad \text{……} \quad (8)$$

The modulated signal $V_{control}$ is compared against a phase shifted triangular signals in order to generate the switching signals for the VSC valves. The Fig 3 shows the pulses for one phase. The main parameters of the phase shifted PWM scheme are the amplitude modulation index of signal, and the frequency modulation index of the triangular signal.

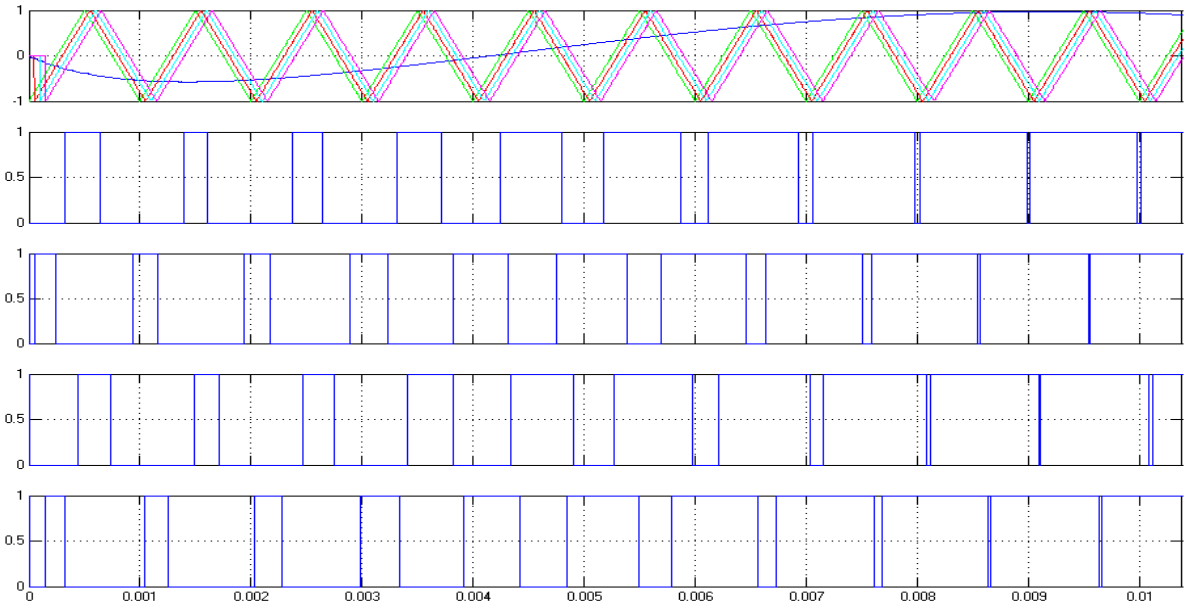

Fig 3. Phase-Shifted PWM pulses for one phase

The amplitude index is kept fixed at 1 pu, in order to obtain the highest fundamental voltage component at the controller output.

$$M_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} = 1.p.u \quad \text{……..} \quad (9)$$

Where

$\hat{V}_{control}$ is the peak amplitude of the control signal

$\hat{V}_{tri}$ is the peak amplitude of the triangular signals

The switching frequency is set at 2000 Hz. The frequency modulation index is given by

$M_f = f_s/f_1$ …….. (10)

Where f_1 is the fundamental frequency

The modulating angle is applied to the PWM generators in phase A. The angles for phases B and C are shifted by 120^0 and 240^0, respectively. It can be seen in that the control implementation is kept very simple by using only voltage measurements as the feedback variable in the control scheme. The speed of response and robustness of the control scheme are clearly shown in the simulation results. The voltage level and switching state of the five level CHB (Cascaded H-bridge inverter) is as shown in the Table1

Table 1: Voltage level and switching states of five level CHB

Output Voltage Van	Switching State					
	S11	S31	S12	S32	Vh1	Vh2
2E	1	0	1	0	E	E
E	1	0	1	1	E	0
	1	0	0	0	E	0
	1	1	1	0	0	E
	0	0	1	0	0	E
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
	1	0	0	1	E	-E
	0	1	1	0	-E	E
-E	0	1	1	1	-E	0
	0	1	0	0	-E	0
	1	1	0	1	0	-E
	0	0	0	1	0	-E
-2E	0	1	0	1	-E	-E

4. PI CONTROLLER

The fig 4 shows the process to be regulated. The circuit comprises of multilevel inverter with an output LC filter. As per fig 4, output voltage of filter is given by

$$V_s = \frac{1}{LCS^2 + RCS + 1} V_{inv} + \frac{LS + R}{LCS^2 + RCS + 1} I_L \tag{11}$$

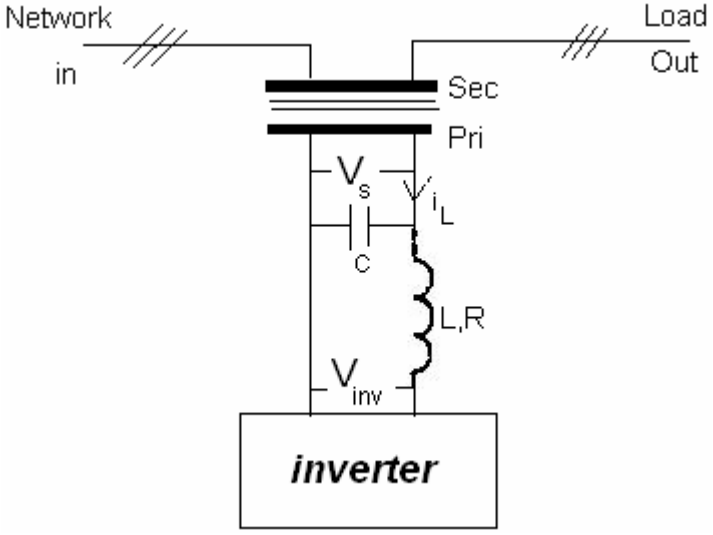

Fig 4: Process to be regulated

Where V_s, V_{inv}, i_L is the filter output voltage, inverter output voltage and transformer primary current. The function of the filter is to block the ripple frequency by its low pass function without modifying the reference signal. The eqn. (11) indicates that the output voltage of the filter is affected by the transformer current as a disturbance. This disturbance has an adverse effect on the controller and indirectly on the dc energy source

which has to supply the power required. Fig 5 represents the closed loop system of a plant with PI controller placed in feed forward path. The reference signals to be generated by DVR will be regulated by a PI or RST controller [13]. Parameters of regulation system ensures the short response time and acceptable reject perturbation caused by the load current i_L crossing the active conditioner and perturbing the injected voltage V_{inv} on the output filter capacitor terminals C. The plant (LC filter) transfer function is given by

$$G(S) = \frac{1}{LCS^2 + RCS + 1} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (12)$$

LC values are chosen to have cut-off frequency of 650 Hz. Assuming K_p and K_i be the proportional and integral gain values, the controller transfer function can be written as

$$C(S) = K_P + \frac{K_I}{s} \quad \text{……..} \quad (13)$$

The closed loop transfer function of the system is given by

$$G_o(S) = \frac{G(s)}{1 + G(s)} \quad \text{……..} \quad (14)$$

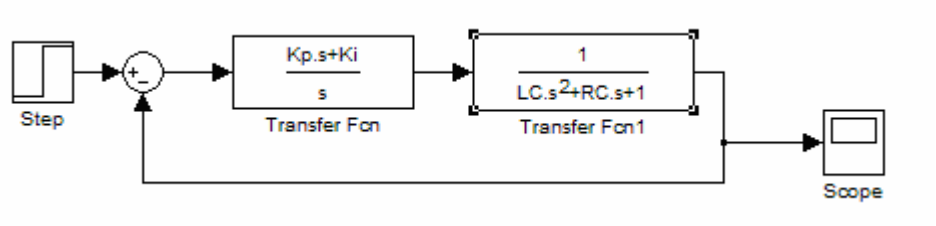

Fig 5: PI controller

The characteristic equation of the closed loop system is given by

$$G(S) = s^3 + 2\zeta\omega_n s + (\omega_n^2 + K_P\omega_n^2)s + \omega_n^2 K_i \quad (15)$$

Where ζ and ω_n are obtained from the plant transfer function by the formulae

$$\zeta = R/2\omega_n L \quad (16)$$

$$\omega_n = \frac{1}{\sqrt{LC}} \quad (17)$$

Since G_{cl} (s) is of third order form, it can be written as $P_1(s)P_2(s)$, where $P_1(s)$ corresponds to dominant pole and $P_2(s)$ corresponds to auxiliary poles chosen depending on poles of the plant. i.e., if plant poles are complex, then auxiliary poles will be also complex. If complex pole is chosen as auxiliary, then it must have its conjugate. $P_1(s)$ & $P_2(s)$ are arbitrarily chosen as real and complex conjugate poles.
Choosing the desired values of peak time, settling time and overshoot, the values of desired damping factor and frequency are obtained. The characteristic equation with desired values is given by

$$G_{clp}(S) = s^2 + 2\zeta_d\omega_d s + \omega_d^2 \quad (18)$$

Since *Gcl*(s) is of third order form, an extra dominant pole is added. G_{clp} (s) now can written as

$$G_{clp}(S) = (s + a)(s^2 + 2\zeta_d\omega_d s + \omega_d^2) = P_1(s)P_2(s) \quad (19)$$

The values of a , ζ_d and ω_d are chosen arbitrarily in order to modify the rise time, zero steady state error and less settling time
a = 133, ζ_d = 0.02 and ω_d = 4851.96 rad/sec.
Substituting these values in eqn. (19)

$$G_{clp}(S) = s^3 + 333.130s^2 + 2356899.8s + 3147612188 \quad (20)$$

Comparing the equating eqns. (15) and (19), values of K_p and K_i are obtained.

The step response of the system with PI controller without and with step disturbance is shown in fig 6 and Fig 7.

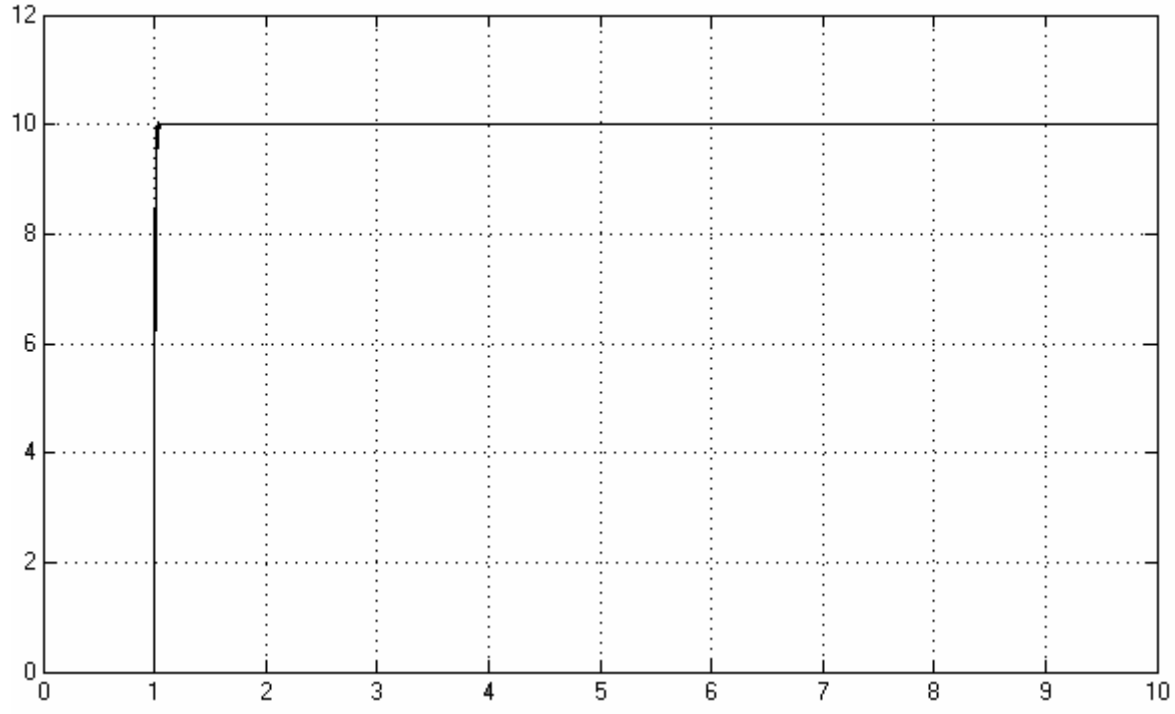

Fig 6: Step response of closed loop system with PI controller without disturbance

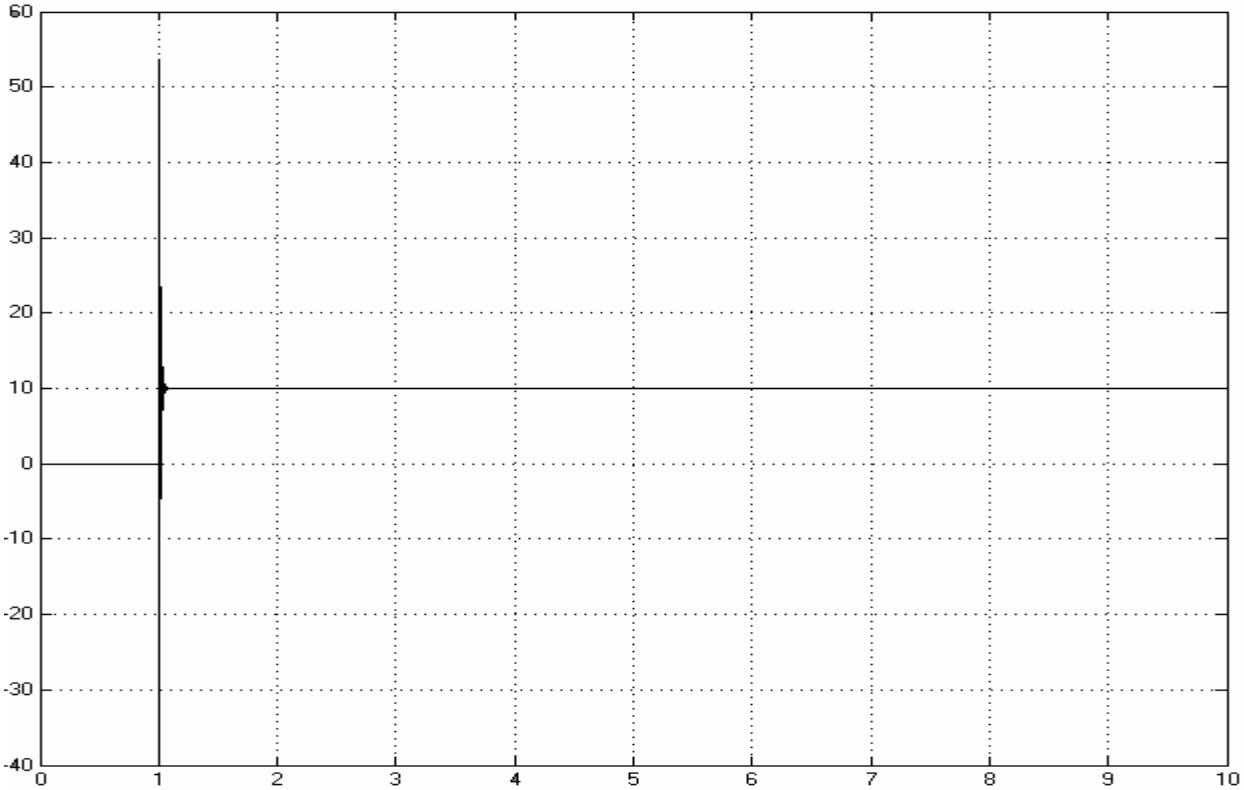

Fig 7: Step response of closed loop system with PI controller and disturbance of u (t) =5

PI controller does not have disturbance rejection capability. So it cannot track the input signal accurately in the presence of disturbance as shown in fig 7. This disturbance will increase the stress on the PWM controller and indirectly increase dc energy required. The controller input is an error signal obtained from the reference voltage and the r.m.s value of the terminal voltage measured. Such error is processed by a PI controller to track the error. PI output is provided to the carrier PWM signal generator. It is important to note that in this case,

indirectly controlled converter, there is active and reactive power exchange with the network simultaneously: an error signal is obtained by comparing the reference voltage with the r.m.s voltage measured at the load point.

5. RST CONTROLLER

RST control realizes a relevant approach for linear single input and single output (SISO) systems. In this paper RST controller is considered to obtain better output disturbance rejection while keeping a good regulation and a good robustness. RST controller has been widely used in many industrial applications [16].The robustness of RST controller via law of generalized predictive control is proposed [17]. The Diophantine equation is widely used for sinusoidal reference signal tracking[18]. The filter output voltage function can be written as

$$V_s = \frac{1}{LCS^2 + RCS + 1} V_{inv} + \frac{LS + R}{LCS^2 + RCS + 1} I_L = \frac{B(s)}{A(s)} V_{inv} + \frac{D(s)}{A(s)} I_L \tag{21}$$

RST controller shapes the compensating voltage to the reference voltage while rejecting the effect of disturbance i_L. The fig 8 shows the RST controller for signal tracking.

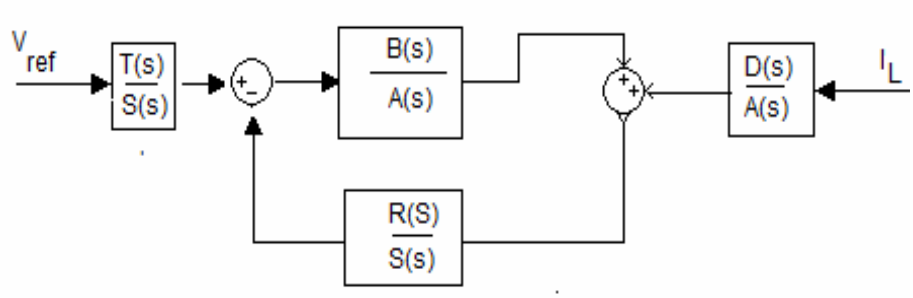

Fig 8: RST controller for Tracking

From the fig 8, transfer of closed loop is given by

$$V_s = \frac{T.B}{S.A + BR} V_{ref} + \frac{S.D}{S.A + B.R} I_L \tag{22}$$

Neglecting the disturbance, controller will track the reference signal only when the closed loop gain becomes unity. i.e

$$\frac{T.B}{S.A + BR} = 1 \tag{23}$$

Unity can be obtained with proper selection of RST polynomials. Polynomial T(s)/S(s) is a feed-forward compensator and R(s)/S(s) is the feedback compensator. An arbitrary polynomial is chosen such that AS+BR=E. This equation is based on bezout equation. For proper regulation, deg (R) =deg (S) ≤ deg (A) – 1and if n is the deg (A), then deg (E) ≥ 2n-1.

Procedure for selecting RST polynomials

1. Select the degree of polynomials.
2. $A(s).S(s) + B(s).R(s) = P_1(s).P_2(s) = E(s)$
3. $P_1(s)$ corresponds to the dominant closed pole chosen to satisfy the desired regulation performance.
4. $P_2(s)$ corresponds to the auxiliary poles which can be introduced either for filtering effects in frequency regions or improving the robustness of the closed loop system.
5. Compute the pre-filter T(s) = 1/B(1), if B(1) ≠ 0
   1, if B (1) = 0
6. $P_1(s)$ is selected as real root and $P_2(s)$ is selected as complex conjugate poles as the roots of A(s) are complex.

From the eqn (21), it is evident that deg (A) = 2. As per good regulation criteria,
deg (R) =deg(S) =1 and deg (E) is 3.So,
Polynomials R(s) & S(s) will be (R_1s+R_0) and (S_1s+S_0).

$$A(s) = LCS^2 + RCS + 1 = A_2 s^2 + A_1 s + A_0 \tag{24}$$

$$B(s) = B_2 s^2 + B_1 s + B_0 \quad , (B_2 = B_1 = 0) \tag{25}$$

$$E(s) = E_2 s^2 + E_1 s + E_0 \tag{26}$$

As per step2 in the procedure, A(s).S(s) +B(s).R(s) = E(s). The equation in matrix form is given by

$$\begin{pmatrix} A_2 & B_2 & 0 & 0 \\ A_1 & B_1 & A_2 & B_2 \\ A_0 & B_0 & A_1 & B_1 \\ 0 & 0 & A_0 & B_0 \end{pmatrix} \begin{pmatrix} S_1 \\ R_1 \\ S_0 \\ R_0 \end{pmatrix} = \begin{pmatrix} E_3 \\ E_2 \\ E_1 \\ E_0 \end{pmatrix} \tag{27}$$

This matrix is also called Sylvester matrix. The values of E(s) matrix is chosen based on steps 3 & 4.

Since the roots of A(s) are -167± 4079i, $P_2(s)$ must be complex conjugate poles and $P_1(s)$ will be dominant real pole.

$P_1(s)$ and $P_2(s)$ are chosen based on sensitivity functions, which are given by

$$S_{yy} = \frac{AS}{AS + BR} = \frac{KP}{1 + KP}$$

$$S_{yb} = \frac{-BR}{AS + BR} = \frac{-KP}{1 + KP}$$

$$S_{yu} = \frac{BS}{AS + BR} = \frac{P}{1 + KP}$$

$KP=L_{yy}$

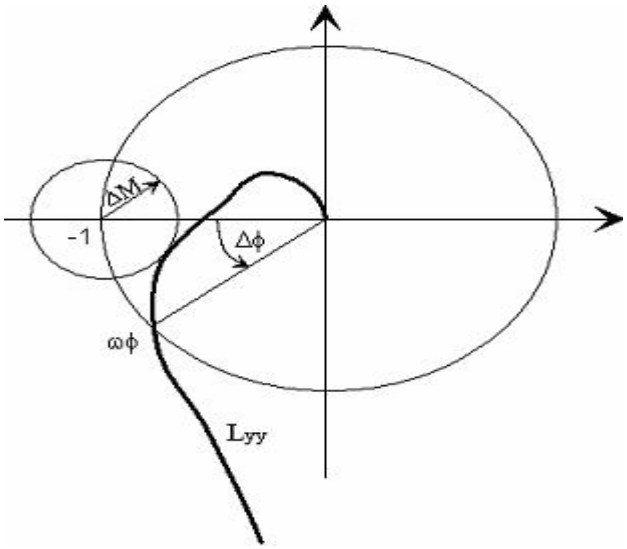

Fig 8a: Nyquist plot of L_{yy}

For an output disturbance with a pulsation of ω_1 (LC filter resonance), the gain of S_{yy} on ω_1 gives the information on the disturbance rejection. Denominator $D = AS + BR$ determines the dynamics of disturbance rejections. For an output disturbance with the pulsation of ω_1, the lower gain of Syy at ω_1, better the attenuation of the output disturbance rejection. However, the diminution of S_{yy} at $\omega_1$can induces an augmentation of the maximum value of Syy which is inversely proportional to ΔM. The fig 8a depicts the ΔM, Δφ, which are obtained from the nyquist plot of L_{yy} The diminution of ΔM reduces the controller robustness. In this paper, RST controller is designed keeping only robustness in terms of disturbance rejection. If robustness in terms of both disturbance rejection and stability required, then RST polynomials must be chosen for appropriate module, phase and delay margins (ΔM, Δφ , Δτ).

The polynomial $P_1(s).P_2(s)$ is given by

$$E = s^3 + 4502s + 1.3764E11s + 1.6792E13 \tag{28}$$

Equating AS+BR=E, RST polynomials can be obtained. The step responses of RST controller is shown in the fig 9.

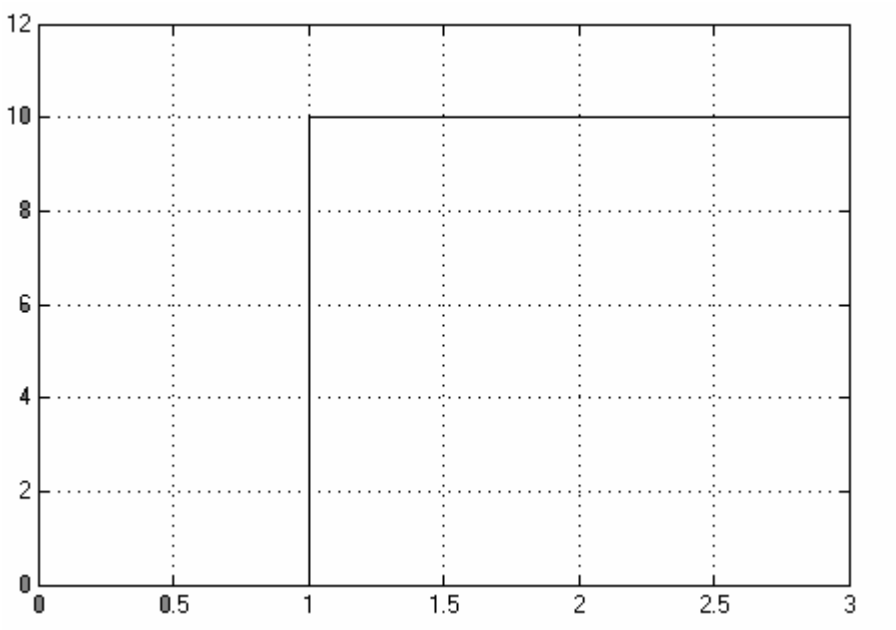

Fig 9: Step response of RST controller without disturbance

The RST controller is tested for robustness by adding the step disturbance to the controller.

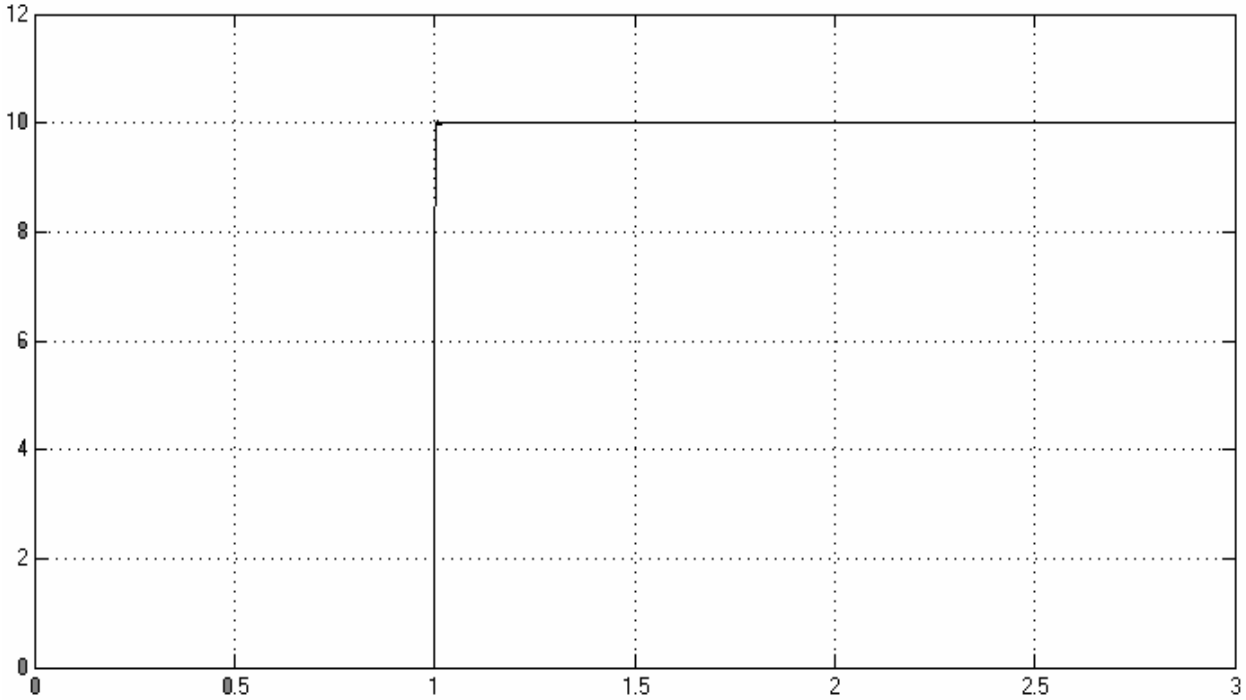

Fig 10: RST controller with step disturbance of u (t) =5

Fig 10 represents the output of RST controller with step disturbance, which shows the accuracy of RST controller in tracking the input signal with disturbance.

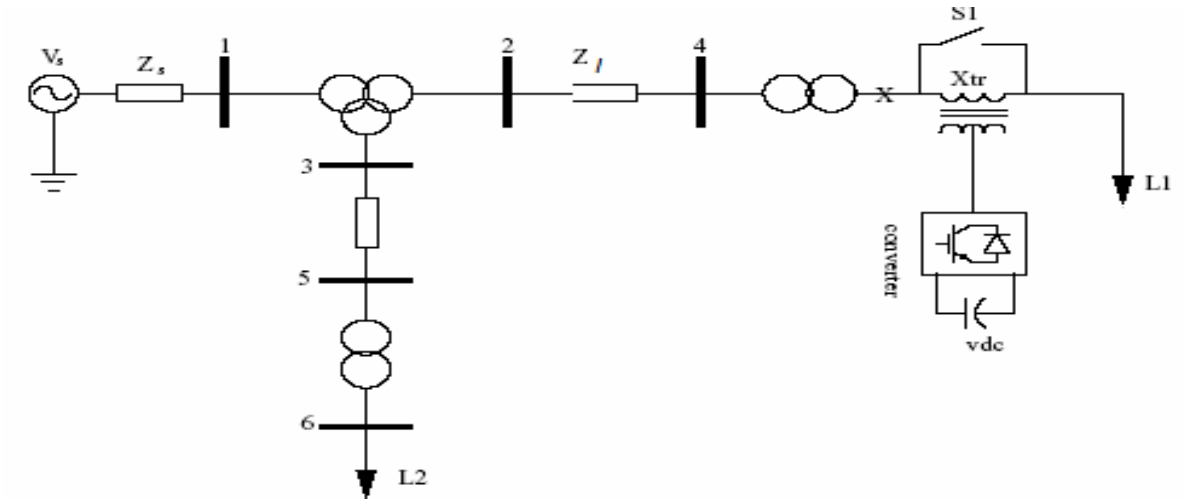

Fig 11: Single Line diagram of test system for DVR

6. TEST SYSTEM

Single line diagram of the test system for DVR is shown in Figure-11 and the test system employed to carry out the simulations for DVR is shown in Figure-12. Such system is composed by a 13 kV, 50 Hz generation system, feeding two transmission lines through a 3-winding transformer connected in Y/Δ/Δ, 13/115/15 kV. Such transmission lines feed two distribution networks through two transformers connected in Δ/Y, 15/11 kV. To verify the working of a DVR employed to avoid voltage sags during short-circuit, a fault is applied at point X via resistance of 0.4Ω. Such fault is applied for 100msec. The capacity of the dc storage is 0.9KV. Using facilities available in MATLAB/SIMULINK the DVR is simulated to be in operation only for the duration of the fault as it is expected to be the case in practical situation. Power System Bock set for the use with Matlab Simulink is based on state-variable analysis and employs either variable or fixed integration-step algorithms. Figure- 12 shows the simulink model of the test system for DVR.

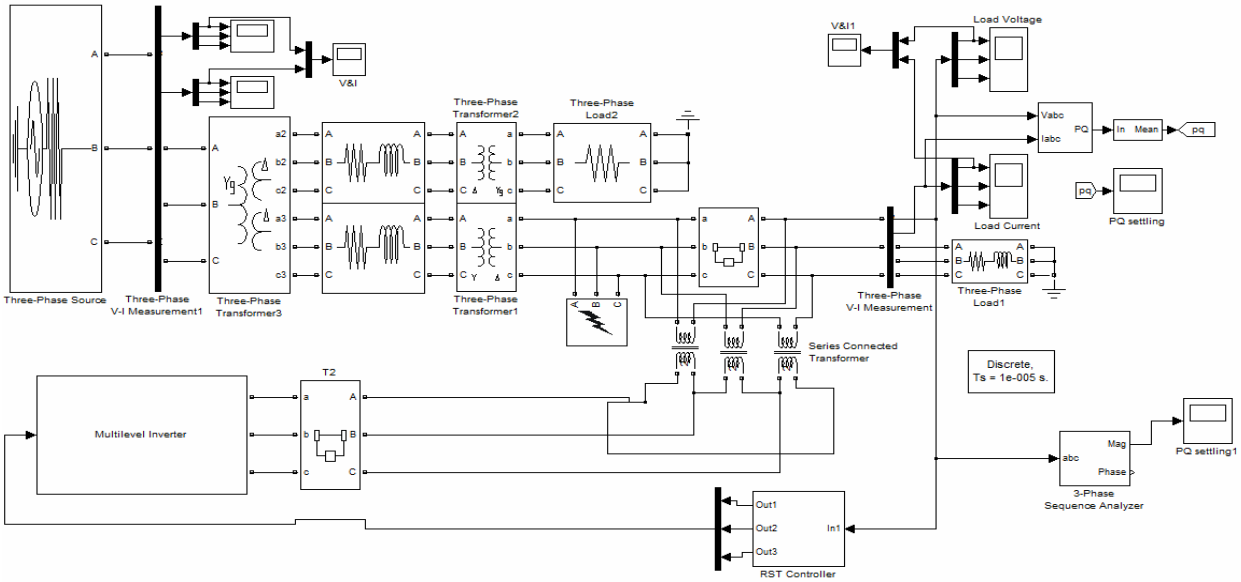

Fig 12: Simulink model of a DVR test system for voltage sag

7. RESULTS AND DISCUSSION

Case 1: Simulation results of voltage during single line to ground fault

The first simulation contains no DVR and a LLL fault is applied at point A in Figure-11 via a fault resistance of 0.66Ω, during the period 500-900msas shown in figure-13. The voltage sag at the load point is 20% with respect to the reference voltage. The corresponding three phase load voltages are shown in figure-14. The second

simulation is carried out using the same scenario as above but now with the DVR in operation. The total simulation period is 1400ms.

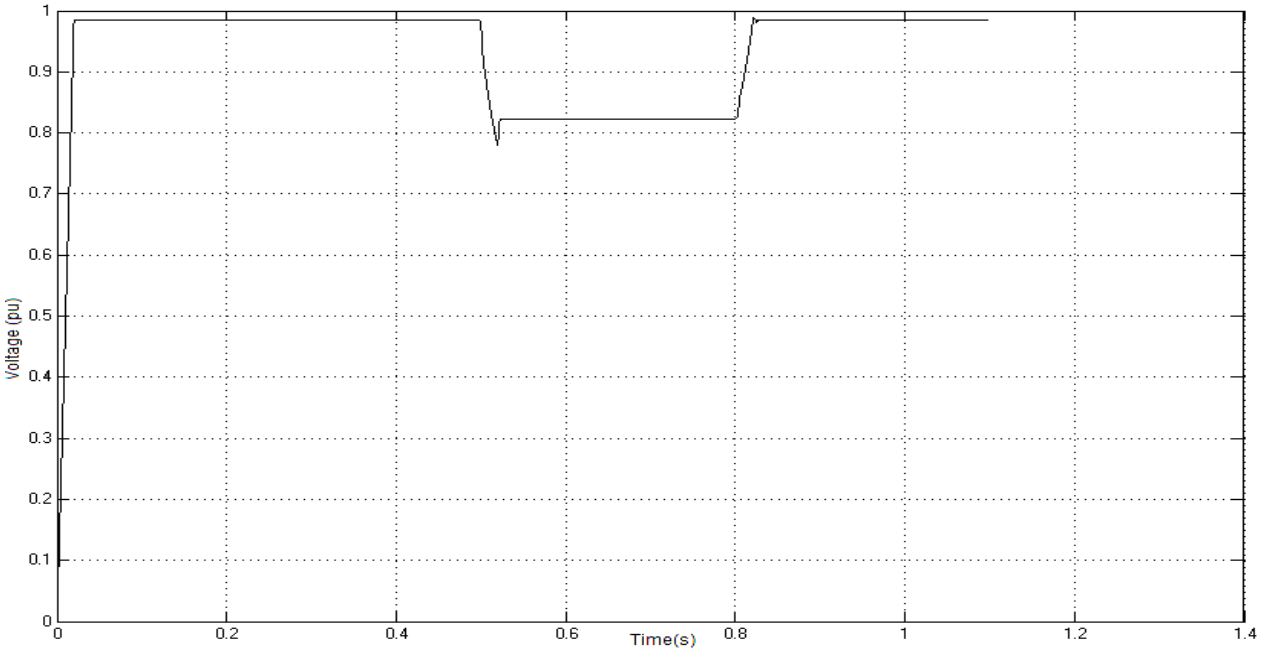

Fig 13: Load Voltage without DVR-voltage sag

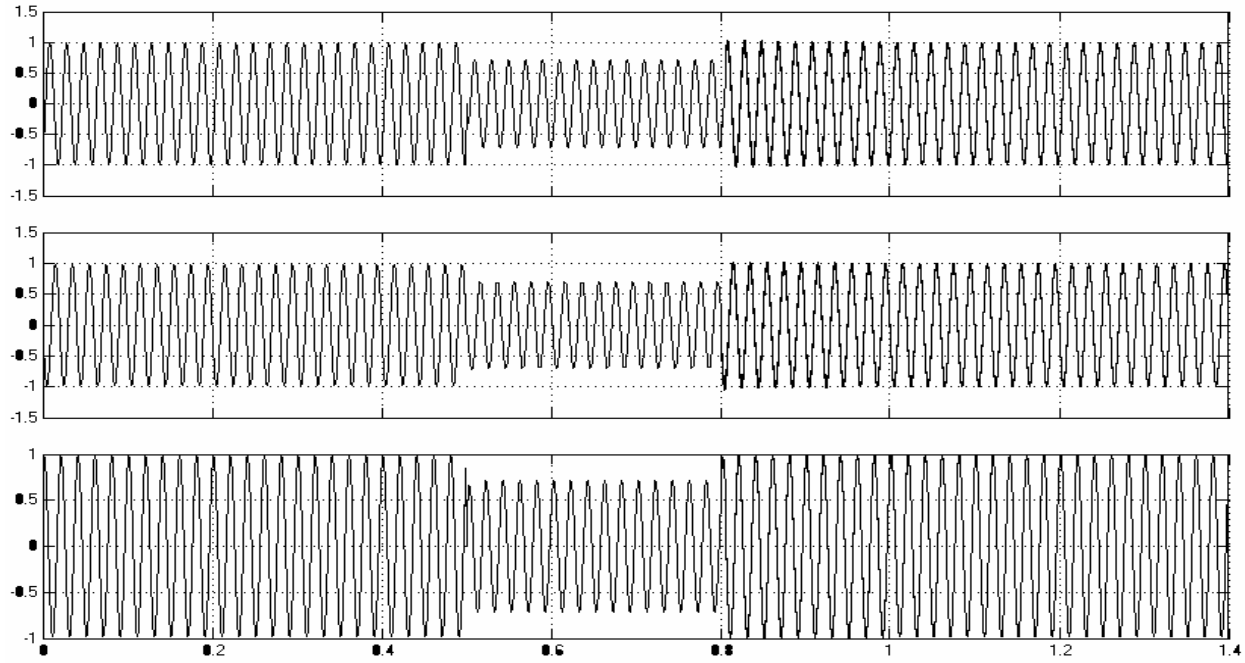

Fig 14: Three phase load voltages without DVR

When the DVR (with PI controller) is in operation the voltage sag is mitigated almost completely, and rms voltage at the sensitive load point is maintained at 98% as shown in figure-15. The total harmonic distortion is observed to be 16% at the load end.

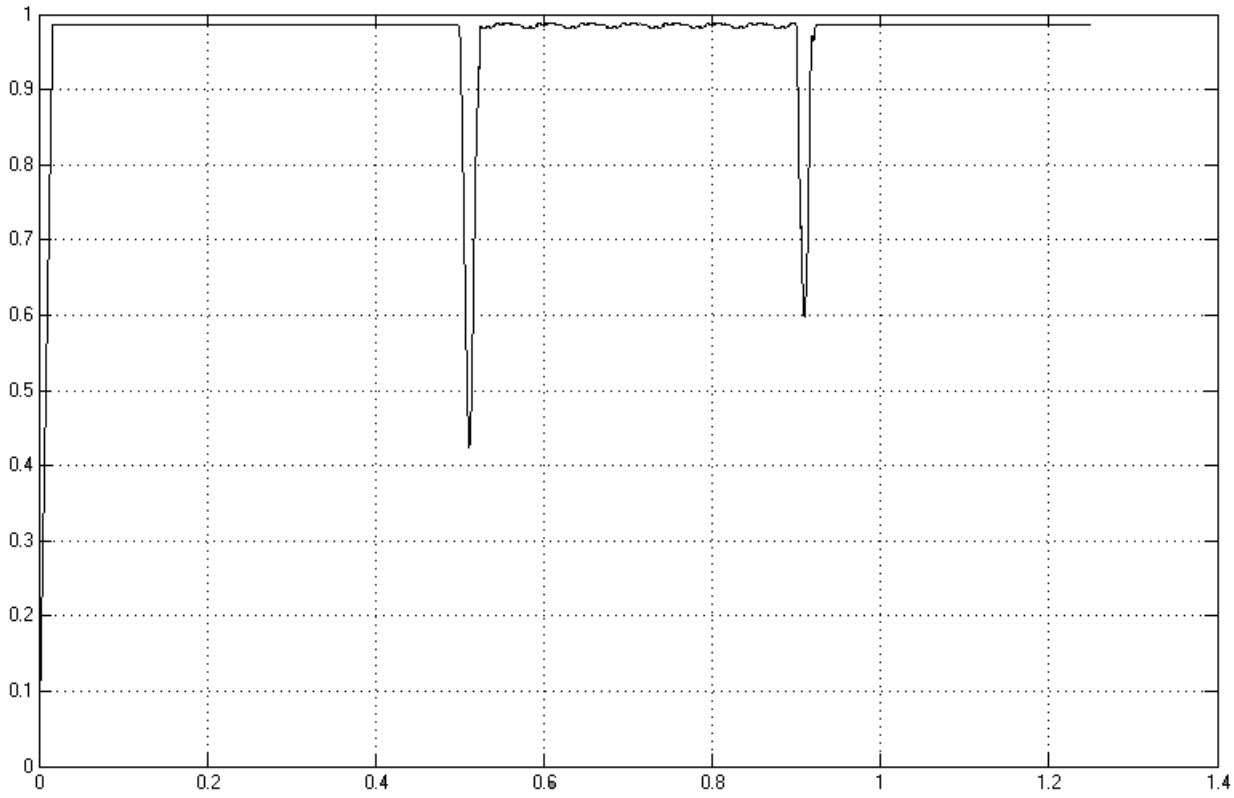

Fig 15: .Load voltage with DVR –mitigation of voltage sag

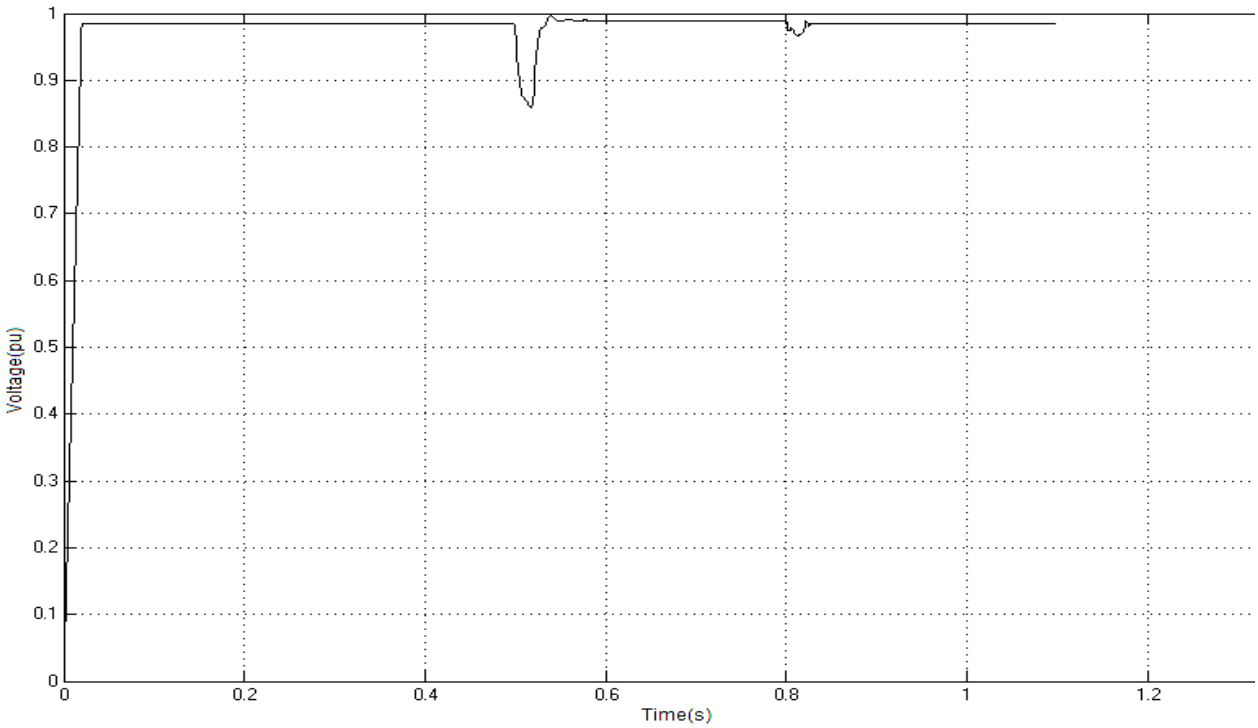

Fig 16: Load voltage with RST controller based DVR

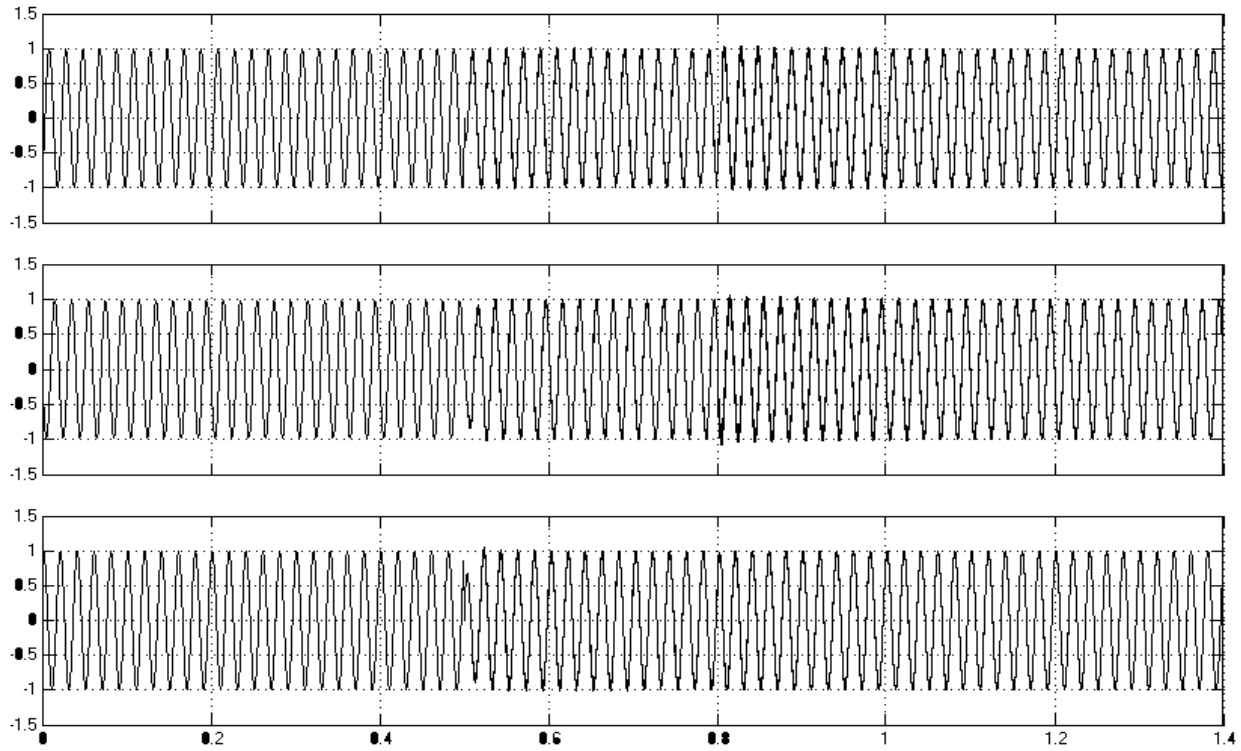

Fig 17: Three phase load voltages with DVR

Fig 16 Shows the DVR with RST controller injecting voltage for mitigating voltage sags at the load end. The corresponding three phase voltages are shown in figure-17. The total harmonic distortion is observed to be 0.84%, which depicted in fig 18.

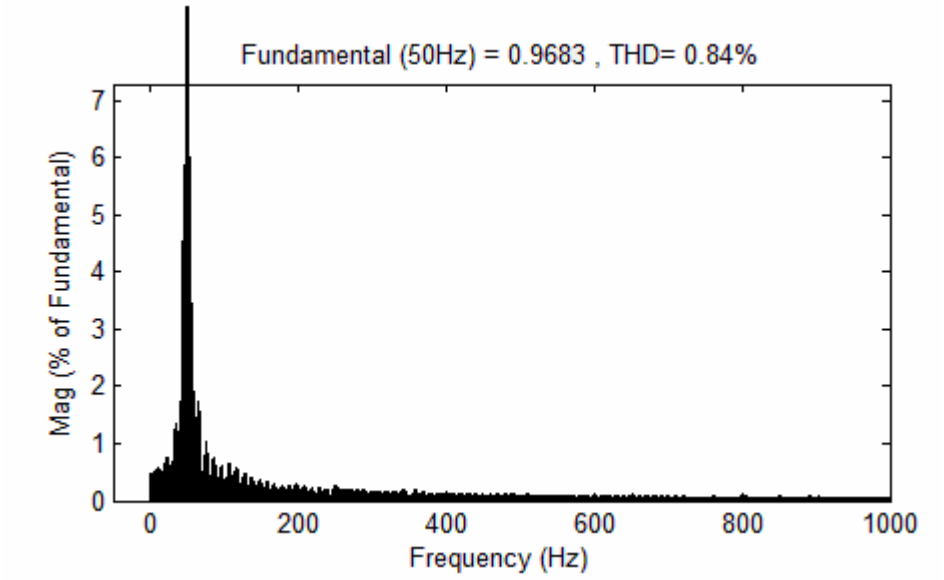

Fig 18: FFT analysis of load voltage

As seen for from fig 14, switching transients are also reduced compared to PI controller. This is mainly due to its ability of disturbance rejection and accurate signal tracking, which reduces stress on PWM controller and inverter.

Case 2: Simulation result of voltage interruption during three phase fault

The first simulation contains no DVR and three phase fault is applied at point A in fig 11, via a fault resistance of 0.001Ω, during the period 500-900ms. The voltage at the load point is 0.05% with respect to the reference voltage as shown in figs 19 & 20. The second simulation is carried out using the same scenario as above but with the DVR in operation. The total simulation period is 1400ms.

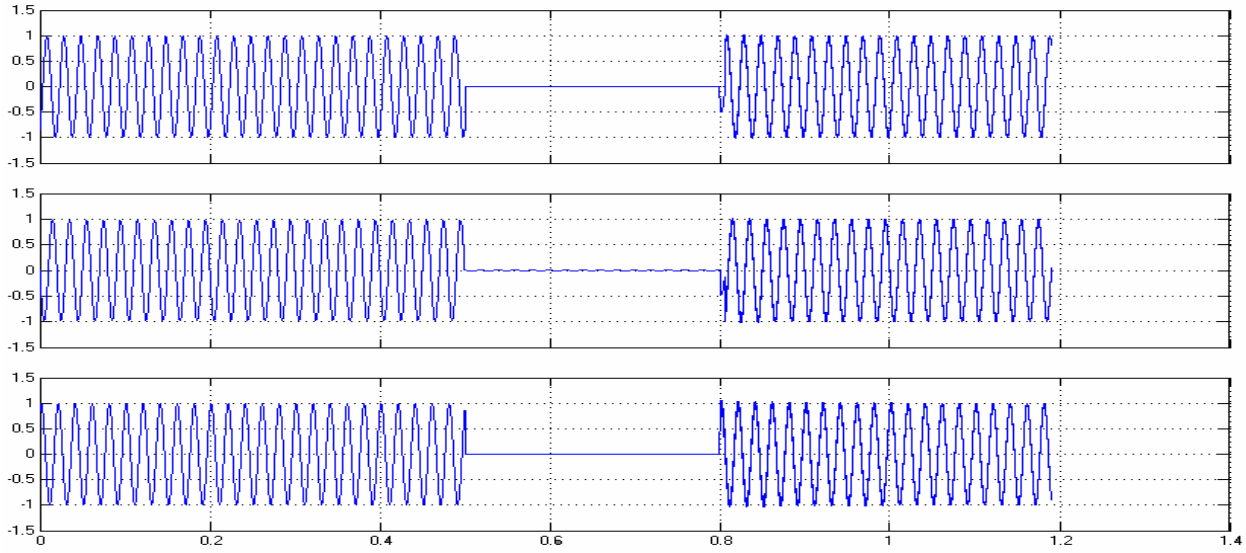

Fig 19: Three phase voltages with voltage interruption for 0.3secs.

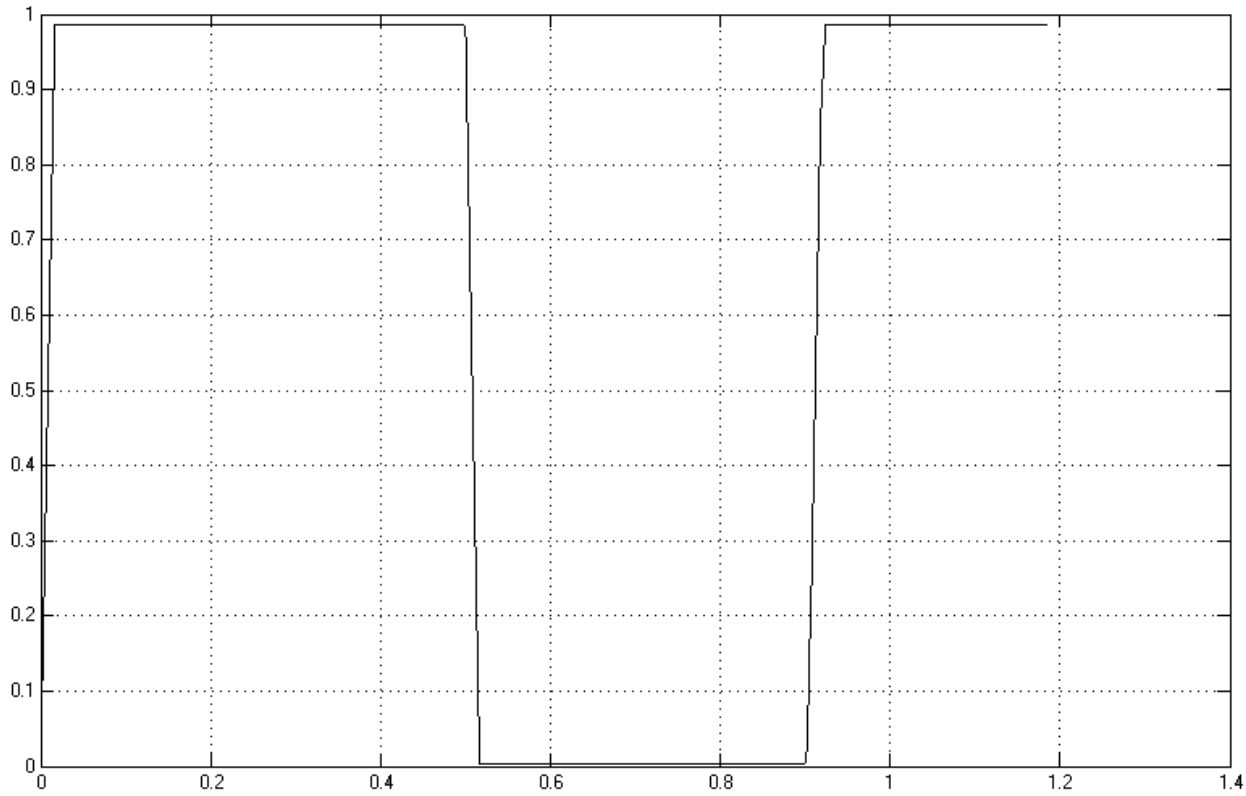

Fig 20: Load voltage without DVR-voltage interruption

When PI controller based DVR is in operation the voltage sag is mitigated almost completely and the r.m.s voltage at the sensitive load point is maintained at 98% as shown in figure 21. Fig 22 & 23 displays the load voltage with RST controller based DVR in operation and corresponding FFT analysis is shown in fig 24.

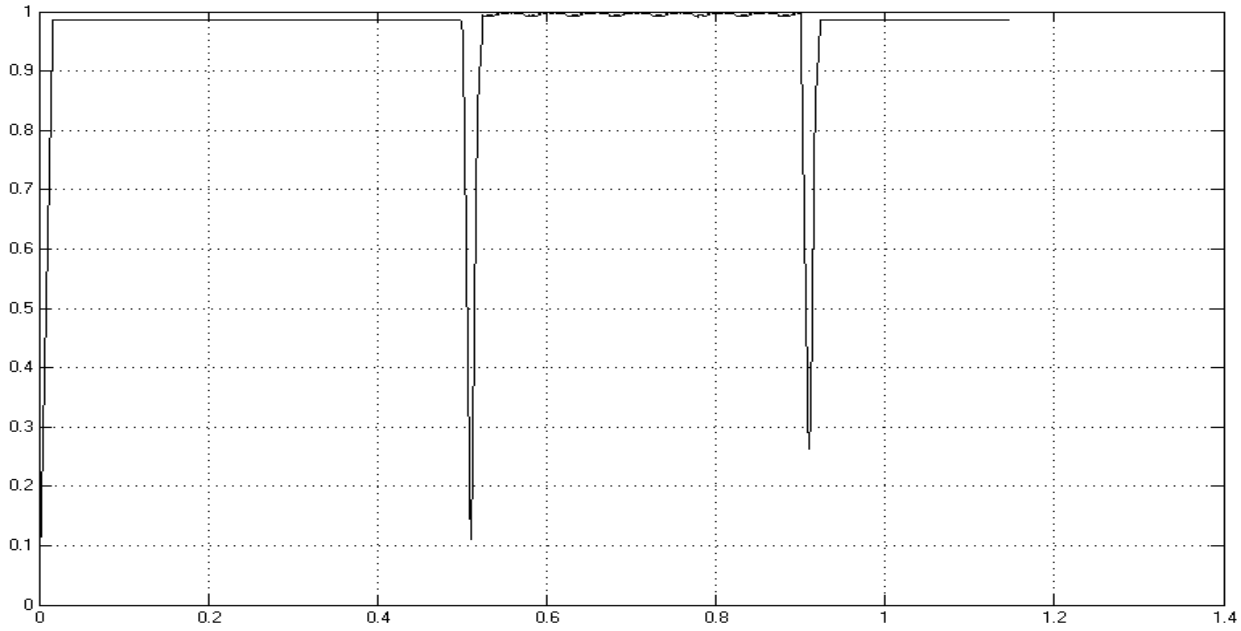

Fig 21: Load voltage with DVR-mitigation of voltage interruption with PI controller

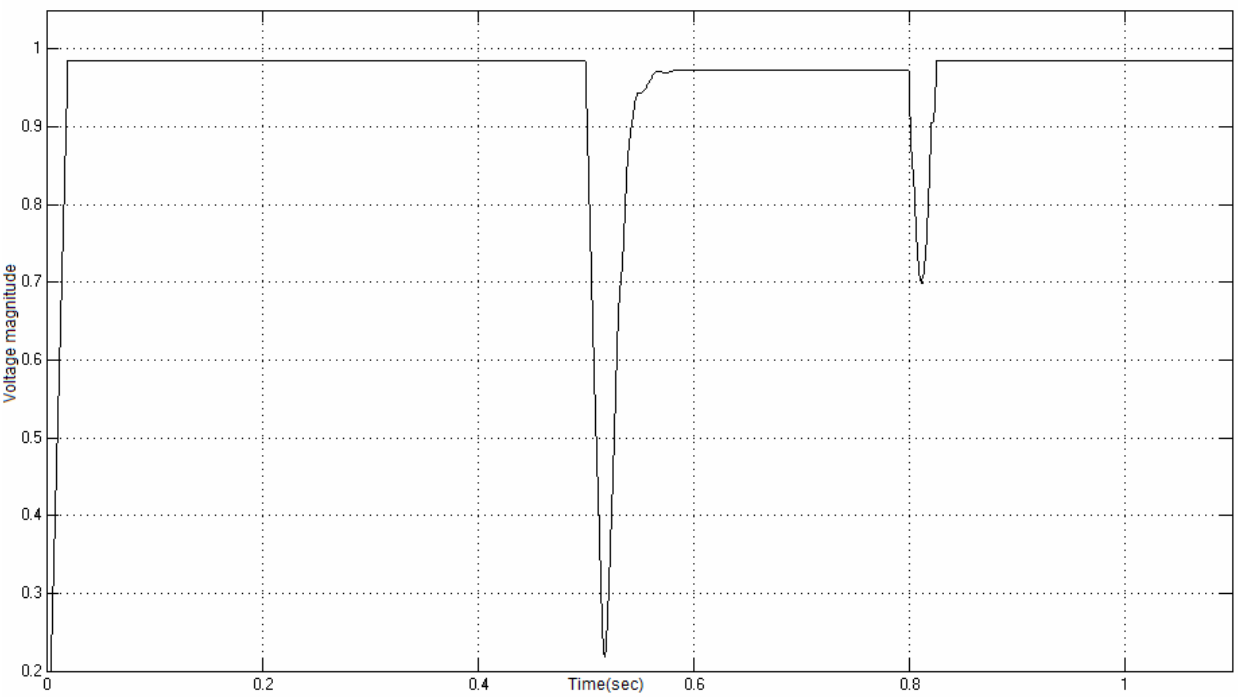

Fig 22: Load voltage with DVR-mitigation of voltage interruption with RST controller

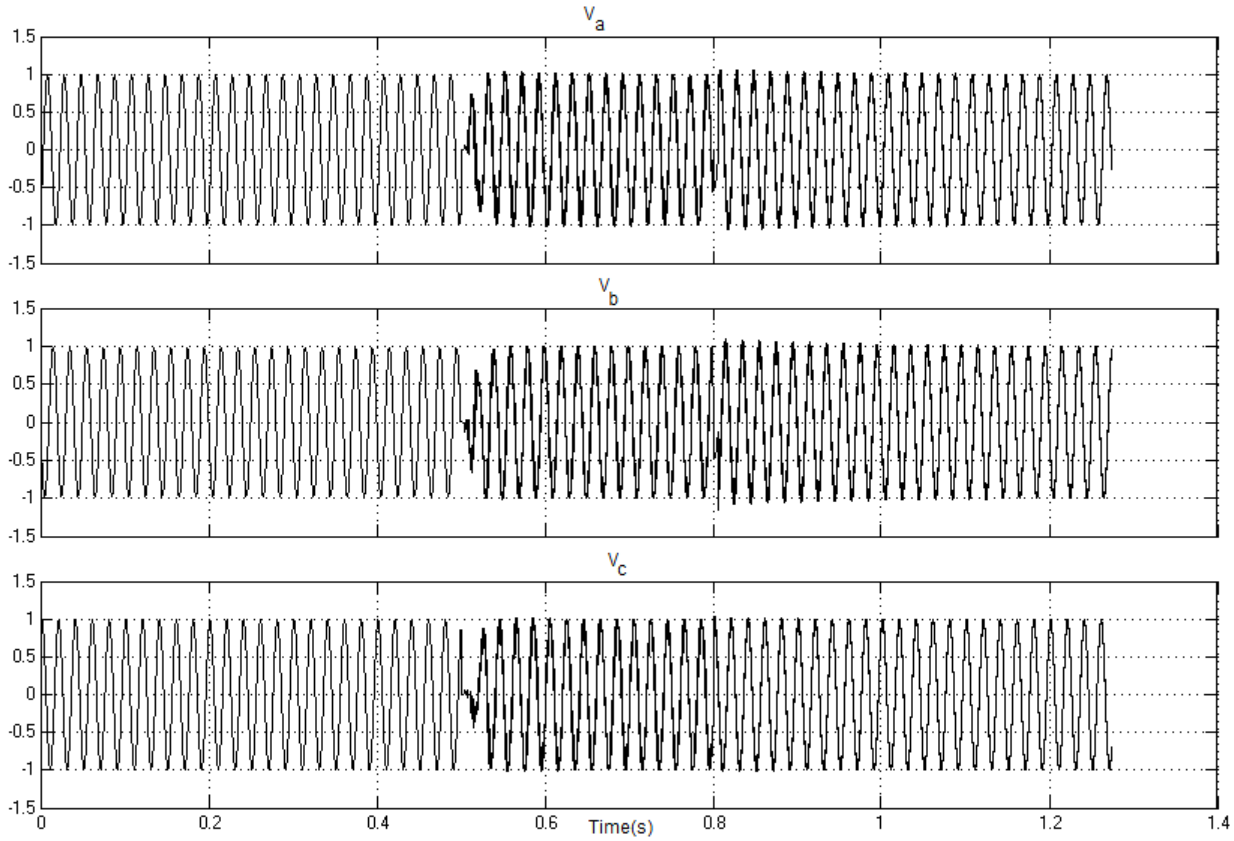

Fig 23: Three phase voltages of load with RST controller

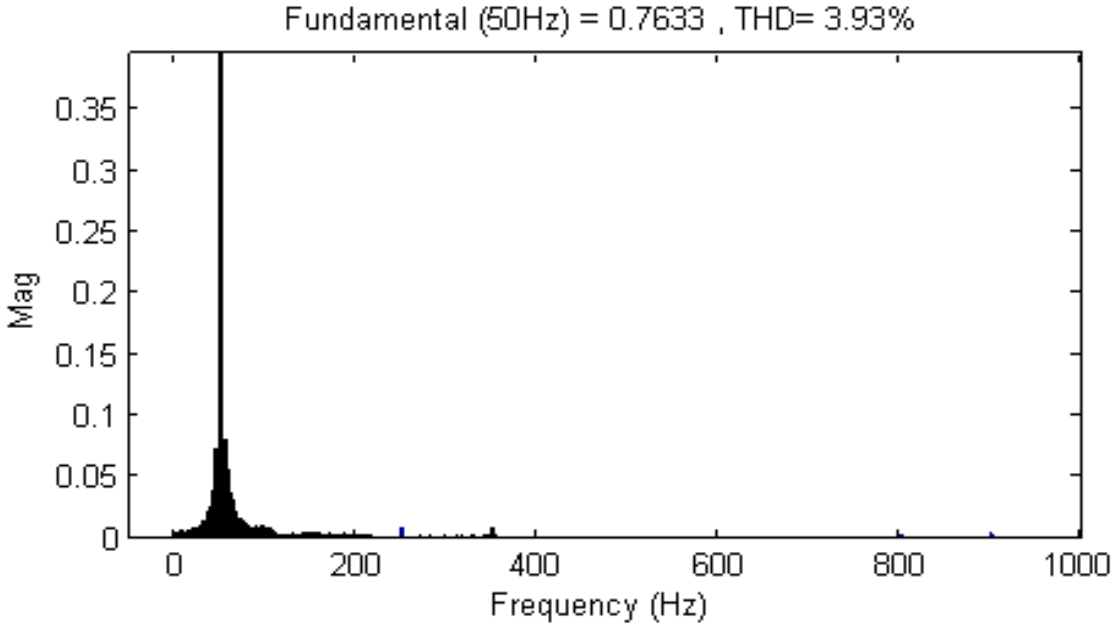

Fig 24: FFT analysis of Load voltage

7. CONCLUSIONS

This paper has presented the power quality problems such as voltage dips, interruptions, consequences and mitigation techniques of custom power electronic device DVR. The design and applications of DVR for voltage sags, interruptions and comprehensive results are presented.
This paper presents multilevel cascaded h bridge topology for DVR modeling. The carrier phase shifted modulation method is implemented to control the electronic valves in the 5-level cascaded multilevel inverter. The advantage of using phase shifted modulation scheme is very effective in maintaining load voltage constant. RST controller possesses disturbance rejection capability. Since the RST controller is able to track the exact actual signal while rejecting the disturbance present in actual signal, Stress on PWM controller is reduced to much extent which is reflected as reduction in transient spikes of the inverter.
PI and RST controller is implemented in multilevel inverter type DVR. From the results, it is observed that

- With RST controller dc voltage requirement is reduced compared to other types of controllers.
- RST controller reduces the switching transients of the inverter as shown in fig 16 & 22.
- RST controller reduces the harmonics in the utility voltages effectively.
- RST controller possesses the disturbance rejection capability without losing the stability.

The table 2 below shows comparison of PI and RST controller in terms of various aspects.

Table 2. Comparison of PI and RST controller

Type of Controller	DC Voltage requirement	THD	Robustness (Disturbance rejection)
PI	2.5kV	No effect	No
RST	1kV	Reduces to much extent	Yes

9. ACKNOWLEDGEMENT

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