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Distribution Static Compensator Performance under Linear and Nonlinear Current Regulation Methods

Reactive power compensation is an important aspect in the control of distribution systems. Reactive current in addition to increasing the distribution system losses, introduces various power quality problems like, harmonics, voltage sag, swell and poor load power factor. These power quality issues result in the malfunction of sensitive equipments. A Distribution Static Compensator (DSTATCOM) proves to be a viable solution for the mitigation of power quality problems. It provides effective compensation to linear varying/nonlinear loads by injecting appropriate reactive power at the point of common coupling (PCC). It exhibits the behavior of an active power filter and that of a voltage regulator. The choice of proper current control strategy is an important aspect in DSTATCOM performance. This paper compares linear and nonlinear methods of current regulation pertaining to DSTATCOM performance operating under Synchronous Reference Frame (SRF). The paper briefly describes the salient features of each regulation method with its merits and demerits. A dynamic model of a DSTATCOM has been developed using the two control techniques in MATLAB/SimPowerSystems environment to observe their performances and comparison.

Keywords *:* Distribution static compensator (DSTATCOM), synchronous reference frame(SRF), rotating reference frame PI controller, hysteresis current controller, load compensation

1. INTRODUCTION

Deterioration in Power Quality is the main cause of concern to utilities as well as to customers, in addition to reliability of supply. Power Quality pollution at the load end is in the form of voltage/current waveform distortions, long/short duration voltage variations and poor load power factor. Amongst the various distribution FACTs controllers, Distribution Static Compensator (DSTATCOM) is an important shunt compensator which has the potential to solve many power quality problems faced by distribution systems [1,2]. DSTATCOM has effectively replaced a Static Var Compensator (SVC), as the latter possesses a larger response time in addition to being supplemented with passive filter banks and offering only steady state reactive power compensation. Moreover SVC's which have been largely used in arc welding plants for voltage flicker mitigation have been replaced by DSTATCOM's because SVC's exhibit limited reduction of instantaneous flicker level IFL[3]. DSTATCOM also finds wide applications in distributed generation [4], small generating units [5] and wind generation applications [6]. A DSTATCOM is basically a Voltage Source Converter (VSC) based FACTS controller sharing many similar concepts with that of a STATCOM used at transmission level [7]. A STATCOM at the transmission level handles only fundamental reactive power and provides voltage support while as a DSTATCOM is employed at the distribution level or at the load end for power factor improvement and voltage regulation. Additionally, a DSTATCOM can also behave as a shunt active filter [8, 9], to eliminate unbalance or distortions in the source current or the supply voltage as per the IEEE-519 standard limits. Since a DSTATCOM is such a multifunctional device, the main objective of any control algorithm should be to make it

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flexible and easy to implement in addition to exploiting its multi functionality to the maximum. Load compensation and voltage support can both be effectively achieved by a DSTATCOM by proper choice of current control technique, which determines the switching logic of the switches used in the converter. The main objective is finally to control the instantaneous current waveform and to compensate for the dc link and ac side voltage changes, with fast response and lesser overshoot.

Various Current control techniques have been reported for VSC based controllers [10-12], but their comparative study by simulation and the filter design criteria have not been discussed. The most commonly used current control techniques in converter based shunt compensation are linear rotating reference frame PI control and a nonlinear hysteresis current control [13-16] with different reference current generation methods. Some authors have also used sinusoidal signal generators for current control which is a frequency based selection which is computationally extensive [17]. This paper compares linear and nonlinear methods of current regulation pertaining to DSTATCOM performance operating under Synchronous Reference Frame (SRF). The paper briefly describes the salient features of each regulation method with its merits and demerits. A dynamic model of a DSTATCOM has been developed using the two control techniques in MATLAB/SimPowerSystems environment to observe their performances and comparison. The simulations are done as per the system parameters given in Appendix I.

2. DISTRIBUTION STATIC COMPENSATOR

A DSTATCOM is a controlled reactive source which includes a Voltage Source Converter and a DC link capacitor connected in shunt, capable of generating and /or absorbing reactive power. It is analogous to an ideal synchronous machine, which generates a balanced set of three sinusoidal voltages at the fundamental frequency with controllable amplitude and phase angle. This ideal machine has no inertia, gives an instantaneous response, does not alter the system impedances, and can internally generate reactive (both capacitive and inductive) [18]. Fig.1 shows the basic structure of a DSTATCOM, if the output voltage of the VSC is equal to the AC terminal voltage, no reactive power is delivered to the system. If the output voltage is greater than the AC terminal voltage, the DSTATCOM is in the capacitive mode of operation and vice versa. The quantity of reactive power flow is proportional to the difference in the two voltages.

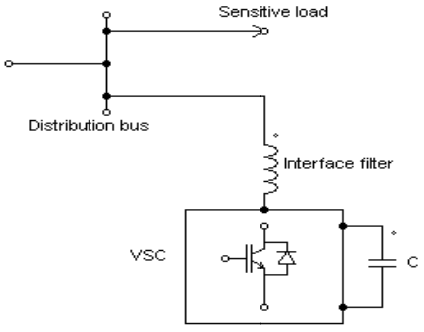


Fig.1 Basic structure of DSTATCOM

It is to be noted that voltage regulation at Point of Common Coupling (PCC) and power factor correction cannot be achieved simultaneously [19]. For a DSTATCOM used for voltage regulation at PCC the compensation should be such that the supply currents should lead the supply voltages and for power factor correction the supply current should be in

phase with the supply voltages. This paper deals with a DSTATCOM used for reactive power compensation and power factor correction.

3. MODELING OF DSTATCOM

The modeling of DSTATCOM is based on the synchronous reference frame method [16, 20]. Fig.2 shows the simplified single line diagram of a DSTATCOM, comprising of a DC link capacitor, IGBT based VSC, coupling filter and the PCC voltage

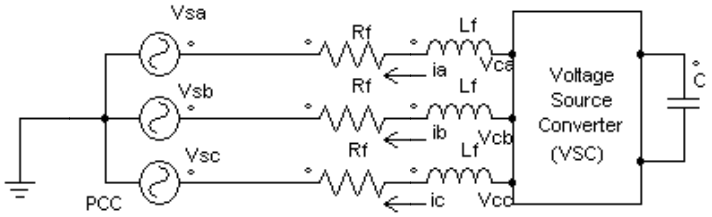


Fig. 2 Simplified model of DSTATCOM

Here,
V_{sa}, $V_{sb,}$ V_{sc} : Voltage at the Point of Common Coupling
V_{ca}, $V_{cb,}$ V_{cc} : Inverter output voltage
L_f : Inductance of the coupling filter
R_f : Equivalent filter resistance
C : DC Link capacitor
The per phase instantaneous PCC voltage is given as:

$$\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} = \sqrt{\frac{2}{3}} V_s \begin{bmatrix} \sin \omega t \\ \sin (\omega t - 2\pi/t) \\ \sin (\omega t + 2\pi/t) \end{bmatrix} \quad (1)$$

where Vs is the rms value of the PCC voltage. The relationship between the PCC voltage, inverter output voltage and the currents is given as:

$$R_f i_a + L_f \frac{di_a}{dt} = v_{sa} - v_{ca} \quad (2)$$

$$R_f i_b + L_f \frac{di_b}{dt} = v_{sb} - v_{cb} \quad (3)$$

$$R_f i_c + L_f \frac{di_c}{dt} = v_{sc} - v_{cc} \quad (4)$$

The above equations can also be written as:

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} R_f/L_f & 0 & 0 \\ 0 & R_f/L_f & 0 \\ 0 & 0 & R_f/L_f \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} v_{sa}\text{-}v_{ca} \\ v_{sb}\text{-}v_{cb} \\ v_{sc}\text{-}v_{cc} \end{bmatrix} \quad (5)$$

Transforming eqs. (2-4) to synchronous reference frame using Park's transformation the equation becomes:

$$L_f \frac{di_d}{dt} + R_f i_d = v_{sd} - mV_{dc}\cos\alpha + L_f \omega\, i_q \tag{6}$$

$$L_f \frac{di_q}{dt} + R_f i_q = v_{sq} + mV_{dc}\sin\alpha - L_f \omega\, i_d \tag{7}$$

where ω is the system frequency and m is the modulation index of the converter.Writing eq.(6-7) in matrix form,

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -R_f/L_f & \omega \\ -\omega & -R_f/L_f \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_f}\begin{bmatrix} v_{cd}-v_{sd} \\ v_{sq}+v_{cq} \end{bmatrix} \tag{8}$$

Neglecting the voltage harmonics produced by the direct and quadrature axis voltages,

$$v_{cd} = mv_{dc}\cos\alpha \tag{9}$$

$$v_{cq} = mv_{dc}\sin\alpha \tag{10}$$

As per the power balance theory, the instantaneous power at the ac-dc terminals of the inverter is equal, giving the following power balance equation,

$$v_{dc} i_{dc} = \frac{3}{2}\left(v_{cd} i_d + v_{cq} i_q\right) \tag{11}$$

And the dc side circuit equation is given as,

$$i_{dc} = \frac{3}{2} m\left(i_d \cos\alpha - i_q \sin\alpha\right) = C\frac{dV_{dc}}{dt} \tag{12}$$

Combining equations (6)-(12), the DSTATCOM model in state space can be written as:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ v_{dc} \end{bmatrix} = A\begin{bmatrix} i_d \\ i_q \\ v_{dc} \end{bmatrix} - \frac{1}{L_f}\begin{bmatrix} v_{sd} \\ 0 \\ 0 \end{bmatrix} \tag{13}$$

Where A is given as,

$$A = \begin{bmatrix} \frac{-R_f}{L_f} & \omega & \frac{-m}{L_f}\cos\alpha \\ -\omega & \frac{-R_f}{L_f} & \frac{m}{L_f}\sin\alpha \\ \left(\frac{3}{2}\right)\left(\frac{m}{C}\right)\cos\alpha & \left(\frac{-3}{2}\right)\left(\frac{m}{C}\right)\cos\alpha & 0 \end{bmatrix}$$

Since d-q axes are not stationary, and they follow the trajectory of the voltage vector, within this synchronous rotating frame, $v_s=v_{sd}$ and $v_{sq}=0$, the instantaneous active and reactive powers as per Instantaneous Reactive Power Theory are described as :

$$p = v_{sd}i_d + v_{sq}i_d = v_{sd}i_d = v_s i_d \tag{14}$$

$$q = v_{sq}i_d - v_{sd}i_q = -v_{sd}i_q = -v_s i_q \tag{15}$$

Observing the R.H.S, it can be concluded that the DSTATCOM performance can be controlled by controlling the active and reactive component of current i_d and i_q. Therefore the choice of the current regulation criteria is extremely important in the performance of DSTATCOM.

4. CONTROLLER DESCRIPTION

As observed in the previous section appropriate performance can be achieved by independent control of the decoupled currents, i_d and i_q. The controller as shown in Fig.3 is an 'indirect' controller [20], with an outer loop consisting of ac and dc voltage controllers. The inner loop is the current controller the output of which fires the IGBT bridge. It is to be noted that the reactive power control can be accomplished using both the controllers, either to achieve a unity power factor operation by compensation of reactive power demand of the connected load, or to regulate the PCC voltage by compensating the losses in the distribution line. These two operations cannot be performed simultaneously.

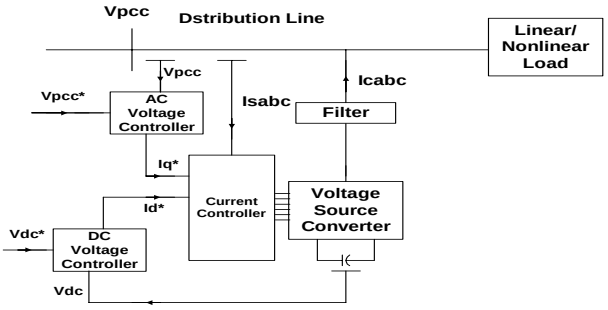


Fig.3 Indirect Control of DSTATCOM

The AC voltage loop is activated in order to achieve voltage regulation. The current i_q* is the output of a PI controller, the input to which is the deviation of the PCC voltage V_{pcc} as compared to a reference V_{pcc}*. The current i_q* is assigned zero during unity power factor operation.

The DC voltage loop is responsible for keeping constant the dc voltage through a small active power exchange with the ac network compensating the active power losses in the filter and the inverter. The output of this PI controller is i_d*, input to which is the deviation of V_{dc} from V_{dc}*. The current i_d* is responsible for unity power factor and harmonic mitigation operation in a DSTATCOM.

Once the decoupled references have been obtained, the inner current controller is activated. The Simulink model of indirect control of DSATATCOM is shown in the Fig.4. The implementation of linear/nonlinear current controllers is dealt with in the subsequent section.

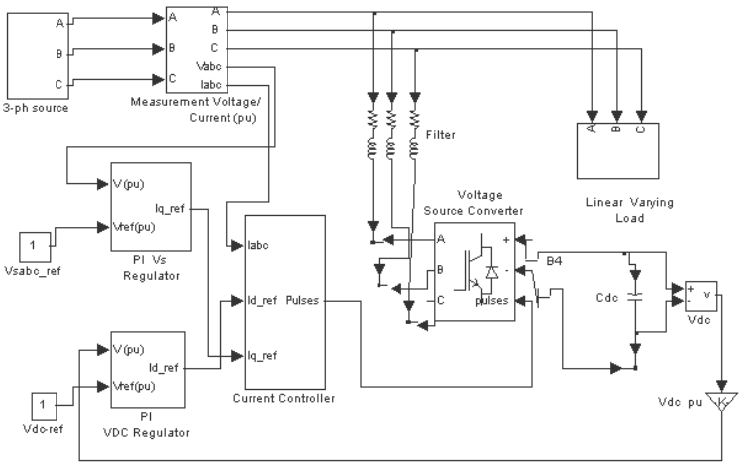


Fig.4 Simulink diagram of Indirect Current Control led DSTATCOM

5. DESIGN OF POWER CIRCUIT PARAMETERS

This includes the design of three important parameters:

- Selection of DC Link Voltage
- Selection of coupling inductance L_f
- Selection of DC Link Capacitor C_{dc}

The selection of parameters assumes a balanced AC supply and the voltage source converter operating in linear mode (0<m<1). Reference value of the dc link voltage is selected mainly on the basis of reactive power compensation capability of DSTATCOM. For satisfactory operation the dc reference magnitude should be greater than the magnitude of the source voltage V_s.

As per the compensation principle a DSTATCOM should be able to compensate reactive power to achieve unity power factor correction and improve voltage regulation which are achieved by DC loop and AC loop PI controllers respectively as shown in Fig.3. For unity power factor operation, the source current I_s should be in phase and the compensator current I_c should be perpendicular to the voltage, which is the PCC voltage, V_s. The three phase reactive power delivered from the compensator is given as [9]:

$$Q = 3V_S I_C = 3V_S \frac{V_C}{\omega L_C}\left(1 - \frac{V_S}{V_C}\right) \tag{16}$$

The above equation implies that the DSTATCOM can compensate the reactive power if and only if $V_C > V_S$. From [9],the per phase output voltage of the converter V_C is a function of the DC bus voltage and of the modulation index m is given as:

$$V_C = \frac{m}{2} \times \frac{1}{\sqrt{2}} V_{dc} \tag{17}$$

Since minimum value of V_C should be equal to the source voltage V_s and the converter is operating in the linear mode, substituting the same in the above equation the reference dc link voltage is calculated.

The coupling inductance serves as a low pass filter and plays a very important role in DSTATCOM performance. The method of generation of PWM signals significantly affects the value of coupling inductance. If fixed switching frequency PWM method is employed as in rotating reference frame controller, in order to maintain the source current THD with in 5%, the medium and higher order harmonics in the converter output voltage have to be reduced. The value of inductance calculated with this criteria is high which in turn hampers the compensation capability of the compensator [21].If variable frequency PWM method is employed, like hysteresis current controller, then the coupling inductance is designed considering the variable switching frequency. In such current controllers a dead band or a hysteresis is imposed around the reference current which is given as per the following equation [22],

$$L_f = \frac{V_{dc}}{9hf_s} \tag{18}$$

The value of DC link capacitance is chosen to limit the ripple in the dc link voltage within a permissible limit. This ripple is proportional to the maximum var handled by the compensator.

In the present case, the DSTATCOM is mainly designed to offer complete reactive power compensation. If the peak reactive power rating of the load be Q_{max}. Therefore the maximum energy the capacitor has to supply is given by [23]:

$$E_{\max} = Q_{\max} * 20 * 10^{-3} J \tag{19}$$

Let the minimum allowable dc link voltage be $V_{dc\,min}$ then :

$$E_{\max} = \frac{1}{2} C V_{dc}^{\ 2} - \frac{1}{2} C V_{dc\min}^{\ 2} \tag{20}$$

where V_{dc} is the DC link voltage at steady state and C is the value of DC link capacitor. Equating ,

$$C = \frac{2.0 * Q_{\max} * 20 * 10^{-3}}{V_{dc}(1 - k_f^{\ 2})} F \tag{21}$$

where k_f =0.6, which describes the minimum allowable dip in DC link voltage.

6. CURRENT CONTROLLER

The main objective of the control scheme is to force the currents in abc frame or dq0 frame to follow their respective reference signals and accordingly generate switching states S_a (S_b and S_c) for the switches in order to improve the tracking error. Thus the desirable features in the control scheme should be:

- Ideal tracking to remove harmonic distortions.
- Fast response under various transient conditions.
- Limited or constant switching frequency to avoid stressing of the semiconductor switches.
- Good dc link utilization

ROTATING REFERENCE FRAME CURRENT CONTROLLER (LINEAR)

The DSTATCOM Controller with rotating frame current controller is shown in Fig. 5. This controller operates in conjunction with the conventional PWM generator.

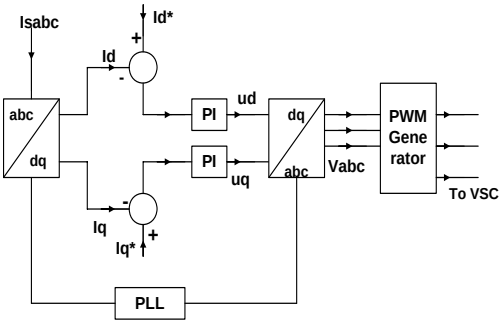


Fig.5 DSTATCOM controller using Rotating Reference frame Current Controller

The three line currents are transferred to (dq0) frame as I_{sd} and I_{sq}. The magnitudes of reference currents in (dq0) frame as I_d* and I_q* are calculated by the dc and ac voltage feedback loops respectively. In order to achieve unity power factor operation, I_q* is zero.
The modulating signals for the rotating frame controller are given by:

$$u_d = K_{p1}\left[i_d^* - i_d\right] + K_{i1}\int\left[i_d^* - i_d\right]dt$$

$$u_q = K_{p2}\left[i_q^* - i_q\right] + K_{i2}\int\left[i_q^* - i_q\right]dt$$

Where K_{p1} , $K_{i1,}$ $K_{p2,}$ K_{i2} are the gains of the two current PI controllers respectively. The modulating signals u_d and u_q are transformed back to the abc frame. The modulating signal output of each phase is compared with a triangular carrier, which is common for all the three phases.
The switching logic for the phase 'a' is formulated as:

S_a= +1 ($vc_a > v_{ct}$)

S_a= -1 ($vc_a < v_{ct}$)

Where v_{ct} is the instantaneous value of triangular carrier waveform and S_a is the switching logic for the inverter leg corresponding to phase 'a'. Similarly, the switching logic of the other two phases 'b' and 'c' are formulated as S_b and S_c.

The Fig. 6 (a-d) shows the DSTATCOM performance with a synchronous PI regulator. The waveforms shown are scaled source voltage and source current ($v_{sa,}$ i_{sa}) confirming unity power factor operation of a DSTATCOM, load current (i_{la}), compensator current (i_{ca}), and the dc link voltage (v_{dc}). The DSTATCOM is turned on at 0.06secs. An overshoot in source current is observed as soon as the DSTATCOM is turned on. This overshoot is due to the sudden rise in the dc link voltage across the capacitor from zero value. The performance during transient conditions is shown by reducing the load at 0.15 secs. by 25%. Fig. 7 shows the frequency spectrum of the source current in steady state after compensation. After compensation the %THD of the source current is 3.11%. The dc loop proportional and integral gains are 25 and 38.5 respectively. The regulator gains for both the current controllers are same as 1.8 and 105 respectively. The switching frequency of the PWM generator is 5kHz.

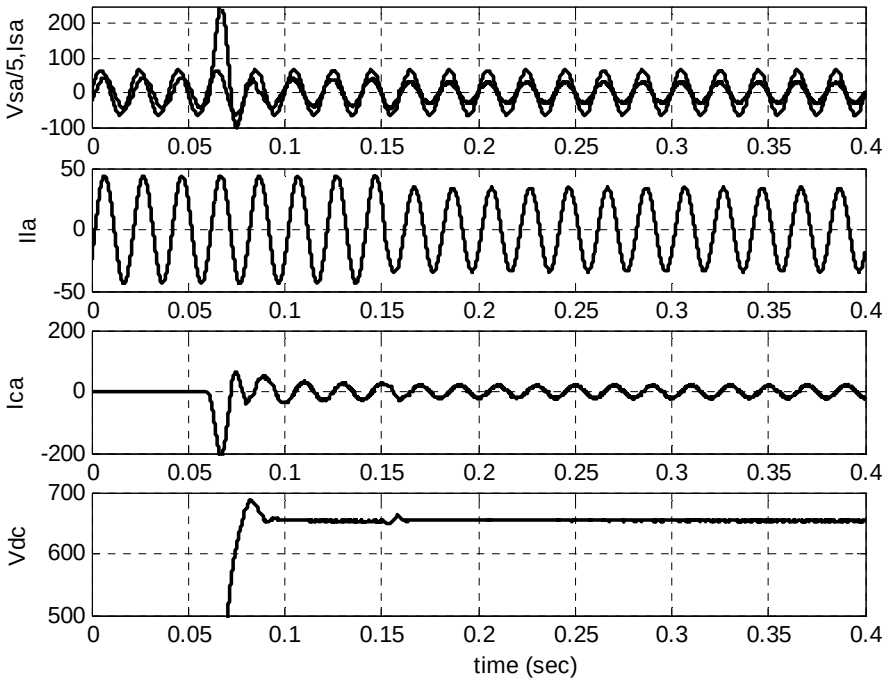


Fig. 6 Performance with DSTATCOM turned on at 0.06 secs Phase 'a' source voltage and current , load current , compensator current ,DC link voltage(Rotating reference frame PI controller)

When observing the DSTATCOM performance for a nonlinear load in Fig. 8 using rotating reference frame current controller and keeping the system parameters same, the %THD in the source current reduces from 26.88% to 18.86% only as shown in Fig 9(a-b) respectively. The major advantage of the control technique is that it operates with fixed switching frequency which provides a definite harmonic spectrum independent of load parameters. The disadvantage being, due to lack of proper tracking the overshoot and settling time are large. In case of nonlinear loads complete harmonic suppression is not achieved.

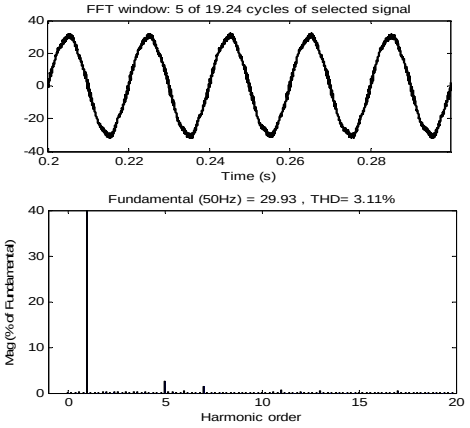


Fig 7 Frequency spectrum of source current (Rotating reference frame PI controller)

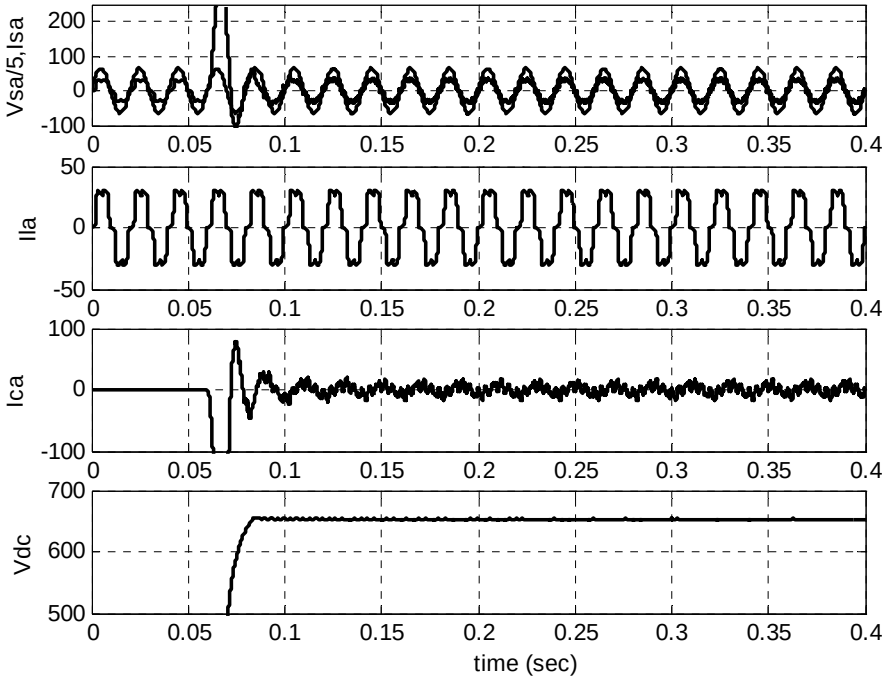
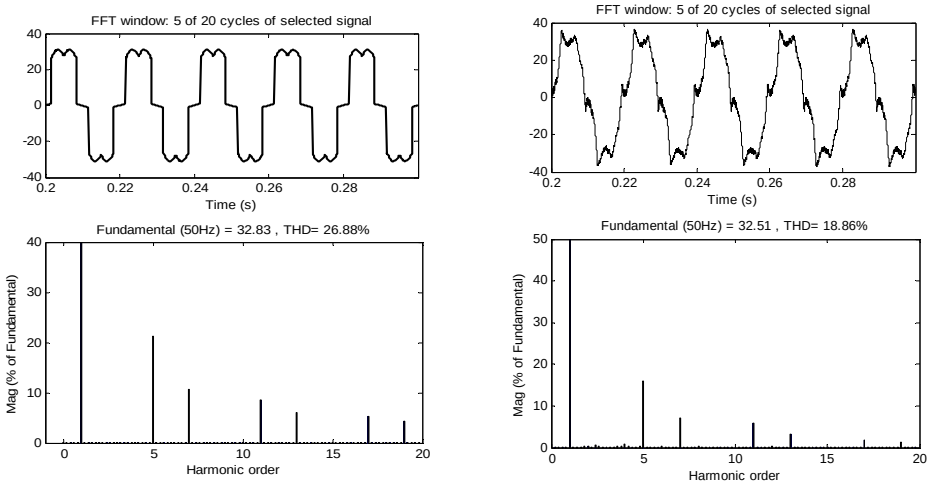


Fig. 8 Performance with DSTATCOM turned on at 0.06 secs Phase 'a' with a nonlinear load for source voltage and current, load current ,compensator current, DC link voltage (Rotating reference frame PI controller)



(a) (b)

Fig 9 (a-b) Frequency spectrum of source current for a nonlinear load before and after compensation (Rotating reference frame PI controller)

HYSTERESIS CURRENT CONTROLLER (NONLINEAR)

The DSTATCOM Controller with hysteresis current controller is shown in the Fig.10. The current controller is based on a nonlinear feedback loop with two level hysteresis comparators. It decides the switching states for the devices of the PWM converter.

The switching are obtained as:

If $i_{sa}>(i_{sa}*+h)$, upper switch of inverter leg corresponding to phase 'a' is ON and the lower

switch is OFF.
If $i_{sa}<(i_{sa}^*+h)$, upper switch of inverter leg corresponding to phase 'a' is OFF and the lower switch is ON.

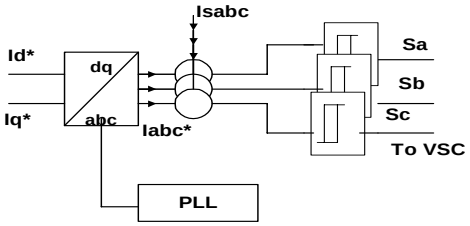


Fig. 10 DSTATCOM controller using hysteresis current controller

Similarly the switching states of the other phases is calculated and the three currents are regulated within the assigned tolerance band 'h' of their respective values. It can be observed that the converter switching largely depends on the load parameters, and source voltage variation. Reduction in the height of the assigned tolerance band improves the current harmonic spectrum but increases the switching frequency. Therefore in order to improve the harmonic spectrum a compromise is made between the switching frequency and the total harmonic distortion. Fig.11 shows the DSTATCOM performance with a hysteresis current controller. The waveforms shown are scaled source voltage and source current ($v_{sa,}$ i_{sa}) confirming unity power factor operation of a DSTATCOM, load current (i_{la}), compensator current (i_{ca}), and the dc link voltage (v_{dc}). The DSTATCOM is turned on at 0.06secs. There is no overshoot in source current as soon as the DSTATCOM is turned on. This is because the capacitor gets charged to about 540V before the pulses are given to the VSC at 0.06secs. The performance during transient conditions is shown by reducing the load at 0.15 secs. Fig.12 shows the frequency spectrum of the source current in steady state after compensation. After compensation the THD of the source current is 0.84%.

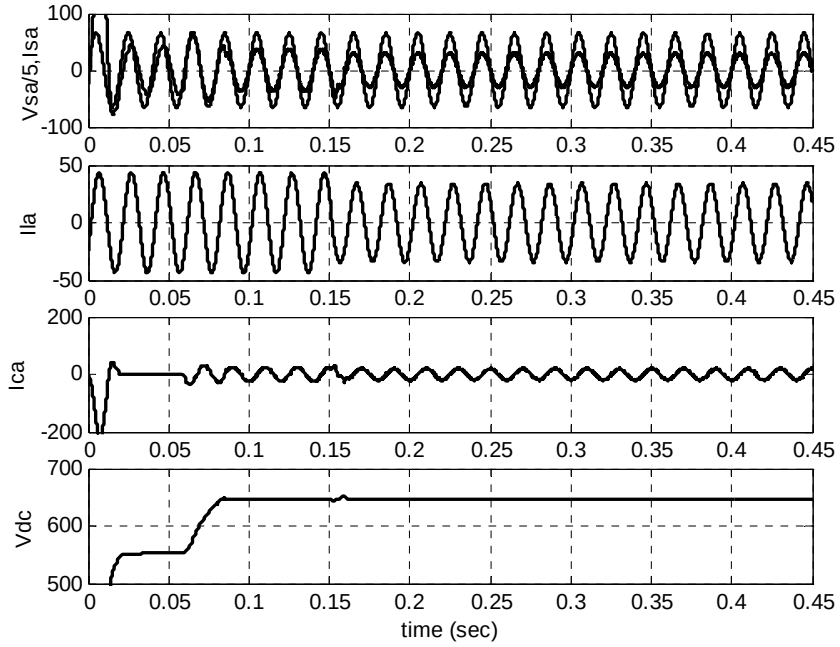


Fig. 11 Performance with DSTATCOM turned on at 0.06 secs Phase 'a' source voltage and current , load current , compensator current , DC link voltage (Hysteresis current controller)

When observing the DSTATCOM performance for a nonlinear load in Fig.13 using hysteresis current controller and keeping the system parameters same, the THD reduces from 26.88% to 2.21% only which is well within the IEEE-519 limit.Fig.14(a-b) shows the frequency spectrum of the source current before and after compensation. The dc loop proportional and integral gains are 45 and 0.8 respectively. The hysteresis band is of 0.5 amps.

On incorporating a hysteresis current controller (HCC), simplicity, lack of tracking errors, robustness are the inherent advantages. Moreover the controller can also be used directly on the dq components if required for independent band selection. The disadvantage of this controller is that the inverter switching depends largely on the load parameters.

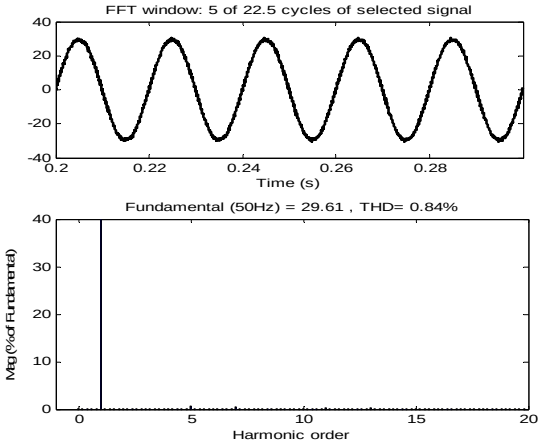


Fig 12 Frequency spectrum of source current (Hysteresis Current Controller)

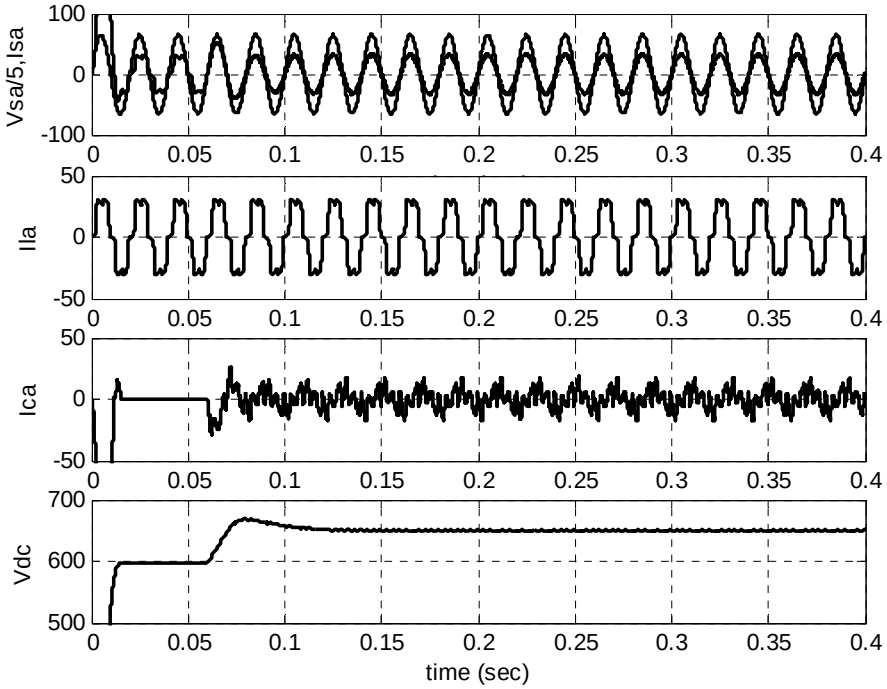
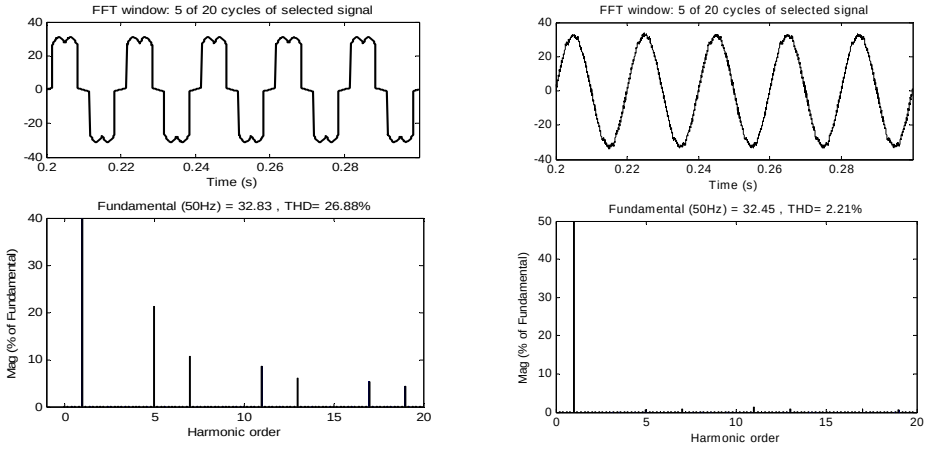


Fig. 13 Performance with DSTATCOM turned on at 0.06 secs Phase 'a'with a nonlinear load for source voltage and current , load current , compensator current , DC link voltage (Hysteresis current controller)



(a) (b)

Fig 14 (a-b) Frequency spectrum of source current with a nonlinear load before and after compensation (Hysteresis current controller)

7. CONCLUSION

The paper describes the performance of DSTATCOM controller under both rotating reference frame PI current controller and hysteresis current controller, with their relative merits and demerits for a linearly variable load and a nonlinear load. When pulse width modulation using carrier technique in rotating reference frame PI controller is implemented, the fixed switching of the VSC results in an overshoot of approx. 2.5 times more as compared to hysterisis current controller. Moreover the settling time of the dc link voltage using rotating reference frame controller is 70msecs and when using a hysteresis current controller is 25 msecs. In case of nonlinear load the THD in fixed switching frame is much higher than in case of variable switching frame. The comparison of both the current regulation methods is summarized in Table1. Due to better current tracking by a Hysteresis Current Controller, a HCC based DSTATCOM in SRF frame proves to be a viable solution for load compensation at the distribution level.

Table 1

Current Controller	Overshoot in source current	Settling Time of dc link voltage	%THD	
			Linear Load	Nonlinear
Rotating reference frame PI Controller	2.5 times	70msecs	3.11%	18.86%
Hysteresis Current Controller	No overshoot	25msecs	0.84%	2.21%

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Appendix

System Parameters

Supply Voltage (Vs)	400V (L-L),50 Hz
Source impedance	Ls=5e-3H,Rs=0.1ohms
Filter Impedance	Lc=5.5e-3H,Rc=0.2ohms
DC Capacitance (Cdc)	3000μF
DC Link Voltage (Vdc)	650V
Load 1(reduced by 25% at 0.15secs.) Load 2	22KVA at 0.83 lagging Nonlinear load Resistive 15 ohms
DSTATCOM turned on at 0.06secs.	