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Development of Digital Hysteresis Current Control with PLL Loop Gain Compensation Strategy for PWM Inverters with Constant Switching Frequency

Hysteresis current control is one of the simplest techniques used to control the magnitude and phase angle of motor current for motor drives systems. However, this technique presents several disadvantages such as operation at variable switching frequency which can reveal problems of filtering, interference between the phases in the case of the three-phase systems with insulated neutral connection or delta connection, and irregularity of the modulation pulses which especially causes an acoustic noise on the level of the machine for the high power drive. In this paper, a new technique is proposed for a variable-hysteresis-band controller based on dead beat control applied to three phase voltage source PWM inverters feeding AC motors. Its main aim is firstly ensure a constant switching frequency and secondly the synchronization of modulation pulses using the phase-locked-loop with loop gain compensation in order to ensure a better stability. The behavior of the proposed technique is verified by simulation.

Keywords- Digital Adaptive Hysteresis Current Control, Switching Frequency, Stability, Phase Locked Loop, Voltage Source Inverter

1. INTRODUCTION

In most applications of power electronics such as direct torque control (DTC), direct power control (DPC), power factor correction (PFC) and active power filters (APF)…etc. The hysteresis current control techniques have been receiving increased attention, especially for high speed electrical drives to provide a PWM signal control of the switches converter's, due to a several advantages such as its ease of implementation, fast current control response, and inherent peak current limiting capability [1].

To date, many researches have been reported in the literature with particular interest focused on fixed band hysteresis control for DC-AC converters [2-4]. However, a current control by conventional hysteresis with fixed band has many inherent disadvantages such as variable switching frequency, consequently a large amount contents harmonic distortion in the load current, which affect the passive filter and hamper its proper design, interference between the phases in the case of the three-phase systems with insulated neutral connection or delta connexion, resulting in irregular operation, and the irregularity of modulation pulses which causes a torque ripples in machine that result in speed oscillation, mechanical vibration and acoustic noise. Thus, these problems reduce the drive performances.

To overcome these disadvantages, recently, many authors have been interested to develop some algorithms to improve the characteristics of the hysteresis control technique [5, 6]. In this paper and in the same way, a novel technique is developed for three phase voltage source inverter feeding AC motors. The main objective of this technique is to modify in adaptive way the hysteresis-band independently on load conditions, in order to ensure a constant switching frequency, this Reasoning based on first order dead-beat control, and to ensure a synchronization of modulation pulses, the phase locked loop (PLL)

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is added. The conventional PLL presents a gain loop depending of the normalized voltage which create stability problem during transient state. In order to ensure a better stability of the system, a PLL loop gain compensation is introduced. For the three phase systems with insulated neutral, the application of this novel technique requires the decoupling of the real current error in order to avoid interference phenomena between the phases.

In this study, the mathematical development of this proposed technique followed by a stability analysis is described, and its performances are confirmed through simulation results using MATLAB/SIMULINK.

2. PRINCIPLE OF OPERATION

The operation of a three-phase voltage-source inverter (VSI) feeding an AC motor is described with reference to Fig.1 [7, 8], where the motor load is represented by a symmetrical approximated equivalent scheme including R.L impedances and back-EMF's e.

Where:

$$R = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix},\ L = \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix},\ e = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}$$

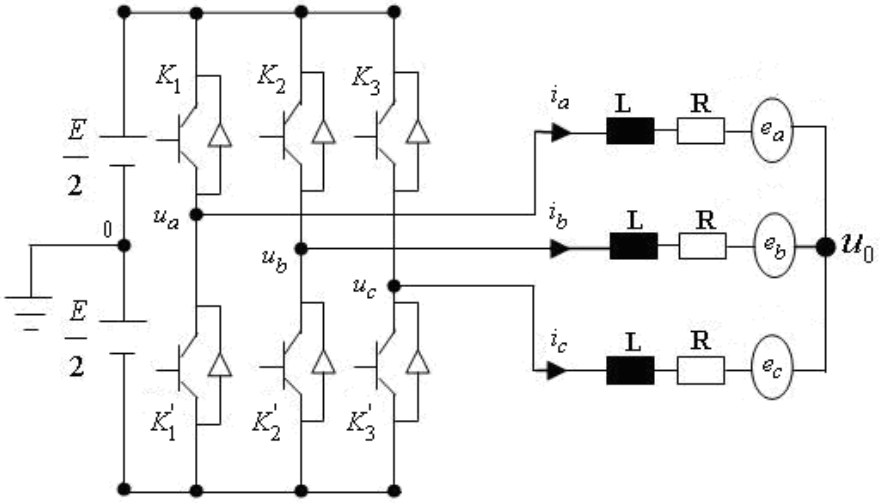


Figure 1: Three phase inverter with insulated neutral motor load.

The load equations are:

$$u = L.\frac{di}{dt} + R.i + e + u_{0\,\mathrm{I}} \tag{1}$$

$$u_0 = \frac{(u_a + u_b + u_c)}{3} \tag{2}$$

Where u and i are vectors of the inverter output voltages and currents, respectively, I is unity vector, and u_0 is the load midpoint voltage. All voltages are referred to the supply midpoint.

The vectors u, i and I are defined as:

$$u = \left[u_a \; u_b \; u_c\right]^T, \; i = \left[i_a \; i_b \; i_c\right]^T, \; \mathrm{I} = \left[1\,1\,1\right]^T.$$

If i^* are load reference currents. Consequently, the phase reference voltages may be defined as:

$$u^* = L.\frac{di^*}{dt} + R.i^* + e \tag{3}$$

Where:

$$u^* = \left[u_a^* \; u_b^* \; u_c^*\right]^T, \; i^* = \left[i_a^* \; i_b^* \; i_c^*\right]^T$$

u^* are the voltages that should be applied to obtain currents i^*.

And the instantaneous current errors are the deviations between the actual currents i and the reference currents i^* as:

$$\delta = i - i^* \tag{4}$$

From (1), (3) and (4), we obtain:

$$L\frac{d\delta}{dt} + R\delta = u - u^* - u_0\,\mathrm{I} \tag{5}$$

Equation (5) shows that, due to the action of load midpoint voltage u_0, each phase current error is affected by the commutations in the other phases. This interference [5, 7], causes severe irregularities in the ordinary hysteresis operation. By introducing a decoupling term δ'' such as:

$$L\frac{d\delta''}{dt} + R\delta'' = -u_0\,\mathrm{I} \tag{6}$$

An interference-free modulation can be obtained if the hysteresis control is performed on the decoupled error terms.

$$\delta' = \delta - \delta'' \tag{7}$$

Instead of total errors δ. Indeed, from (1) to (7), it results:

$$L\frac{d\delta'}{dt} + R\delta' = u - u^* \tag{8}$$

Which shows that terms δ' are independent from u_0.

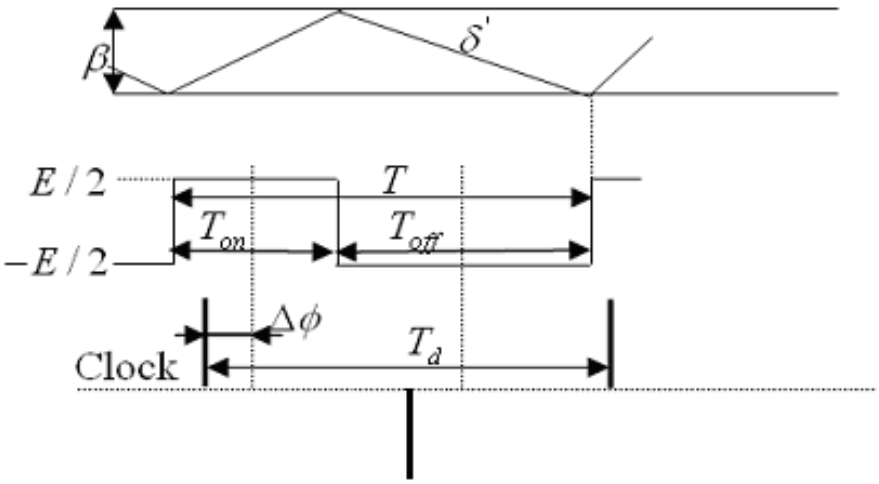


Figure 2: Upper: Hysteresis-band and decoupled current error, Middle: output voltage, lower: clock of synchronization.

Once decoupled, each phase control can be performed independently. The instantaneous phase voltage has a rectangular waveshape of amplitude $\pm E/2$, with duration T_{on} of the positive pulse and T_{off} of the negative one, for a total period T (figure 2). Usually, the effects of load resistance R can be neglected, and the term $u-u^*$ can be considered constant during a modulation period; from (8), it results that current error has a triangular behavior, as shown in Figure 2. In these assumptions, from (8), it also results that the average of the phase voltage u over T is equal to u^*. By defining the normalized phase voltage

$$u_n = u^*/(E/2) \tag{9}$$

And with reference to Figure 2, it can be derived:

$$T = \frac{4.L.\beta}{E(1-u_n^2)} \tag{10}$$

$$T_{on} = T\frac{1+u_n}{2}, T_{off} = T\frac{1-u_n}{2} \tag{11}$$

Equation (10) shows that, if u_n is variable and β is constant, a variable modulation frequency is produced.

3. DIGITAL ADAPTIVE HYSTERESIS CURRENT CONTROL

A. Constant switching Frequency

To obtain a constant switching frequency $(1/T_d)$, the hysteresis-band β has to be modified dynamically, according to equation (12) [7, 8]:

$$\beta = \frac{E\,T_d}{4.L}(1-u_n^2) \tag{12}$$

The controller maintains its analog structure, but an adaptive bandwidth digital control is added which ensures constant switching frequency. Figure 3 shows the adaptation of the hysteresis-band for two successive modulation periods.

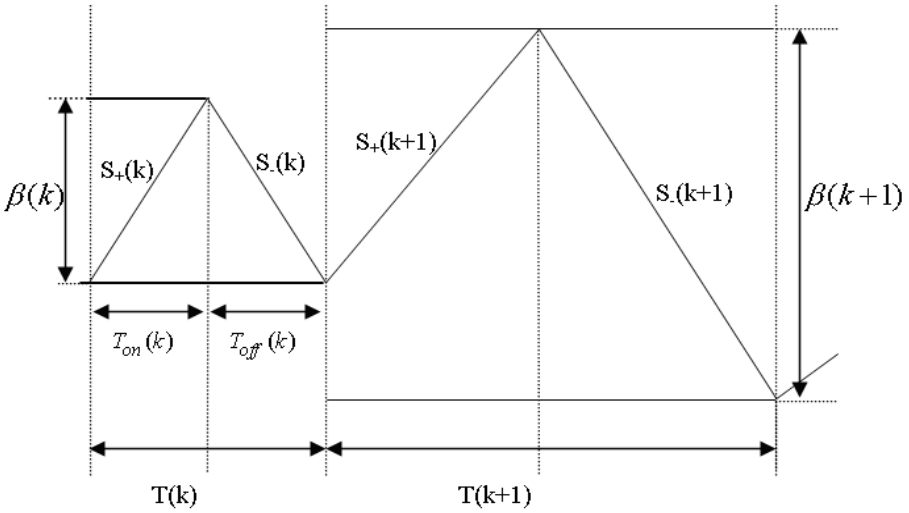


Figure 3: Bandwidth control algorithm.

From the figure 3, we deduce the following equations:

$$\forall k: \begin{cases} s_+.T_{on} = s_-.T_{off} = \beta \\ T_{on} + T_{off} = T \end{cases} \tag{13}$$

For a switching period corresponding to k , we have:

$$T(k) = \frac{\beta(k)}{s_+(k)} + \frac{\beta(k)}{s_-(k)} = \beta(k).\frac{s_+(k)+s_-(k)}{s_+(k).s_-(k)} \tag{14}$$

For a switching period corresponding to k+1, the equation (14) is written:

$$T(k+1) = \beta(k+1).\frac{s_+(k+1)+s_-(k+1)}{s_+(k+1).s_-(k+1)} \tag{15}$$

For two successive periods, we have the following simplifying assumption:

$$\begin{aligned} s_+(k) &= s_+(k+1) \\ s_-(k) &= s_-(k+1) \end{aligned} \tag{16}$$

From (14), (15) and (16), we can get:

$$T(k+1) = \beta(k+1).\frac{T(k)}{\beta(k)} \tag{17}$$

From (17), it is possible to derive the control equation:

$$\beta(k+1) = \beta(k).\frac{T_d}{T(k)} \tag{18}$$

Where $T_d = T(k+1)$ is the desired switching period.

It is worth noting that this reasoning leads to an algorithm which is equivalent to a first order dead-beat control of the switching period, habitually a low-pass filter is added to output of this algorithm to ensure the stability of its loop. The control algorithm is very simple; unfortunately, the switching pulses are not phase-controlled. This means that the allocation inside the modulation period of the switching pulses is random. To avoid this problem, the solution is equivalent to the implementation of a digital phase locked loop (PLL).

B. Synchronization of modulation Pulses

When locked to a suitable clock signal, the PLL not only ensures constant modulation frequency, but also minimizes the phase displacement between the output voltage pulses and the clock itself as shown in figure 4, with an accuracy limited only by the control loop gain. This feature is of particular importance for three-phase insulated neutral system, where the "centered pulse" condition results in optimal reduction of the current ripple [5, 9]. Thus, we have two cases to study:

- *Case 1: non-compensated PLL loop gain*

In controlling the hysteresis modulation, the ability of the PLL to limit the phase displacement is restricted to slow variations of u_n. This because its bandwidth is limited by the wide variations of the loop gain in dependence of u_n.

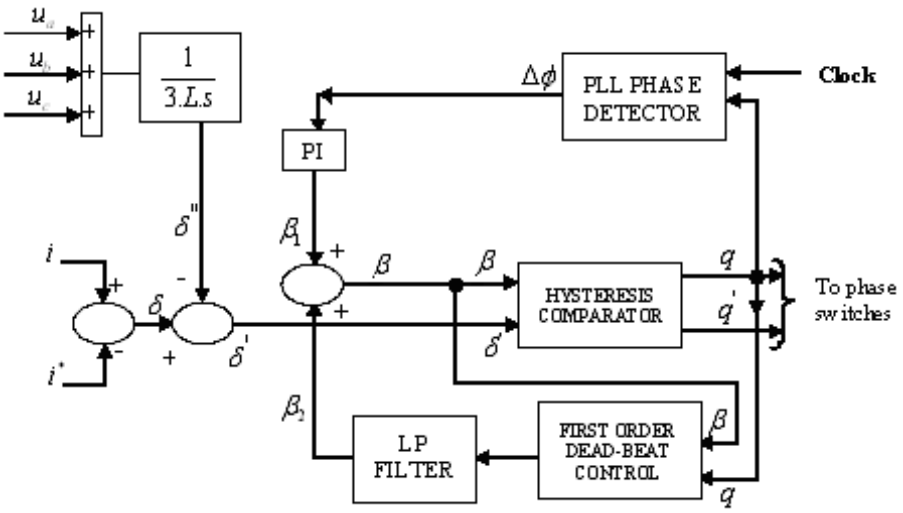


Figure 4: Digital hysteresis current control with non-compensated PLL loop gain.

From the figure 4 and with reference to PLL loop as shown in the upper part, we deduce the following equations:

The phase detector transfer function can be modeled as an integrator as:

$$PHD = \frac{d\Delta\phi}{df} = \frac{2\pi}{s} \tag{19}$$

The filter has a proportional-integral characteristic to ensure a zero steady-state phase error:

$$PI = \frac{d\beta_1}{d\Delta\phi} = k_p.\frac{1+sT_z}{sT_z} \tag{20}$$

Being k_p the high frequency gain and T_z the zero of the filter.

From (10) and (12), the differential gain H_c of the Hysteresis comparator turns out to be:

$$H_c = \frac{df}{d\beta} = -\frac{E}{4.L.\beta^2}.(1-u_n^2) = -\frac{f_d}{\beta} \tag{21}$$

Were $f = 1/T$ is the actual frequency and in the last term it is assumed that the system is locked at $f_d = 1/T_d$.

The closed loop gain GP in lock conditions is obtained from (12), (19), (20) and (21):

$$GP = -\frac{8\pi k_p L}{E}.\frac{f_d^2}{[1-u_n^2]}.\frac{1+sT_z}{s^2T_z} = -2\pi k_p \frac{1+sT_z}{s^2T_z}\frac{f_d}{\beta} \tag{22}$$

The equation (22) shows that GP varies with the normalized voltage u_n, becoming very large as its absolute value approaches unity. On the contrary, the gain decreases for small values of u_n near zero. This behavior is shown in figure 5, where asymptotic Bode plots of GP are reported, for $u_n = 0$ and $u_n = 0.8$.

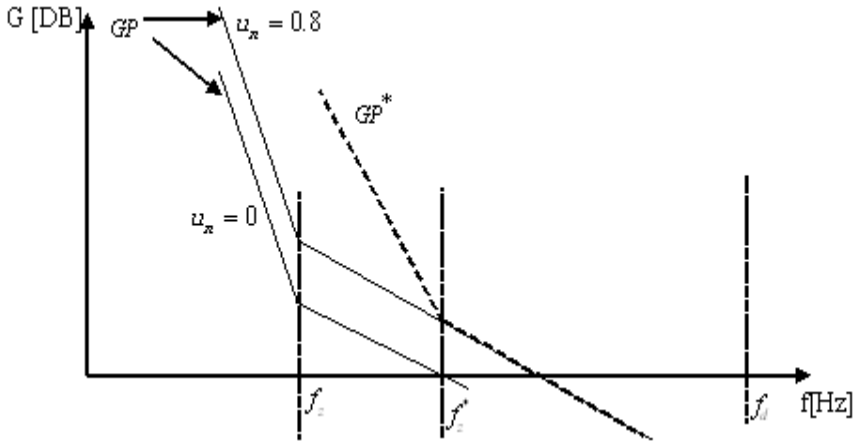


Figure 5: Bode diagrams.

The large variations of GP may result in instability, especially if unity crossing approaches the switching frequency f_d. This instability affects the switching regularity and

the current error. The instability occurs near to the maximum positive and to the minimum negative values of u^*, where β is minimum, according to (12).

To avoid instability, it is customary to set a lower limit to the band β. This corresponds to an upper limit for u_n, beyond which the PLL loses the lock and the modulation frequency slows down.

From the diagram of figure 5, it can be seen that, in order to ensure good stability margins and to keep the unity-gain crossing well below the switching frequency, the PLL bandwidth is reduced appreciably at low values of u_n.

- *Case 2: PLL loop gain compensation*

To improve the PLL characteristics, a solution is suggested by the expression of GP given by the last term of (22). A constant gain, independent of β and thus of u_n, can be obtained if a multiplicative factor proportional to β is introduced in the loop as shown in figure 6.

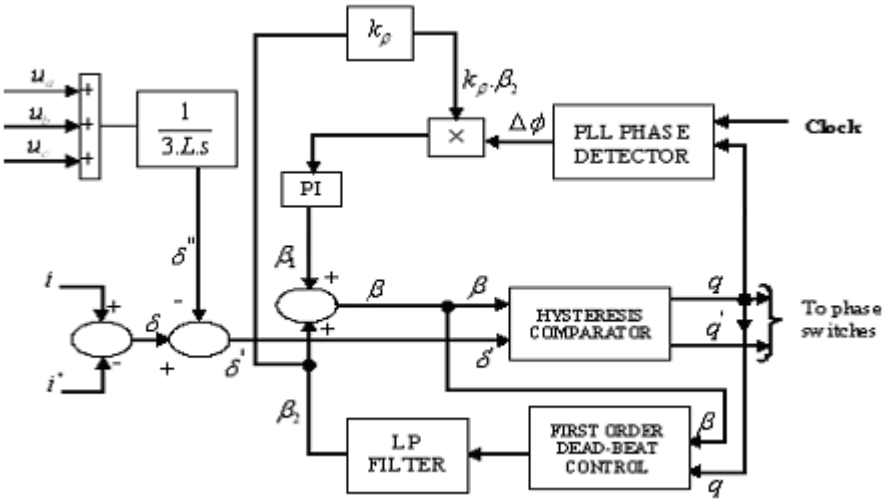


Figure 6: Digital hysteresis current control with compensated PLL loop gain.

The expression (22) of the loop gain becomes:

$$GP^* = -2\pi k_p . \frac{1+sT_z}{s^2 T_z} . f_d . K_\beta \qquad (23)$$

Where k_β is a proper constant. As a result, GP^* is independent of u_n and β, this behavior is shown in figure 5. In practice, if the absolute value u_n approaches unity, particularly higher gain is obtained which does not depend on u_n. Thus, to ensure a correct operation, u_n must be limited by a limit strictly lower from 1 ($u_n < 1$).

Finally, with reference to figure 6, it can be derived:

$$\beta = \beta_1 + \beta_2 \tag{24}$$

$$\beta_1 = K_p . \frac{1 + sT_z}{sT_z} . \Delta\phi \tag{25}$$

$$\beta_2 = \frac{f}{f_d} \beta \tag{26}$$

The equation (26) shows the first order Dead-Beat control with correction by PLL with compensated loop gain, which allows to obtain a constant switching frequency and a synchronization of modulation pulses of inverter with a better stability.

4. SIMULATION RESULTS

In this simulation, we used the parameters which are shown in table 1.

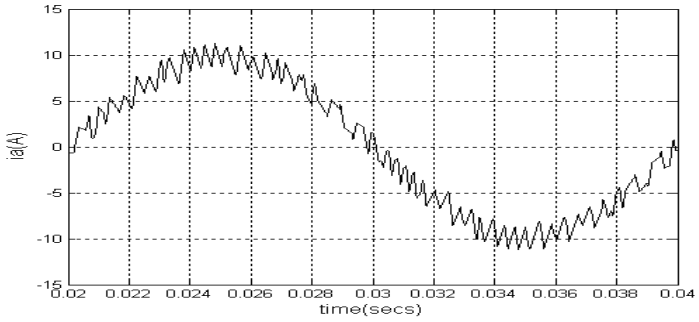
Table 1: Design specifications and circuit parameters

Desired Switching Frequency	$f_d = 5KHz$
Fundamental Frequency	$50Hz$
Inverter DC Voltage	$E = 500V$
Load resistance	$R = 1\Omega$
Load inductance	$L = 10mH$
The magnitude of EMF's	$95V$
The magnitude of reference currents	10 A
PLL parameters	$f_z = 500Hz \;\; k_p = 0.5$
The constant	$k_\beta = 0.3$

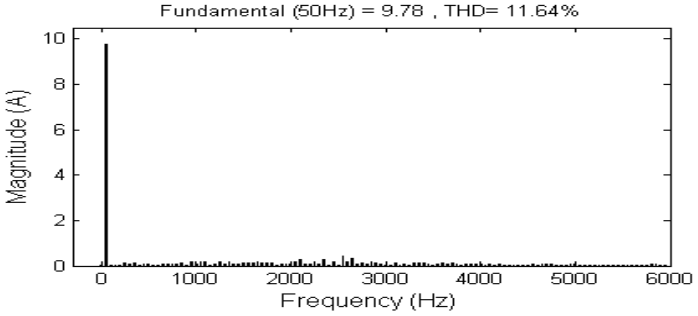
To verify the performances of the proposed technique compared to the conventional fixed band hysteresis current control, the simulation results will be shown as follows.

Figure 7 shows the a-phase current waveform, its harmonic spectrum and PWM switching frequency for the conventional fixed band hysteresis current control with interference phenomena (the current error is not decoupled), where the hysteresis-band is fixed to 2.5 A. The phase current has a high current ripple, its harmonic components are widely distributed with Total Harmonics Distortion (THD) is equal to 11.64%, and thus the switching frequency varies widely and randomly.

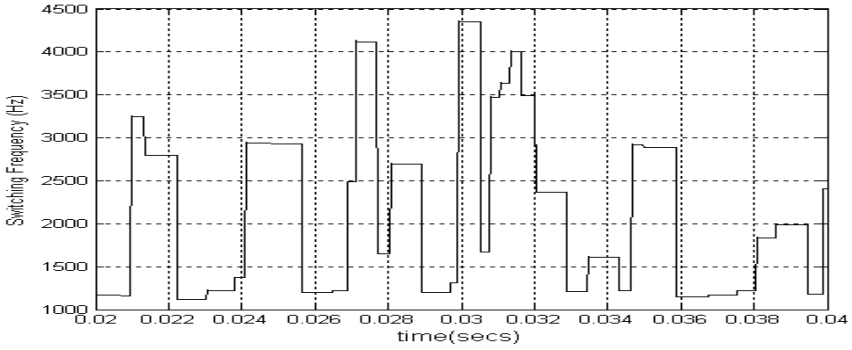
Figure 8 shows the a-phase current waveform, its harmonic spectrum, PWM switching frequency and phase error $\Delta\phi$ between the switching signal and the extern clock for digital hysteresis current control with non-compensated PLL loop gain. In this case, the phase current waveform has almost negligible current ripple, its harmonic components are negligible with THD is weak equal to 1.05%, the switching frequency is always almost held in 5 KHz, and the phase error varies around zero, between almost 10° and -10°.



(a). Phase current.

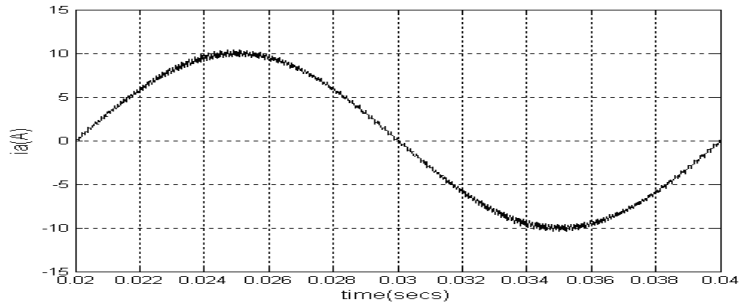


(b). Spectrum harmonic of phase current.

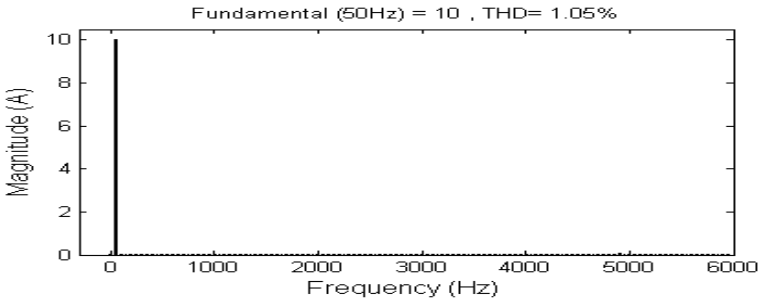


(c). PWM inverter switching frequency.

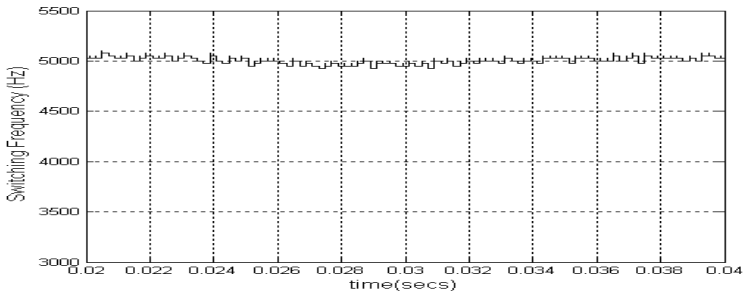
Figure 7: Simulation results for conventional hysteresis-band controller with interference phenomena.



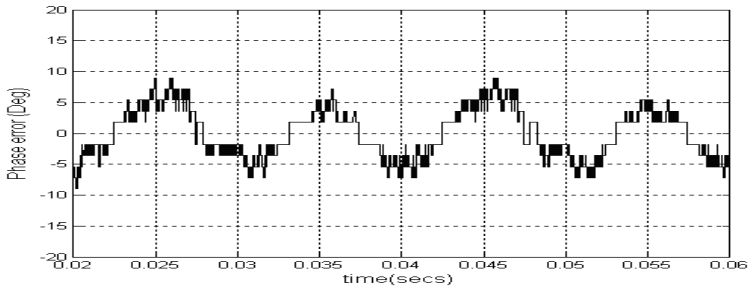
(a). Phase current.



(b). Spectrum harmonic of phase current.

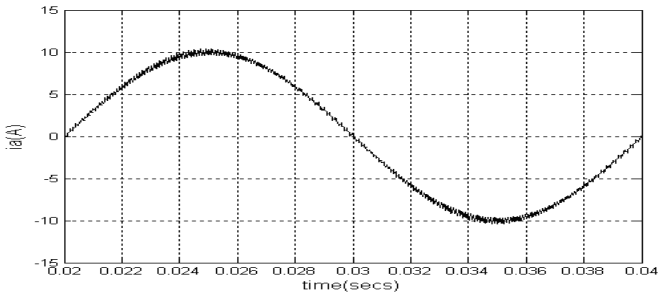


(c). PWM inverter switching frequency.

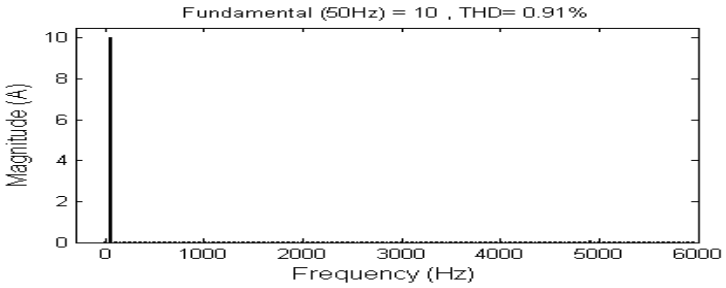


(d). Phase error.

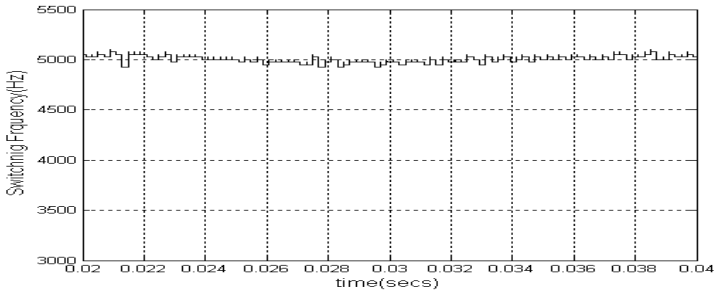
Figure 8: Simulation results for digital hysteresis current control with non-compensated PLL loop gain.



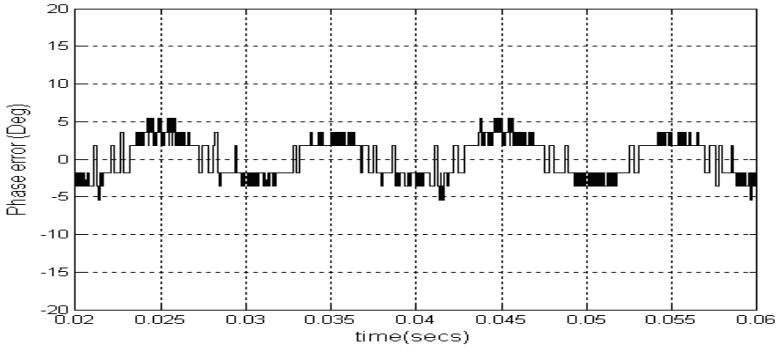
(a). Phase current.



(b). Spectrum harmonic of phase current.



(c). PWM inverter switching frequency.



(d). Phase error.

Figure 9: Simulation results for digital hysteresis current control with compensated PLL loop gain.

The a-phase current waveform, its harmonic spectrum, PWM switching frequency and the phase error waveform for digital hysteresis current control with compensated PLL loop gain are shown in Figure 9. In this case, the phase current waveform has almost negligible current ripple, its harmonic components are negligible with THD is very weak equal to 0.91%, , the switching frequency is always almost held in 5 KHz, and the phase error varies around zero, between almost 5° and -5°. We observe that there is an important improvement of the load current quality for the digital hysteresis technique with compensated PLL loop gain compared to the digital hysteresis technique with non-compensated PLL loop gain, this improvement is explained by the reduction of the THD from 1.05% to 0.91% and thus of the maximum phase error from 10° to 5°.

Figure 10 shows the variation of the maximum phase error $\Delta\phi$ as a function of normalized voltage u_n for compensated and non-compensated PLL loop gain. For the case of non-compensated PLL loop gain, the phase error undergoes a great variation when the normalized voltage varies, especially around of unity ($u_n > 0.8$). For the case of compensated PLL loop gain, the variation of the normalized voltage does not have a great effect on the phase error. Thus the digital hysteresis technique with compensated PLL loop gain shows a better stability compared to the digital hysteresis technique with non-compensated PLL loop gain. But for the two cases, to ensure a correct operation of the system, the normalized voltage must be strictly lower of unity.

Figure 11 shows the variation of the THD of load current as a function of switching frequency for compensated and non-compensated PLL loop gain. It is noted that the PLL with gain compensation presents a better THD compared to the PLL with non-compensated gain, especially for the low switching frequency.

5. CONCLUSION

This paper has presented a digital adaptive hysteresis current control with PLL loop gain compensation which is shown to be particularly simple and effective in achieving both a constant switching frequency and the phase control of the inverter voltage pulses. This technique is characterized by a better stability; it allows also an improvement of the load current waveform in term of total harmonics distortion (THD). The performances of the proposed digital hysteresis current control are verified by simulation.

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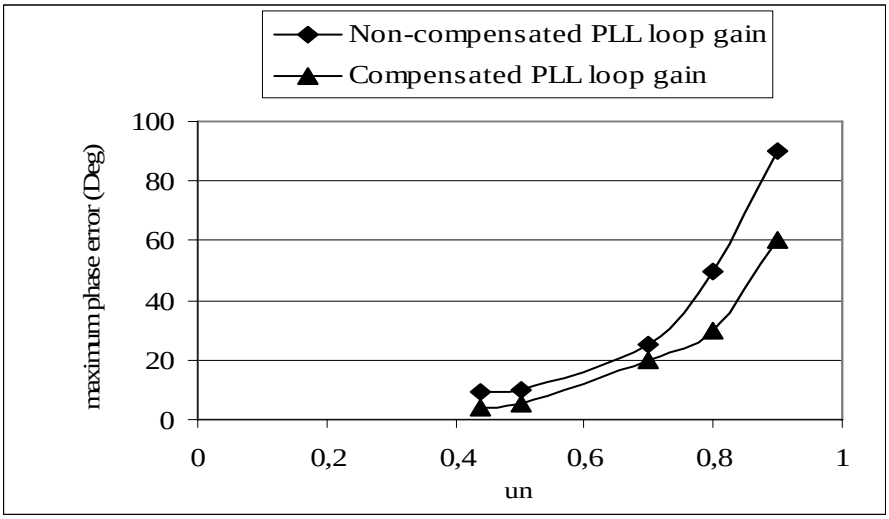

Figure 10: Maximum phase error as a function of normalized voltage for two cases: compensated and non-compensated PLL loop gain.

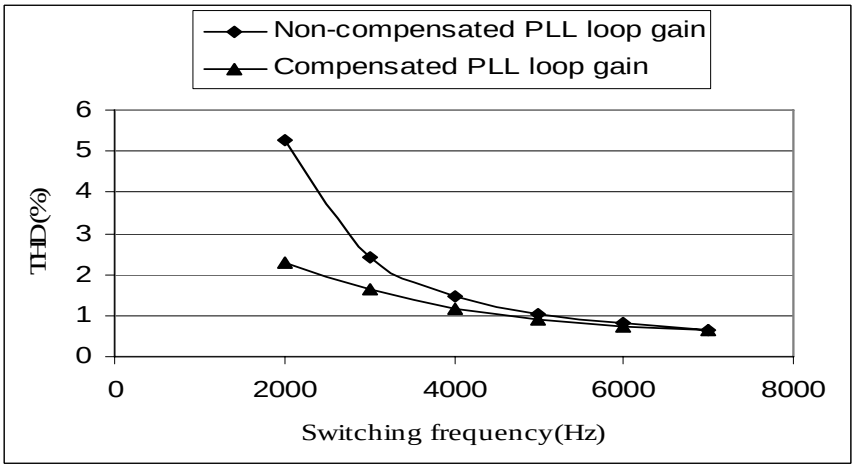

Figure 11: THD of load current as a function of switching frequency for two cases: compensated and non-compensated PLL loop gain.