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Regular paper

Single Stage ZVS PFC Circuits with Voltage Doubler

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To improve the efficiency of the circuit and to minimize the THD to the negligible level voltage doubler circuit is interleaved with the single stage ZVS PFC converter circuits. The voltage doubler circuit is used to obtain UPF with low THD and increased performance efficiency of the converter by imposing the control over the current. The voltage doubler is charged by the converter operation at both negative and positive cycle. The converter circuit without voltage doubler was used in low power rating applications. But with the voltage doubler circuits high power ratings applications are possible. In this circuit the reduced switching loss of 6.7% is obtained with the THD 2.95[12]. The improvised performance efficiency with the input condition of 529.65W/ 31.21 A is 93.28%.

Keywords: ZVS- Zero Voltage Switching- PFC -Power Factor Correction, THD- Total Harmonics Distortion

1. Introduction

The proposed design of the ZVS PFC Circuit with VD is illustrated in the Fig.1. In this circuit the voltage doubler is used to improvise the power factor of the circuit and to suppress the total harmonic distortion. The proposed design of the ZVS PFC Circuit with VD is illustrated in the Fig.1. In this circuit the voltage doubler is used to improvise the power factor of the circuit and to suppress the total harmonic distortion. [1]

The negligible THD totally overthrows the noise and fluctuations in the circuit by increasing the performance characteristics of the circuit with increased efficiency [3]. There are different switching schemes in this circuit which is discussed in detail in the following sections.

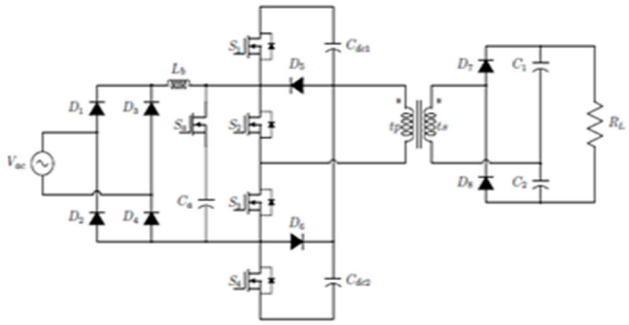

Fig.1: ZVS PFC Circuit With VD

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2 Modes of Operation

The converter with the voltage doubler circuit has seven operating modes. The detailed explanation of each mode is given in the following sections. [4]

This mode occurs in the interval of [t0-t1]. In this mode the switches S1 and S2 are in OFF state and the remaining switches S3, S4 and Sa are turned ON to establish a circulating inductive current path from the positive of the supply voltage through base inductor, Auxiliary components like switch and capacitor to the negative terminal of the supply voltage[3].

Mode 0:

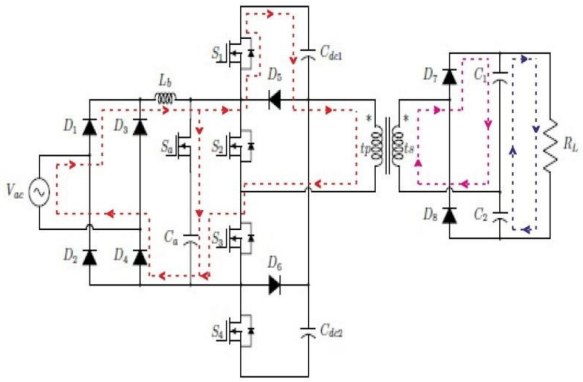

Fig.2. Mode 0

During this establishment the diode D1 is forward biased and transfers current in the primary winding[3]. Due to the mutual induction considerable amount of flux occur in the secondary winding causing the flow of current in the secondary side winding. This forward biases the diode D7 in the secondary side and causes charging of the response capacitor as shown in the Fig.2.

Mode 1:

In this mode the switching scheme happens in the interval [t0 - t1].

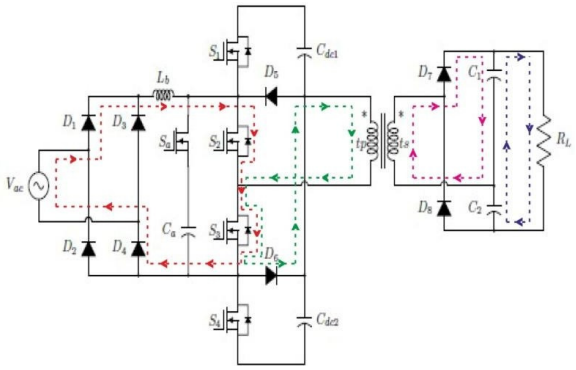

Fig.3. Mode 1

In this mode the switches S1 and S4 are in OFF state and the switches S2 , S3 and secondary switch Sa are in ON state [6]. The circulating current established in the previous mode remains same in this mode. During this mode the resistive load across the primary winding unit discharges the capacitive current from the capacitor C01 through capacitor C02. The operation of the Mode 1 is shown in the Fig.3.

Mode 2:

This mode happens in the interval of [t1-t2]. In this mode only the auxiliary switch Sa is kept in ON state while the other switches are in OFF state. In this mode the auxiliary switch establishes a circular current from the positive terminal of the supply voltage through the base inductor through the auxiliary components to the negative terminal of the supply voltage as shown in the Fig.4. During this phase the capacitor Co1 discharges through the resistive load and charges the capacitor Co2.

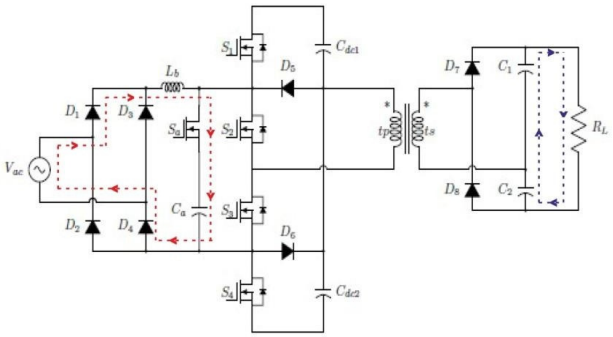

Fig.4. Mode 2

Mode 3:

This mode occurs in the interval [t2-t3]. The switching conditions in this mode is inverse that of the mode0. Here the switches S1 and S2 are turned OFF and the switches S3, S4 and Sa are turned ON[5] .This forms a circulatory path for the current in the primary winding and the charging of the primary capacitors happen. Due to the induced mutual induction, a certain current path is also established in the secondary side winding. During this transition the diode D8 is forward biased as shown in Fig.5.

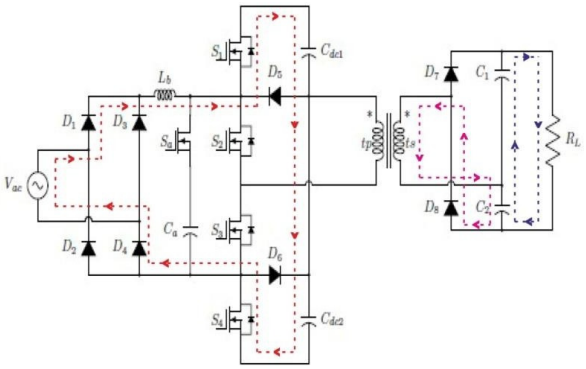

Fig.5. Mode 3

Mode 4:

This mode happens in the interval [t3-t4]. In this mode the switches S1, S2 and Sa are turned ON and the switches S3 and S4 are in OFF state[6]. The auxiliary switch initiates the current flow from the positive terminal of the supply voltage to the negative terminal of the power supply through the auxiliary components like Base inductor, Auxiliary switch and capacitor. Other operations are retained from the previous mode as shown in Fig.6.

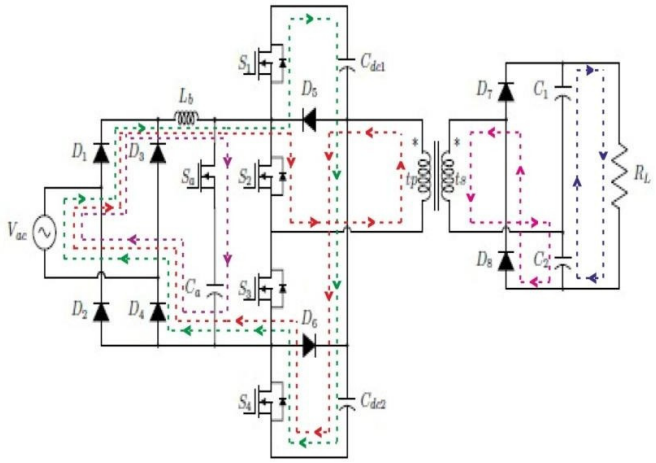

Fig.6. Mode4

Mode 5:

This mode operates in the interval of [t4-t5]. In this mode the switches S2,S3,and Sa are turned ON and the switches S1 and S4 are turned OFF[10]. As the outer switches are turned OFF the discharging of the capacitors Cdc2 and Cdc1 happens. Due to the center switches current flow is set in the primary winding which is transferred to the secondary winding due to the mutual inductance as illustrated in Fig.7.

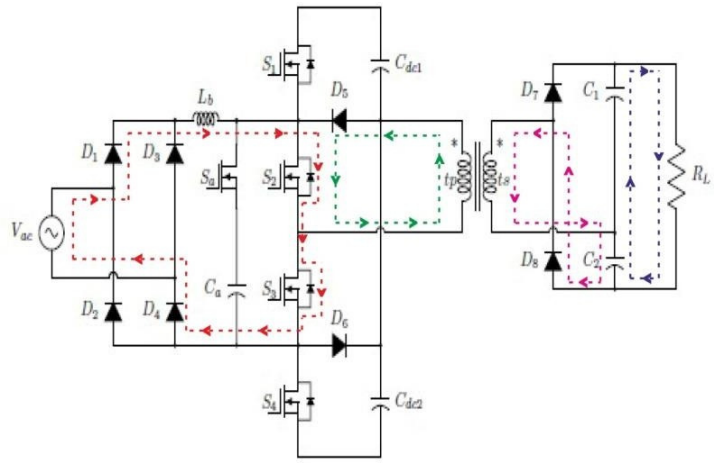

Fig.7. Mode 5

Mode 6:

This mode occurs in the interval [t5-t6]. In this mode all the switches except auxiliary switch is in OFF state. Only Sa is turned ON. Due to Sa the inductive current transfer from the positive terminal of the power supply is done to the negative terminal of the power supply through the base inductor and auxiliary switch and capacitor[7]. The circulating path is set between the Capacitor Co1 and Co2 through RL as illustrated in Fig.8.

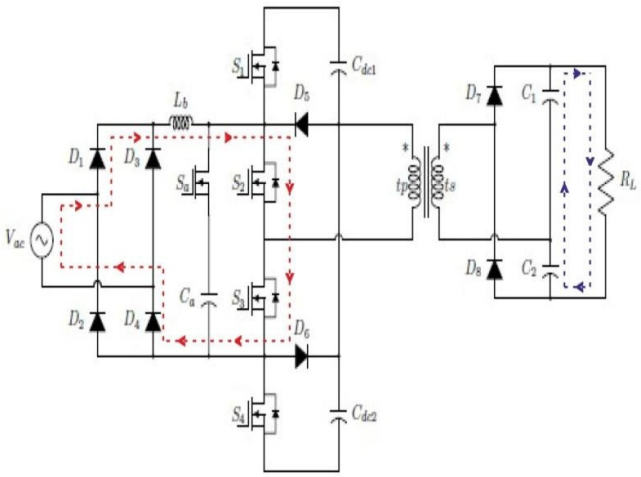

Fig.8. Mode6

Mode 7:

This is the last mode occurring in the interval [t6-t7][9]. In this mode the switches S3 and S4 are turned ON and the switches S1,S2 and Sa are turned OFF. Hence the discharging of the capacitors in the primary winding establish a circulatory path for the transmission of the capacitive current as shown in Fig.9. Due to the flux created by the mutual induction a circulatory current path is set at the secondary winding too.[12]

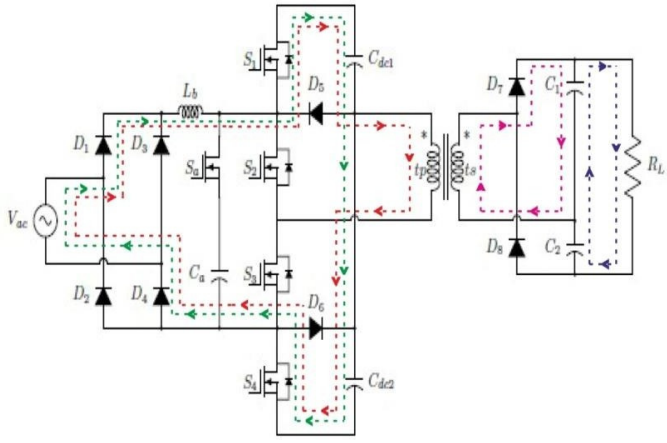

Fig.9. Mode 7

The switching scheme waveforms are illustrated in the following Fig 10

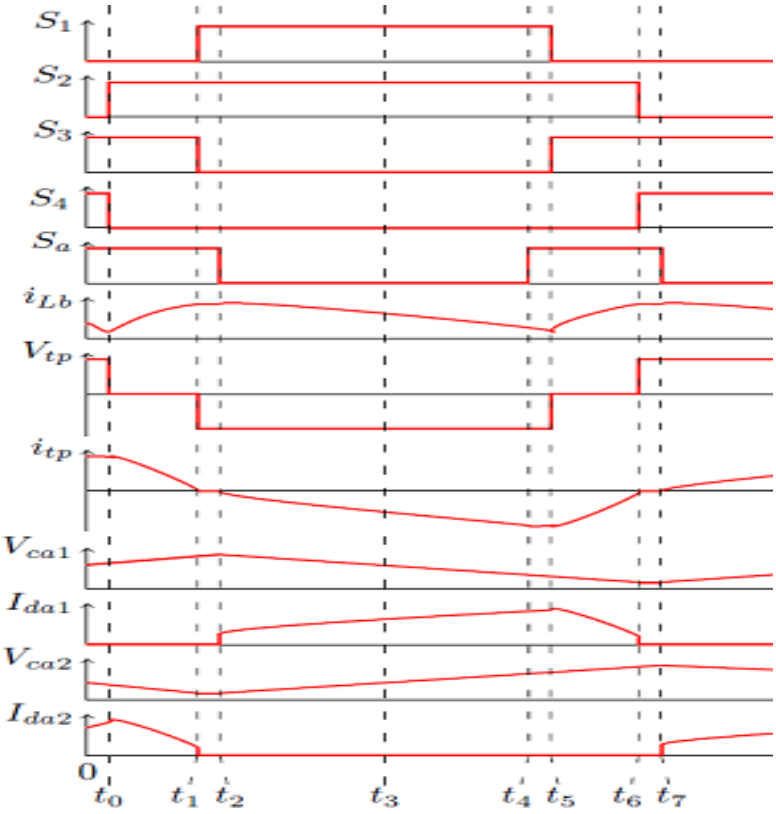

Fig.10. Switching Scheme Waveforms

3. Steady State Performance Analysis

The input voltage, current and power given to the proposed single stage ZVS PFC converter with voltage doubler unit is illustrated in the Fig.11. This converter is designed to produce the peak voltage of 33.94 V, output power of 500W with the load current of 31.21A

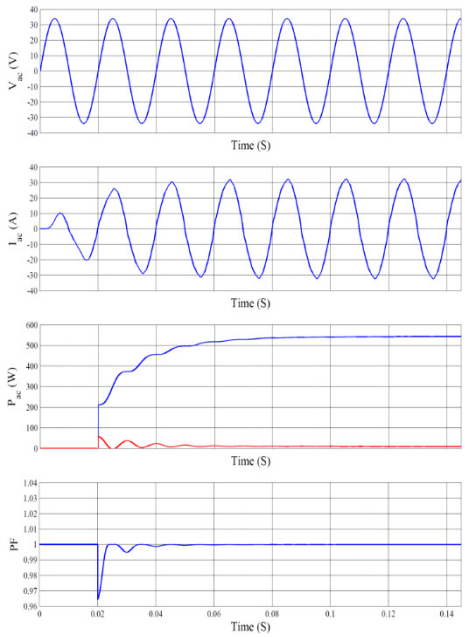

Fig.11. Waveforms of Input Parameters given To The Single Stage ZVS PFC Converter with voltage doubler unit

And the corresponding response waveforms of the obtained specifications according to the designed reference values are illustrated in the Fig.12

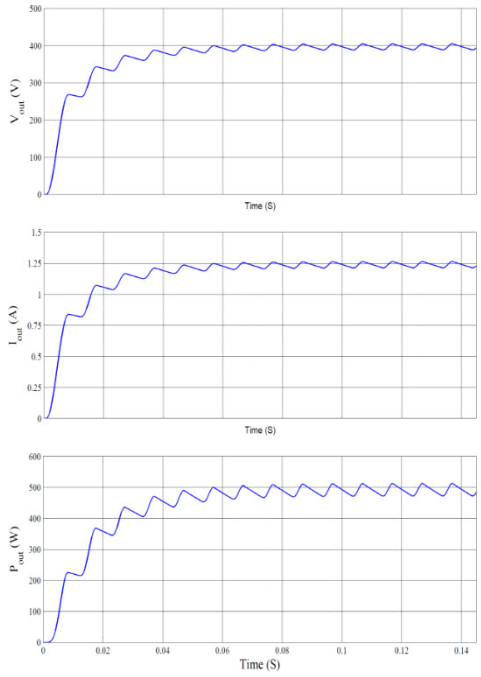

Fig.12. Waveforms Of The Obtained Specifications From The Single Stage ZVS PFC Converter with voltage doubler uni

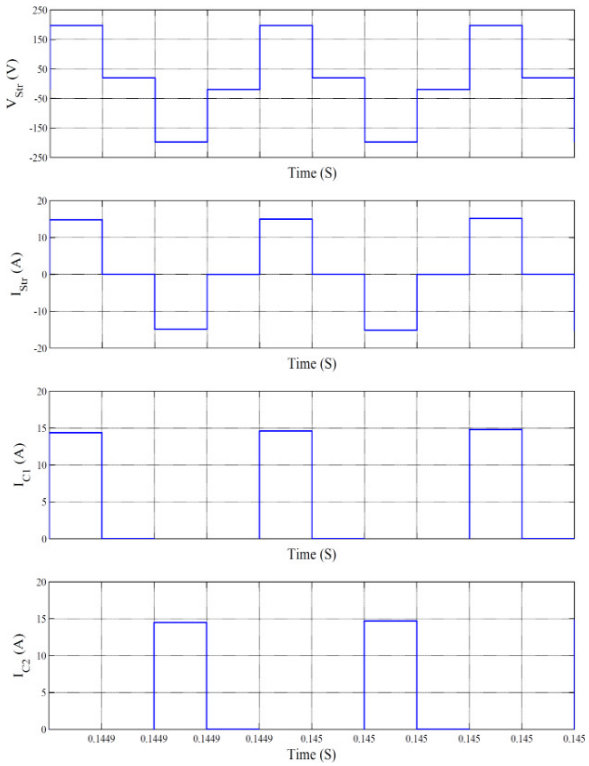

Fig.13. Internal waveforms of the voltage doubler

The internal waveforms of the single stage ZVS PFC with voltage doubler during the operation of the switching schemes are illustrated in the Fig.13.[12]

From the graphs it is evident that the efficiency of the circuit is increased by the use of the voltage doubler circuit[8]. The efficiency of the circuit is about 93.28% with the power factor 0.99995 reaching the unity. . Given the feed voltage of 24V resulting response output is 400V and the response current is 1.25A[7]. These response ratings produces high power of about 500W which makes it preferable for the high power applications.

These waveforms clearly illustrates the varying levels of the current and the voltage across the different circuit components of the feed and the response unit. It is also evident from the figures that the switching schemes of the converter circuit has significant impact over the current and the voltage across each circuit component[5]. The obtained

Power factor is in the range of 0.99995 which is increased by 0.000005 when compared to that of the previous module. Hence the HPF circuit which supports the high-power application was designed and simulated successfully [9]

By FFT analysis in the Figure 6.14 its clearly indicate that Total Harmonics Distortion 2.95% at a fundamental Frequency (50Hz) =8.25.

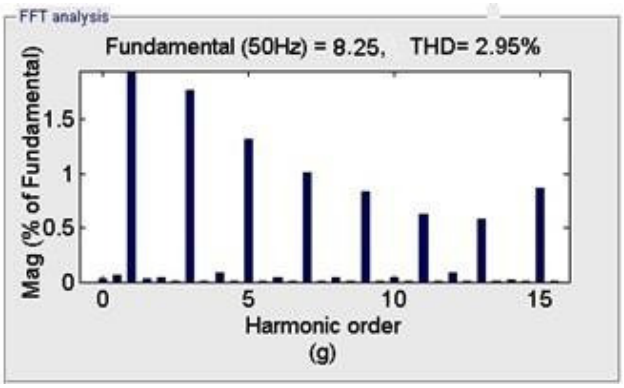

Fig.14. Harmonic spectra of the applied input current

3. Result and Discussion

The design of the ZVS PFC converter with the voltage doublers circuit was accomplished and the simulation was done in the MATLAB / Simulink software with the use of simpowersystem toolbox.[8] The analysis of the characteristics of the input and the response parameters were done with the help of the corresponding waveform diagrams and the efficiency and power rating of the design was estimated[11]. The power indices like THD, DPF and PF are measured to study about the quality of the obtained results. The parameters utilized in the simulation of the proposed converters are summarised in the Table.6.1.

Table.6.1. Specification of the single stage ZVS PFC with VD

PARAMETERS	VALUES
Supply voltage Vac in rms	24 V
Supply voltage Vac in peak	33.94V
Supply current Iac in rms	22.06 A
Supply current peak	31.21 A
Output voltage (Vout)	400V
Output currnet(Iout)	1.25 A
Output power (pout)	500W
Input power	529.65 W
Switching frequency	25 KHz
Supply frequency	50 HZ
Transformer ratio	1:7
Efficiency	93.28%
Power factor	0.99995
THD	2.95

4. Conclusion

Thus, an PFC circuit with VD unit is depicted and successfully simulated [13]. The input voltage given to the circuit was reduced to half when compared to the previous circuit. But the Response voltage and the power ratings are same despite of the decreased input. This is due to the voltage doubler unit. In this circuit the reduced switching loss of 6.7% is obtained with the THD 2.95[12]. The improvised performance efficiency with the input condition of 529.65W / 31.21A is 93.28%.

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