Phase Opposition Disposition PWM Strategy and Capacitor Voltage Control for Modular Multilevel Converters

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Abstract*-- *This paper focuses on the carrier disposition Pulse Width Modulation (PWM) strategies for Modular Multilevel Converters (MMC). The authors propose a new Phase Opposition Disposition PWM (PODPWM) scheme applicable regardless of the converter's sub-modules number. Moreover, a capacitor voltage sorting algorithm is synthesized aiming to ensure the converter's balanced operation. Simulation results of a 3.6 MVA, 3-SM-MMC are presented and discussed.

***Index Terms*-- Modular multilevel converter, pulse width modulation, circulating current, active balance**

1. Introduction

The Modular Multilevel Converter (MMC) was proposed by R. Marquardt in 2001 [1]. MMC topology has proved to be an attractive alternative in high voltage applications such as HVDC transmissions [2]-[3]. It is made by a serial connection of identical DC-choppers called Sub-Modules (SM), with flying capacitors that stand for independent DC sources. The output voltage is obtained by a control of the state of sub-modules switches with taking into account the capacitors voltage balance and the circulating current, which are the main issues of this topology [4].

Many research studies have been dedicated to the modulation of the MMC converter. The modularity and simple implementation of PWM-based modulation strategies make them the most suitable for MMC converters [5]. In this paper three Carrier Disposition CDPWM strategies are considered: Phase Disposition PWM (PDPWM), Alternative Phase Opposition Disposition PWM (APODPWM) and Phase Opposition Disposition PWM (PODPWM). Previous researches [6]-[7] demonstrated that when used for MMC modulation, PDPWM yields to better THD performances. PODPWM and APODPWM performances can be enhanced using an output filter. Furthermore, lower circulating current and inductor voltage are obtained with PODPWM and APODPWM techniques considering the higher number of voltage levels. However, in [8], it is shown that PODPWM technique is applicable only when the number of sub-modules per arm is even. In this paper, the authors propose an original implementation of the PODPWM for MMC converters that remains valid regardless of the converter's sub-modules number.

2. Operation Principle and Modulation Strategies for MMC Converters

A. Operation Principle of MMC Converter

The topology of a three-phase MMC is depicted in fig.1. One leg converter consists of a connection of two arms. Each arm is a series connection of N identical sub-modules (SM) and an inductor L. Each SM contains a half bridge converter and one capacitor C as shown in fig.2.For a given SM in the upper arm (respectively lower arm), the

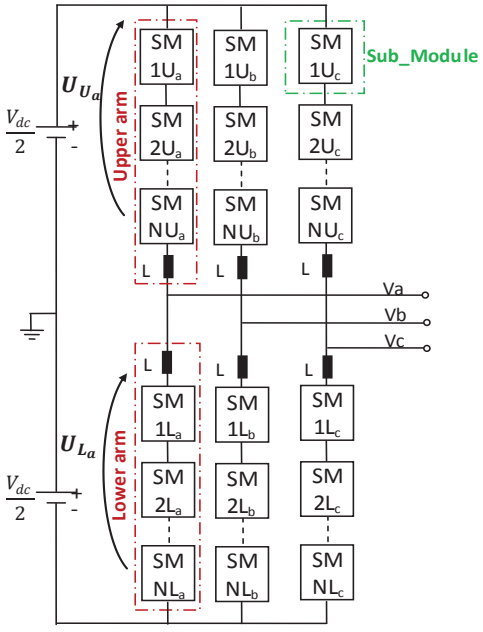

Fig. 1. N-SM Modular Multilevel Converter

output voltage $U_{SM\_Ui}(t)$ (respectively $U_{SM\_Li}(t)$) is given by

$$\begin{cases} U_{SM\_Ui}(t) = SC_{Ui}.U_{c\_Ui}(t) \\ U_{SM\_Li}(t) = SC_{Li}.U_{c\_Li}(t) \end{cases} \quad (1)$$

where SC_{Ui} (respectively SC_{Li}) is the modulation function of the i^{th} SM in the upper arm (respectively the i^{th} SM in the lower arm) and $U_{c\_Ui}(t)$ (respectively $U_{c\_Li}(t)$) is the corresponding flying capacitor voltage. SC_{Ui} and SC_{Li} are equal to 1 when the SM's upper switch is ON and the SM's lower switch is OFF, and are equal to 0 when the SM's upper switch is OFF and the lower switch is ON.

Under full balance conditions, we can write

$$U_{C\_Ui}(t) = U_{C\_Li}(t) = U_C(t) = \frac{V_{dc}}{N} \quad (2)$$

where N is the number of sub-modules per arm.

Consequently

$$\begin{cases} U_{Ux}(t) = \sum_{i=1}^{N} U_{SM\_Ui_x}(t) = \sum_{i=1}^{N} SC_{Ui_x}.\frac{V_{dc}}{N} = \frac{n_{U_x}}{N}V_{dc} \\ U_{Lx}(t) = \sum_{i=1}^{N} U_{SM\_Li_x}(t) = \sum_{i=1}^{N} SC_{Li_x}.\frac{V_{dc}}{N} = \frac{n_{L_x}}{N}V_{dc} \end{cases} \quad (3)$$

where x denotes phase a, b or c, $U_{Ux}(t)$ and $U_{Lx}(t)$ denote respectively phase x upper and lower arm voltages and n_{U_x} and n_{L_x} are the number of the ON-stated SM of phase x upper and lower arm respectively.

Kirchhoff' s voltage law for phase a can be expressed as

$$V_a - \frac{V_{dc}}{2} + U_{U_a} + L\frac{di_{U_a}}{dt} = 0 \quad (4)$$

$$V_a + \frac{V_{dc}}{2} - U_{L_a} - L\frac{di_{L_a}}{dt} = 0 \quad (5)$$

The subtraction of (5) from (4) gives:

$$\frac{V_{dc} - U_{L_a} - U_{U_a}}{2} = L\frac{d}{dt}\left(\frac{i_{U_a} + i_{L_a}}{2}\right) = L\frac{di_{za}}{dt} \quad (6)$$

where i_{za} is defined as phase a circulating current.

Under balance condition operation, the converter output current is equally split among the two corresponding arms.

Therefore, phase a output current can be written as

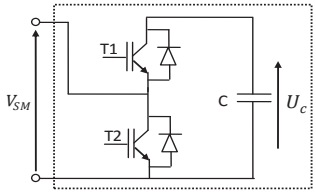

Fig. 2. Topology of a single Sub-Module SM of a MMC converter

$$i_a = \frac{i_{U_a} - i_{L_a}}{2} \quad (7)$$

and i_{za}, which results from the voltage difference between the DC bus and the sum of the upper and lower arms voltages, is given by

$$\begin{cases} i_{z_a} = 0 \\ V_{dc} = U_{L_a} + L\frac{di_{L_a}}{dt} + U_{U_a} + L\frac{di_{U_a}}{dt} = U_{L_a} + U_{U_a} + 2L\frac{di_{za}}{dt} = U_{U_a} + U_{L_a} \end{cases} \quad (8)$$

Moreover, from (3) and (8), one can write:

$$n_{U_a} + n_{L_a} = N \quad (9)$$

Thus, for a balanced MMC converter operation, the modulation strategy and algorithm control has to ensure that N SMs among the 2N available ones are switched ON.

B. PWM Strategies for MMC Converters

PWM based modulation strategies are widely used in multilevel converters modulation [9]. The association of each triangular carrier to a particular SM goes along with the nature of modularity and scalability for MMC converters [5]. However, the influence of the carriers' disposition on the MMC converter is still not deeply investigated. Basically, their arrangement directly influences the number of the output voltage levels [10]. This criterion was used to classify modulation strategies into two main categories: *N+1* and *2N+1* modulations. The first category lead to N+1 voltage levels and the second one lead to 2N+1 voltage levels.

In the following, analysis of one example of each of these two PWM categories is carried out based on a comparison of their output performances.

(N+1) modulation

An (N+1) modulated MMC converter is able to generate (N+1) voltage levels. Fig.3 shows the Alternative Phase Opposition Disposition PWM (APODPWM). Neighbored carriers are 180° phase shifted. For a 4-SM MMC converter, simple output voltage presents 5 levels, as shown in fig.3 b).

The symmetry of the carriers and reference voltages disposition in (N+1) modulation strategies guarantees that N SMs are ON switched [10]. Consequently, according to equations (4) and (5), (N+1) modulation strategies lead to a low inductor voltage and a negligible MMC circulating current.

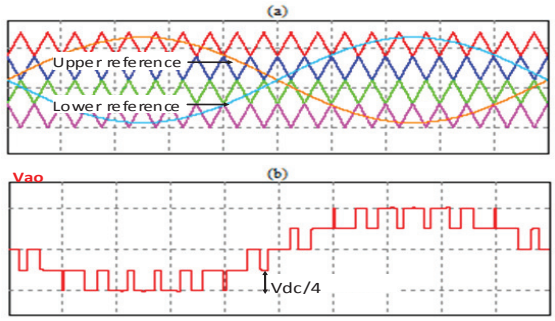

Fig. 3. (N+1) modulation strategy: APODPWM;N=4 a) carriers disposition b) Simple output voltage: 5 voltage levels

Fig.4 gives the three line currents for a 4-SM MMC converter with: V_{dc}=600 V, L=100 µH, f_{sw}=10 kHz, R_{load}=10 Ω and L_{load}=11,5 mH. Line current amplitude is equal to 25 A.

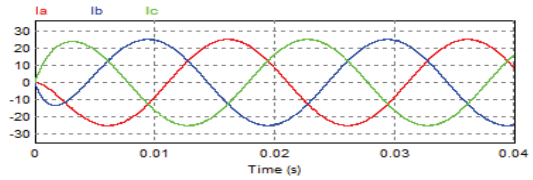

Fig. 4. 3-SM MMC APODPWM modulated converter: line currents (10A/div)

Line *a* current spectrum presented on fig.5 shows that first harmonics appear around 10 kHz with maximum amplitude equal to 0.045 A, which is lower than 0.18% of the fundamental magnitude. The THDi is equal to 0.36%

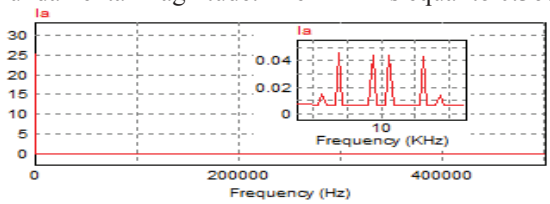

Fig. 5. Spectral analysis of Phase *a* output current

Fig.6 gives leg *a* steady state inductor voltage and circulating current. The inductor voltage, which is the difference between the phase-leg voltage and the DC side voltage, has a high frequency component that is related to the capacitors' charge and discharge [11]. Due to the small difference between the DC side voltage and the phase-leg voltage for APODPWM, the magnitude of the resulting circulating current is nearly equal to zero.

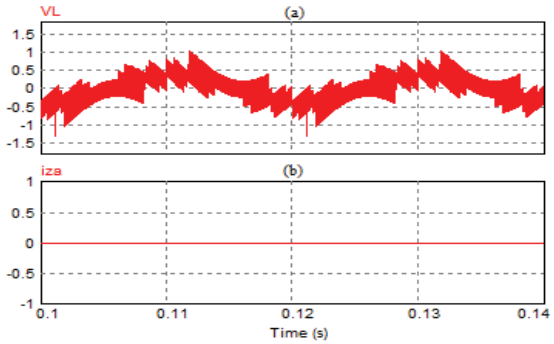

Fig. 6. APODPWM modulation strategy for a 4-SM MMC converter *Vdc*=600 V; *L*=100 µH, *fsw*=10 kHz a) inductor voltage (2.10-2V/div) b) Leg *a* circulating current i_{za}

(2N+1) modulation

MMC converter controlled with (2N+1) modulation strategies is able to generate 2N+1 voltage levels. Fig.7 shows the Phase Disposition (PDPWM) strategy used for a 4-SM MMC converter. The converter's output voltage has 9 voltage levels. Due to the asymmetry of the carriers disposition, the number of ON switched SMs varies between N, N-1 and N+1, as shown in fig.8-a and the inductor's voltage is equal to $0, +\frac{V_{dc}}{2N}$ or $-\frac{V_{dc}}{2N}$ as shown in fig.8-b. First harmonics appear at 20 kHz with maximum amplitude equal to 8 mA.

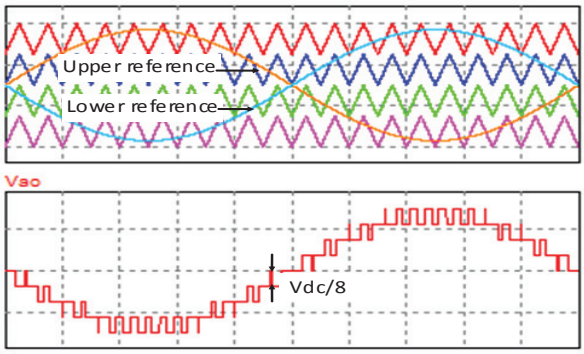

Fig. 7. 2N+1 modulation strategy: PDPWM a) carriers disposition b) leg *a* output voltage: 9 levels

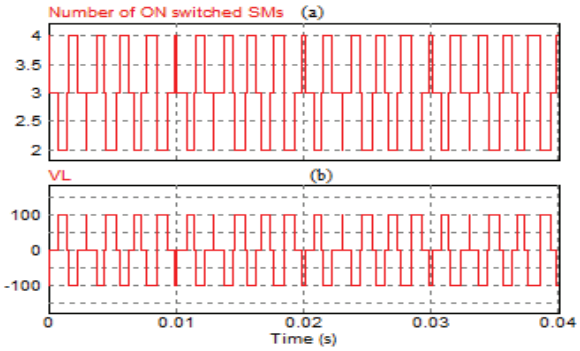

Fig. 8. PDPWM modulation strategy for a 3-SM MMC a) voltage level b) leg *a* upper arm inductor voltage

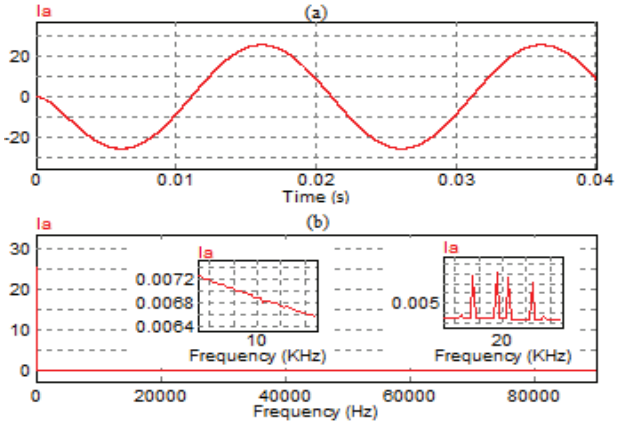

Fig. 9. Line a current a) temporal analysis b) spectral analysis

As the number of ON switched SMs is not always equal to N, the circulating current increases dramatically and reaches 20 A as shown in fig.10. However, the increase of the output voltage levels improves THDv with a 5% rate and THDi with 77% rate compared to APODPWM.

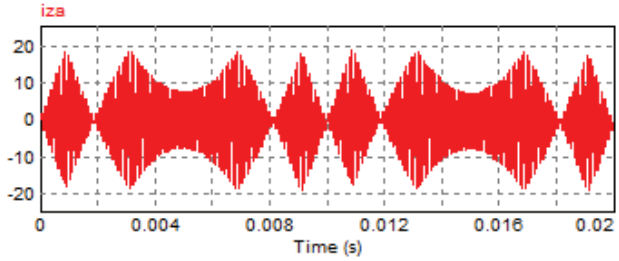

Fig. 10. Leg *a* circulating current under PDPWM modulation strategy

C. Limits of Existing PODPWM Strategy for MMC Converters

The disposition of the references and carriers is the key element towards the possibility to apply the PODPWM according to the number of sub-modules.

For example, PODPWM proposed in [8] is based on the comparison of N carriers with the upper arm reference to generate the upper arm control signals, and the comparison of the same carriers with the lower arm reference to generate lower arm control signals. This strategy is only effective when sub-modules number is even, as shown in fig. 11 where N=4.

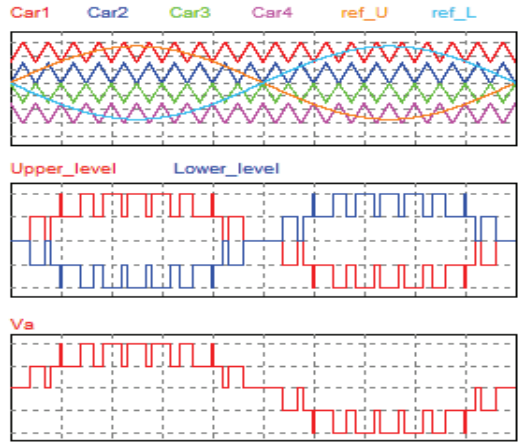

Fig. 11. PODPWM for MMC with even number of sub-modules; N=4

However, the strategy is limited when the sub-modules number is odd. In fact, with this disposition, it is impossible to define the carriers' phases so that they are symmetric according to the average value of the reference signal. The asymmetry causes an imbalance in the upper and lower levels, as shown in fig. 12 (N=5).

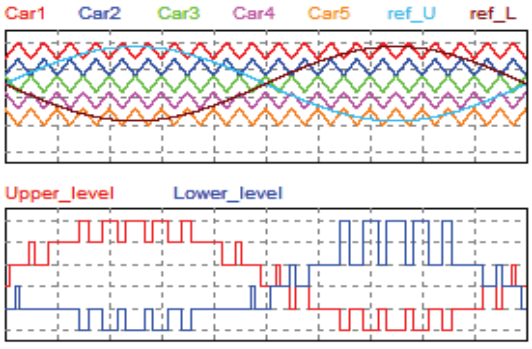

Fig. 12. PODPWM for MMC with odd number of sub-modules; N=5

In order to generalize PODPWM strategy for even and odd sub-modules number per branch, this paper proposes an original scheme that aims to modify the carriers and references disposition.

3. Proposed PODPWM Strategy Implementation for MMC Converter

Basically, the PODPWM (Phase Opposition Disposition PWM) strategy is a (N+1) modulation type since in this case, an N-SM MMC converter generates an output voltage with N+1 levels. However, in [10], the authors confirm that this PWM strategy is limited since it is only applicable for MMC converters when the number of sub-modules in each arm is even.

In this paper, we propose a PODPWM modulation strategy for MMC converter independently of its sub-modules numbers. Simulations tests are carried out with a 3-SM MMC converter. The capacitance of each SM is equal to 6 mF. The DC bus is equal to 3600V. Two 100µH inductors are used in the arm inductors to ensure an equal distribution of the line current among the two arms. The carrier frequency is equal to 10 kHz, thus switching period equal to 100 µs. The MMC converter is connected to an *RL* load where *R* is equal to 10 Ω and *L* is equal to 11.5 mH.

A. Converter Control Principal

In this paragraph, flying capacitors are replaced by perfect DC sources, each equal to Vdc/3. The issue of flying capacitors balance is investigated in the next paragraph.

Rather than using the same carriers for upper and lower sub-modules, the proposed PODPWM assigns a carrier for each SM and a reference for each arm. The control signal of each SM results from the comparison of its carrier and its corresponding reference. PODPWM, presented on fig. 13, is designed as follows:

- All three carriers for the upper arm are identical: initial phase angle is 0 and the magnitude is equal to $\frac{V_{dc}}{N}$. These three carriers are vertically shifted with $\frac{V_{dc}}{N}$, forming 3 contiguous bands varying from 0 to V_{dc}. They are compared with a sinusoidal reference V_{ref_U} defined as follows:

$$V_{ref\_U}(t) = \frac{V_{dc}}{2} + m\frac{V_{dc}}{2}\cos(2\pi ft) \qquad (10)$$

where V_{dc} is the DC bus, m is the modulation depth and f is the reference frequency

- All three carriers for the lower arm defined with 180° initial phase and $-\frac{V_{dc}}{N}$ magnitude, forming 3 contiguous bands varying from $-V_{dc}$ to 0. The so generated carriers are compared with a sinusoidal reference V_{ref_L} defined by:

$$V_{ref\_L}(t) = -\frac{V_{dc}}{2} + m\frac{V_{dc}}{2}\cos(2\pi ft) \qquad (11)$$

One can note that both references and carriers are symmetrical according to the 0 voltage level. Unlike PDPWM, the symmetry property can also be found on each arm phase level, as shown in fig.14.

Fig.15 shows that for a three-SM MMC converter, the number of switched ON SMs is continually equal to 3.

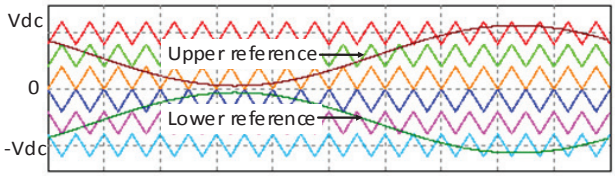

Fig. 13. Proposed PODPWM for a 3-SM MMC converter

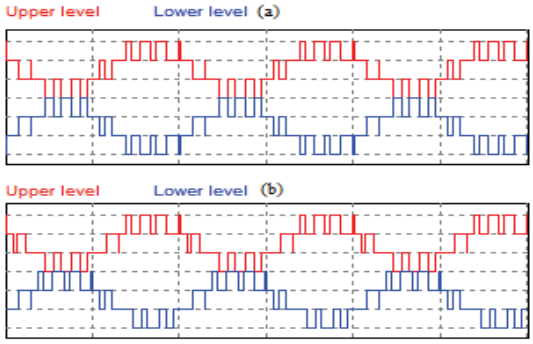

Fig. 14. Upper and lower arms voltage levels a) PODPWM b)PDPWM

Therefore, the DC bus-leg balance condition defined in (9) is verified, leading to a sensitive reduction of the inductor voltage as shown in fig.16.

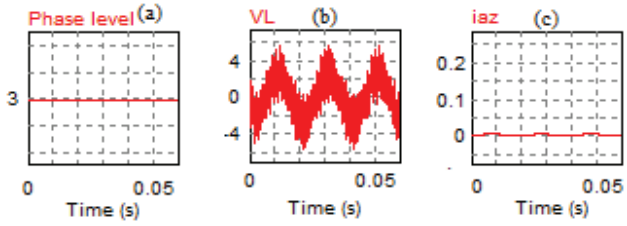

Fig. 15. 3-SM MMC converter leg characteristics a)Number of ON switched SMs b) Inductor voltage c) circulating current

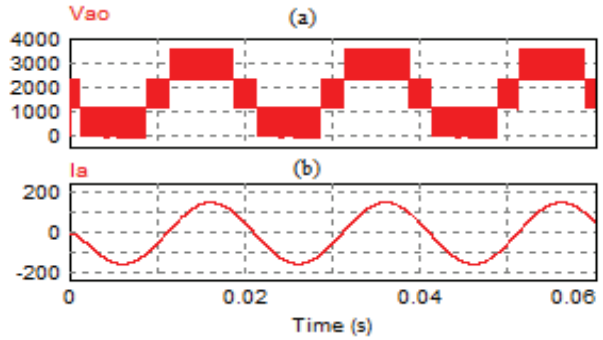

Fig. 16. 3-SM MMC converter a) Simple output voltage b) Line current

B. Flying Capacitors Voltage Balance Issue

When perfect DC sources are replaced with flying capacitors, output leg voltages are unbalanced, as shown on fig.17.

However, for an MMC converter, the same voltage level can be obtained with different configurations of the sub-modules control signals. This degree of freedom can be exploited to perform the flying capacitors voltage balance.

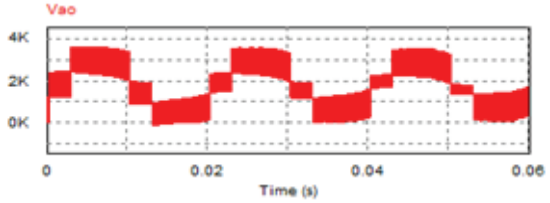

Fig. 17. Leg *a* output voltage of MMC without balancing algorithm

In fact, PODPWM carriers are not assigned to specific SMs. They are used to determine the required voltage level for upper and lower arms. It is to mention that the arms of each leg are controlled separately, but the number of ON switched SM in both arms together is equal to N. For a 3-SM MMC converter, each arm can generate 4 voltage levels: 0, 1, 2 and 3. If voltage level is equal to 0 (respectively 3), all control signals have to be equal to 0 (respectively 1). However, many combinations are available to achieve voltage level 1 and 2. This extra degree of freedom is used to perform flying capacitors voltage balance. If voltage level is equal to 1, the switched ON SM is the one with the most charged or discharged flying capacitor, depending on the current sign. Likewise, if voltage level is equal to 2, the SMs with the most charged or discharged flying capacitors are switched ON. This strategy is extendable to N number of sub-modules. A sorting algorithm is implemented in order to determine the priority degree for each flying capacitor. For an N-SM MMC converter, the sorting algorithm is as follows:

- Measured flying capacitors voltages of each branch are stored in an array with N cells.
- We suppose that array's first cell contains the greatest value. We browse the cells from 2 to N with comparing the value of each cell with value n°1. If value n°1 is less than value n° X, cells 1 and X switch values.
- The same algorithm is applied for the next (N-1) cells.

The sorting algorithm output is an array of N cells, containing the N capacitors voltages sorted from greatest to lowest. The sorting algorithm is depicted on fig.18 and fig. 19 shows the overall block diagram of the proposed method, applied to one single arm.

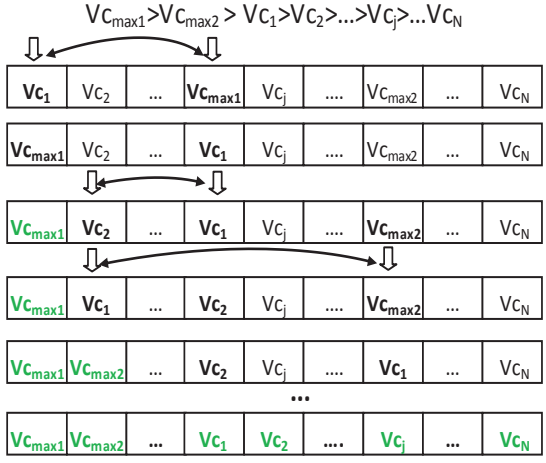

Fig. 18. Sorting algorithm for an N-SM MMC

The converter's output voltages are shown on fig. 20. Line to line output voltage shows the expected voltage levels. However, when a zoom is applied on the different levels, an error equal to 100V appears. This error corresponds to the flying capacitors voltages. Fig. 21 shows the flying capacitors voltages of the upper and lower arms of leg *a*. The error varies between 100V and 51V which respectively represents 4.16% and 2.1% of the initial voltage.

Line to line output voltage shows the expected voltage levels. However, when a zoom is applied on the different

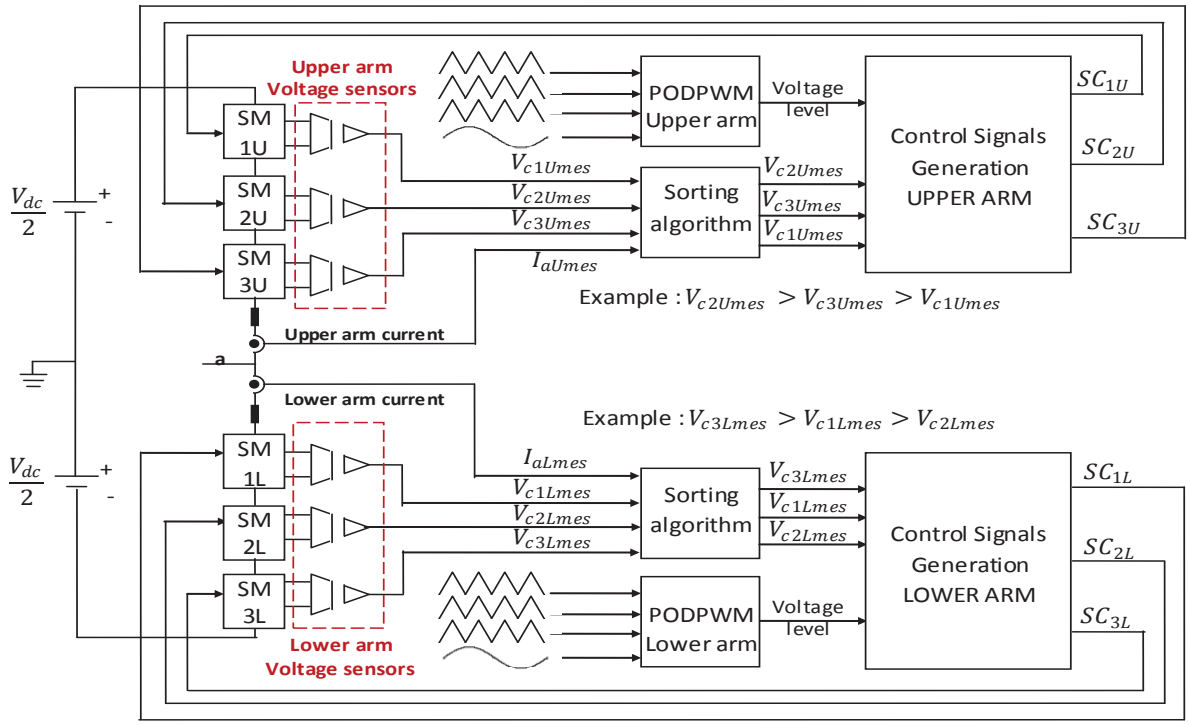

Fig. 19. Block diagram of the proposed algorithm applied for one leg

levels, an error equal to 100V appears. This error corresponds to the flying capacitors voltages. Fig. 21 shows the flying capacitors voltages of the upper and lower arms of leg *a*. The error varies between 40V and 22V which respectively represents 3.33% and 1.8% of the initial voltage

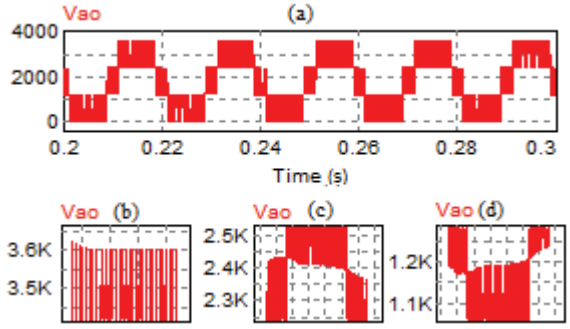

Fig. 20. Three-SM MMC converter output voltage a)output voltage b) zoom on the 3600V level c) zoom on the 2400V level d) zoom on the 1200V level

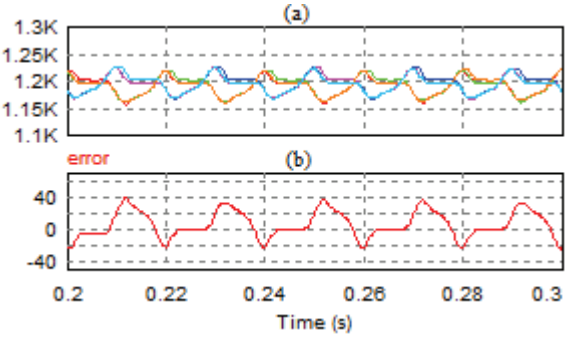

Fig. 21. Voltage balance outputs a) Leg *a* flying capacitors voltages b) error on the capacitor voltage of the first sub module of leg *a* upper arm.

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