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Impact of Various Gate Dielectric Arrangement on the RF Performance of FDSOI MOSFET

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Abstract: In this work, comparative study of different structures i.e conventional with high-k material as gate insulator, gate stack (GS), symmetric double material gate insulator (SDMGI), asymmetric double material gate insulator (ADMGI) FDSOI MOSFET have been performed for investigation of its analog and RF performance. The important figure of merits (FOMs) studied in this work are on-state drive current, ION/IOFF, transconductance (gm), transconductance efficiency (gm/ID), output conductance, early voltage, intrinsic gain, cut-off frequency (fT), transconductance frequency product (TFP), output conductance (gd), gain frequency product (GFP) and gain transconductance frequency product (GTFP). It has been observed that best FOMs is obtained in case of SDMGI based MOSFET structure. It has further been observed that on increasing the BOX thickness of SDMGI FDSOI MOSFET, performance improves but on considering high-k as an alternative BOX material or increase in gate-insulator thickness, its performance degrades. All the design and simulation has been done using Silvaco TCAD tool.

Keywords: FDSOI MOSFET; Short Channel Effects (SCEs); high-k; Radio Frequency (RF).

1. Introduction

To meet the ever-increasing demand of wireless world, the requirement for low power dissipation, fast switching, high speed and high frequency devices is continuously pushing the fabrication to shrink in nanometre regime [1] - [2]. As the devices scales down into nanometre regime, SCEs like drain induced barrier lowering, hot carrier charge effect, impact ionization etc. takes place due to which device performance degrades [3]. To obtain same device performance as that of conventional MOSFET, there is need of high doping concentration in the channel region due to which undesirable junction capacitances increases. Ran-Hong et al. explained that junction capacitance can be reduced by using fully depleted silicon-on insulator (FDSOI) MOSFET [4]. It is also reported that the hot carrier charge effect is reduced whereas analog and RF performance improves when PDSOI or bulk Si devices is replaced by FDSOI [5] - [9]. Scaling of MOSFET requires reduction of gate oxide thickness but when the gate oxide thickness is decreased direct tunnelling current through the gate dielectric increase exponentially at 50 nm gate length, which increases standby power of the chip. To get rid of this problem high-k dielectric material as gate insulator is used. Conventional with high-k as gate insulator (CH-k) based MOS structure helps to reduce leakage current to some extent as compared to SiO_2 of same electrical thickness [10] - [12]. However, it is also reported that due to fringing field effect the short channel performance degrades when high dielectric is directly deposited on the silicon film and this issue can be resolve by using gate stack FDSOI MOSFET [13] - [16]. Pradhan et al. has reported that silicon nitride in the single layer gate stack configuration provides better RF performance as compared to other high dielectric materials [17]. In order to further reduce the short channel effects (SCEs) gate insulator is replaced by hetero gate dielectric in symmetric manner and due to different permittivity an additional peak is obtained in electron velocity and electric field which results in enhanced value of carrier transport efficiency. It was also observed that an improved value of I_{OFF}, transconductance and transconductance generation factor is obtained [18]. Proper asymmetricity in oxide division of gate dielectric material improves I_{ON} to I_{OFF} ratio [19]. The transconductance efficiency, g_m,, g_d, f_T, TFP and GTFP are important parameters for the design of low power and high frequency circuits [20] - [23].

In this work, for the first time, a comparative analysis on the analog and RF performance of conventional, gate stack, conventional with high-k as gate insulator, SDMGI, ADMGI FDSOI MOSFET devices has been carried out with the help of simulation tool in order to find which one is best for fast

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switching, low power and high frequency applications. The paper is organized in subsequent sections as follows. Section 1 provides the brief introduction of the work. Section 2 discuss about the specification of all the designed devices along with the geometry of all the structures. Section 3 consists of the simulated results of analog and RF parameter of all the structures and finally the relevant conclusions are made.

2. Device Structure and Specification

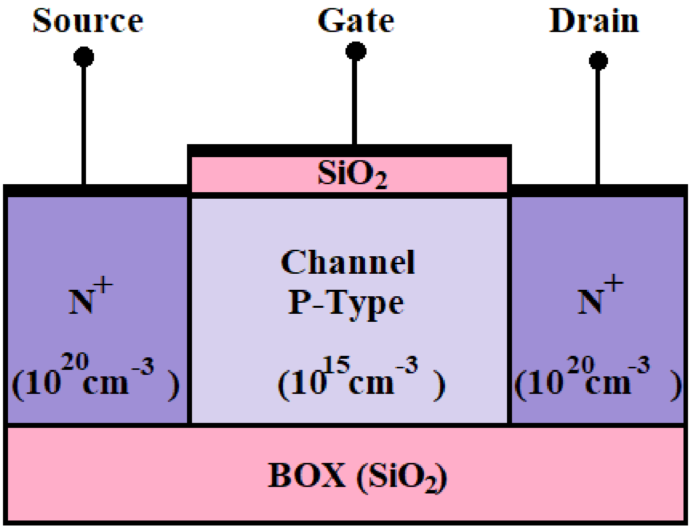
In this paper, different types of MOSFET structure models have been presented. Figure 1(a) shows the model of conventional FDSOI MOSFET and its device specification is listed in Table 1.

Table 1. Device Specification of Conventional FDSOI MOSFET

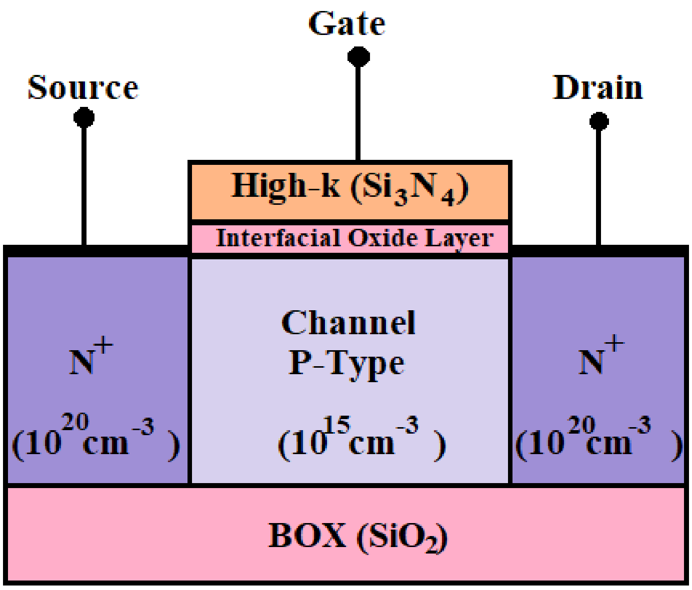
Parameters	Values
Drain Voltage (V_{DS})	1.1 V
Doping in Source region	1 x 10^{20} cm^{-3}
Silicon Thickness	12nm
Work Function of Gate	4.77eV
Doping in Drain region	1 x 10^{20} cm^{-3}
Gate Length	50 nm
Doping in Channel	1 x 10^{15} cm^{-3}
BOX Thickness	5nm

In case of second model which is shown in Figure 1 (b) gate stack FDSOI MOSFET is designed in which thick high-k (Si_3N_4) layer is deposited over a thin layer of silicon dioxide to significantly reduce gate tunnelling current. Third model is shown in Figure 1(c) in which silicon dioxide (SiO_2) as gate insulator is replaced by high-k (Si_3N_4) dielectric to reduce hot carrier charge effect and impact ionization. Symmetric double material gate insulator (SDMGI) is shown in Figure 1(d) in which silicon dioxide (SiO_2) as gate dielectric material is substituted by heterogeneous dielectric with silicon nitride at source end and hafnium oxide at drain side in symmetric way to improve electron velocity and carrier transport efficiency. Asymmetric double material gate insulator (ADMGI) is shown in Figure 1(e) in which silicon dioxide as gate dielectric material is substituted by heterogeneous dielectric with silicon nitride at source end and hafnium oxide at drain end in asymmetric way.

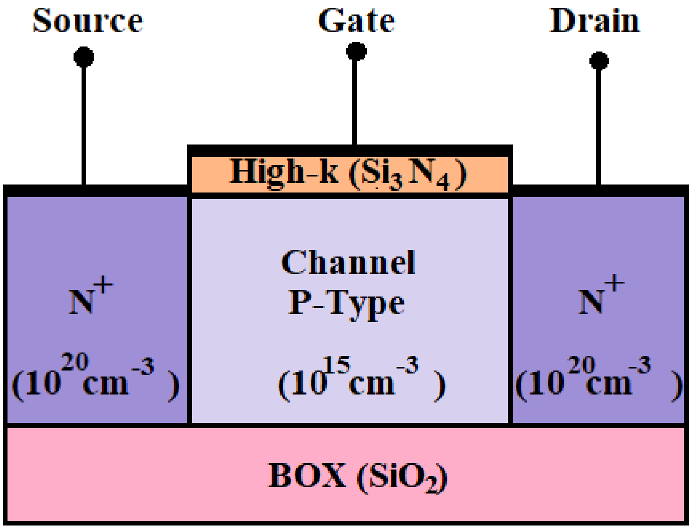
In order to analyse the analog and RF performance, the results are extracted using Silvaco TCAD tool. The simulation of leakage current is done by using Shockley-Read-Hall model. The parallel electric field dependence model is used to model velocity saturation effect. The Lombardi model is used for electric field modelling and uniform doping profile is used.



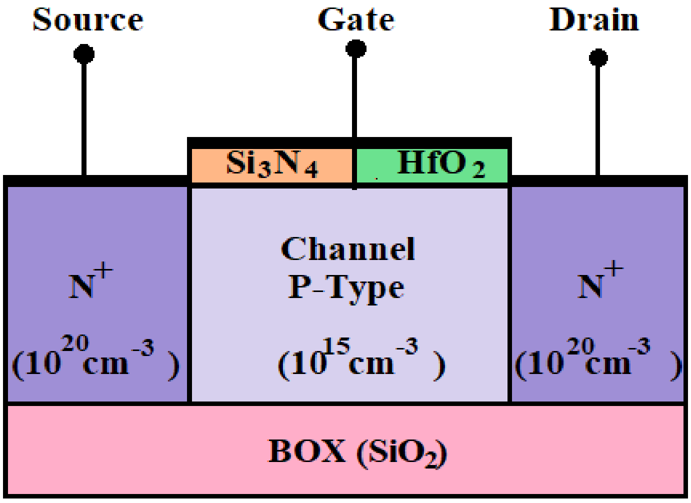
(a)


Gate
Source
Drain
High-k (Si_3N_4)
Interfacial Oxide Layer
N^+
($10^{20}cm^{-3}$)
Channel
P-Type
($10^{15}cm^{-3}$)
N^+
($10^{20}cm^{-3}$)
BOX (SiO_2)

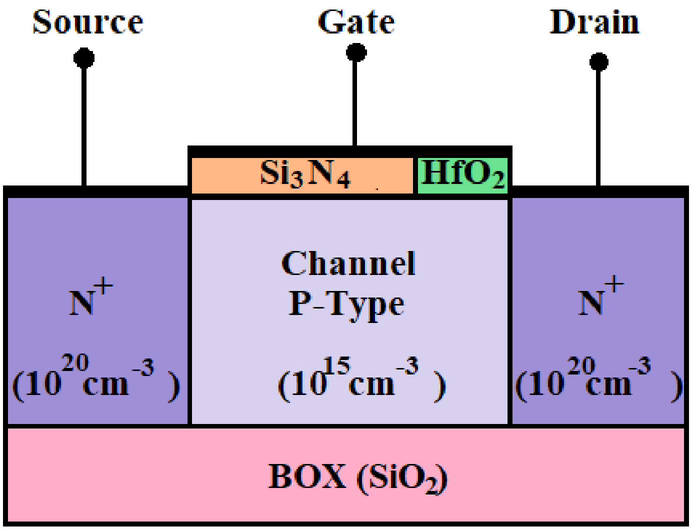
(b)


Source
Gate
Drain
High-k (Si_3N_4)
N^+
($10^{20}cm^{-3}$)
Channel
P-Type
($10^{15}cm^{-3}$)
N^+
($10^{20}cm^{-3}$)
BOX (SiO_2)

(c)


Source
Gate
Drain
Si_3N_4
HfO_2
N^+
($10^{20}cm^{-3}$)
Channel
P-Type
($10^{15}cm^{-3}$)
N^+
($10^{20}cm^{-3}$)
BOX (SiO_2)

(d)



(e)

Figure. 1 Simulated device structure of (a) Conventional FDSOI MOSFET (b) Gate Stack (GS) FDSOI MOSFET (c) Conventional with high-k as gate insulator (CH-k) FDSOI MOSFET (d) SDMGI FDSOI MOSFET (e) ADMGI FDSOI MOSFET.

3. Results and Discussion

The simulation models have been validated using Visual TCAD tool. Figure 2 shows the extracted data of transfer characteristics of SDMGI obtained using Silvaco TCAD tool and Visual TCAD tool. The fitting results are obtained from both the models.

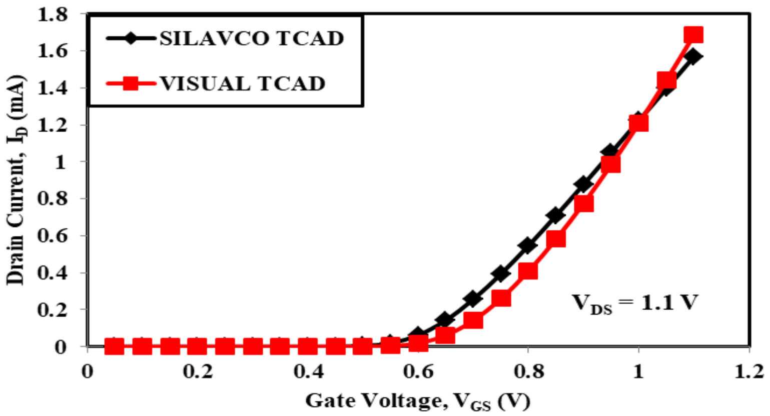
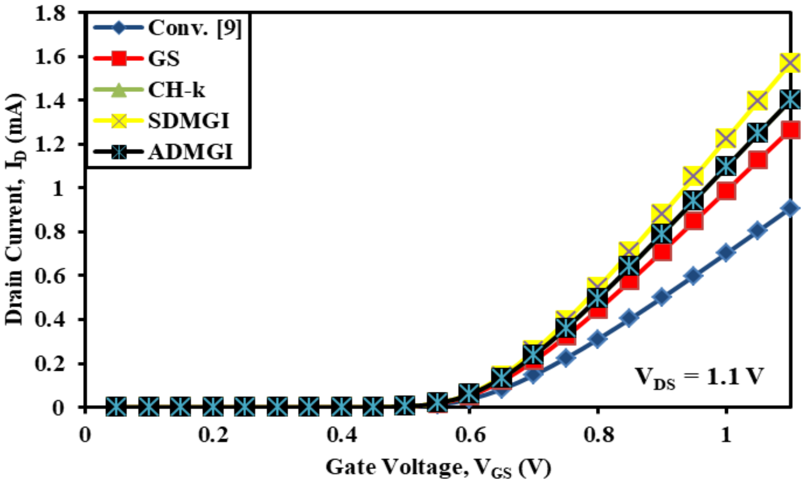
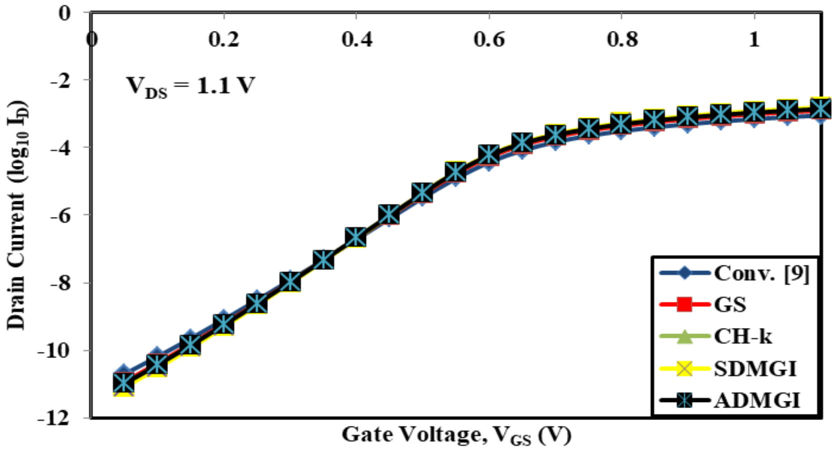


Figure. 2 Validation of transfer characteristics of SDMGI with Visual TCAD tool and Silvaco TCAD tool.

The transfer characteristics is shown in Figure 3 for different structures. Leakage current is the drain current measured at V_{GS} = 0V and V_{DS} = 1.1 V. To minimize static power dissipation in standby mode leakage current must be small. It is apparent from the figure that in case of symmetric double material gate insulator (SDMGI), leakage current is lowest as compared to other structures. It is also observed from the figure that highest on-state drive current is obtained in case of SDMGI. In SDMGI, the permittivity of gate insulator material near the source end is lower than that near the drain end. As a result, an additional peak is obtained in electric field near the junction of the two gate insulator materials which results in increment of gate controllability over the conductance of the channel. Thus, SDMGI is capable of driving high capacitive loads. The comparison of I_{ON}/I_{OFF} of different structures is presented in Figure 4. The ratio of I_{ON} to I_{OFF} is an important parameter to determine device performance. In SDMGI leakage current is lowest whereas on-state current is highest due to which I_{ON}/I_{OFF} is highest and it is most suitable for fast switching applications.



(a)



(b)

Figure. 3 Transfer Characteristics of different structures (a) linear scale (b) log scale.

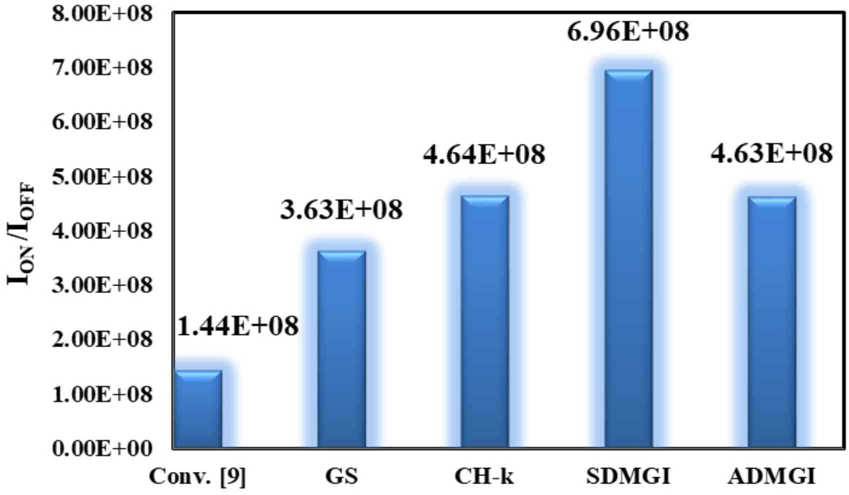


Figure. 4 Comparison of I_{ON}/I_{OFF} of different structures.

Figure 5 shows transconductance versus gate voltage (V_{GS}) characteristics of different structures. Transconductance is mathematically expressed in (1) and determine gain of MOSFET amplifiers. It is apparent from the figure that transconductance is highest when silicon dioxide as gate dielectric material is substituted by heterogeneous dielectric in symmetric way. In SDMGI, electron velocity increases due to different permittivity of two gate insulator materials which results in increase of gate transport efficiency. Hence, SDMGI is suitable candidate for analog applications due to highest g_m as compared to other structures.

$$g_m = \delta I_D/\delta V_{GS} \qquad (1)$$

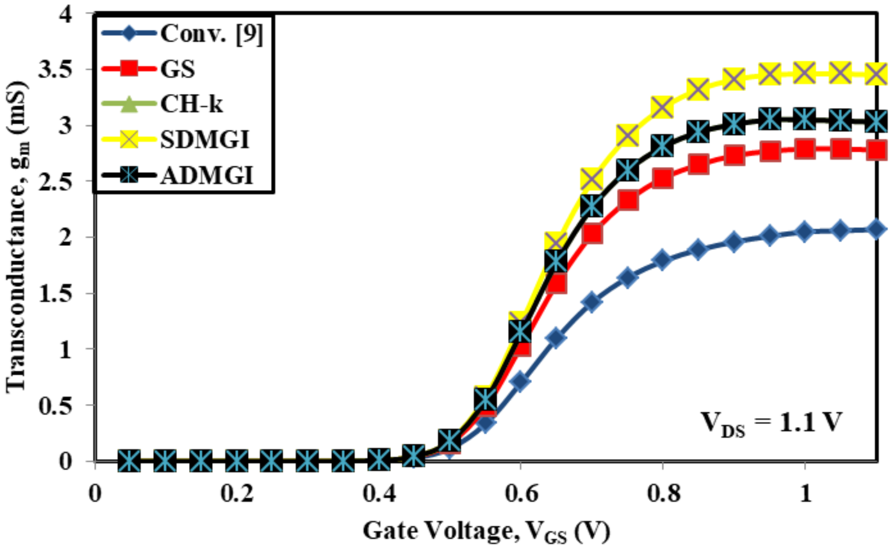


Figure. 5 Transconductance Vs. Gate voltage (V_{GS}) characteristics of different structures.

Figure 6 shows transconductance efficiency (g_m/I_D) versus gate voltage characteristics for different structures and is formulated in (2). It is observed from the figure that highest value of transconductance efficiency is obtained in SDMGI. To operate analog circuit at low supply voltage, high value of transconductance efficiency is advantageous.

$$\text{Transconductance Efficiency} = g_m/I_D \qquad (2)$$

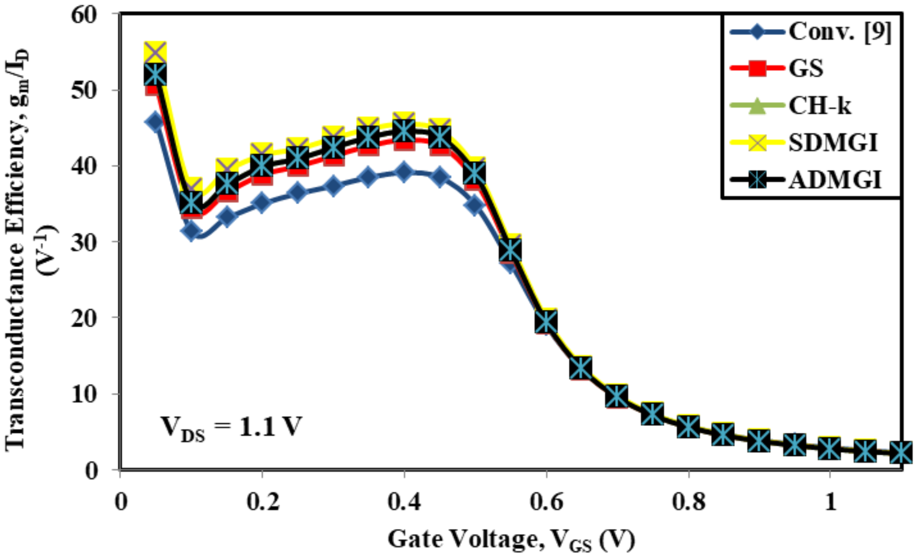


Figure. 6 Transconductance efficiency - Gate voltage characteristics of different structures.

Output conductance (g_d) versus drain voltage (V_{DS}) is shown in Figure 7 and is formulated in (3)

$$g_d = \delta I_D/\delta V_{DS} \qquad (3)$$

As per the drain characteristics, drain current is highest in case of SDMGI due to which output conductance is highest. Output resistance (R_0) is inversely proportional to output conductance due to which when g_d is high then R_0 is low which results in increase in I_D with V_{DS}. In order to obtain high gain, output conductance must be low.

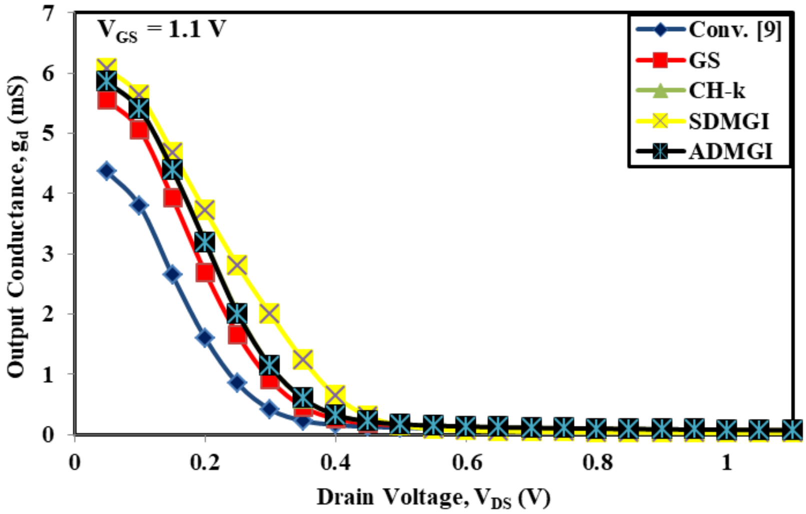


Figure. 7 Output conductance (g_d) Vs. Drain voltage (V_{DS}) characteristics of different structures.

Figure 8 and Figure 9 shows variation of early voltage and intrinsic gain with gate voltage of different structures. In order to achieve better analog performance, early voltage and intrinsic gain should be as high as possible. The dependence of drain current on drain bias will be less when early voltage is high. It is evident from the figure that highest value of early voltage and intrinsic gain is obtained in case of SDMGI.

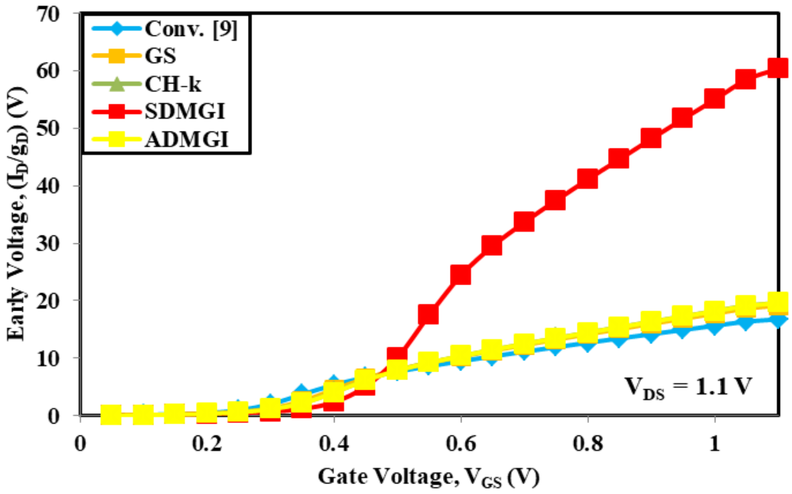


Figure. 8 Early Voltage, (I_D/g_D) Vs. Gate voltage (V_{GS}) characteristics of different structures.

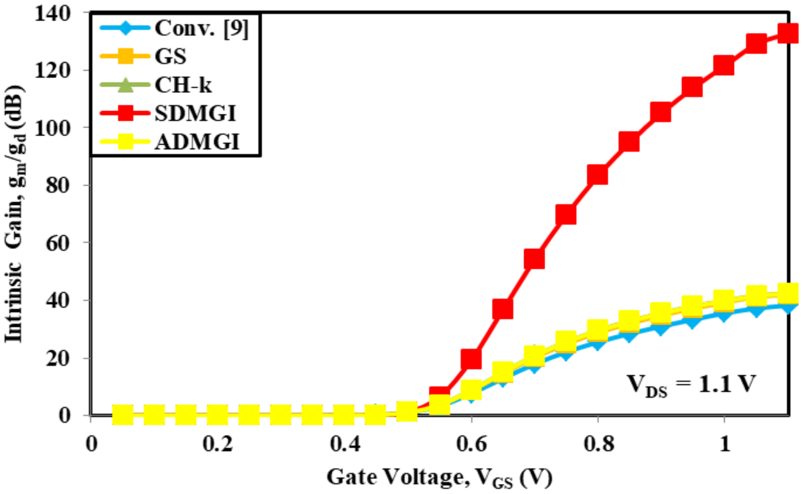


Figure. 9 Intrinsic Gain (g_m/g_D) Vs. Gate voltage (V_{GS}) characteristics of different structures.

MOSFET offers unity current gain at cut-off frequency and is formulated in (4)

$$f_T \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \qquad (4)$$

Figure 10 shows cut-off frequency (f_T) variation with gate voltage (V_{GS}) of different structures. For useful transistor operation, f_T defines the upmost frequency restriction and it should be as high as possible. Cut-off frequency is different for different structures due to different values of transconductance and partially due to high value of parasitic capacitances (C_{gd} and C_{gs}). From the simulation result, it is evident from the figure that cut-off frequency is highest in case of symmetric double material gate insulator (SDMGI). It is due to lower parasitic capacitances and higher transconductance as compared to other structures.

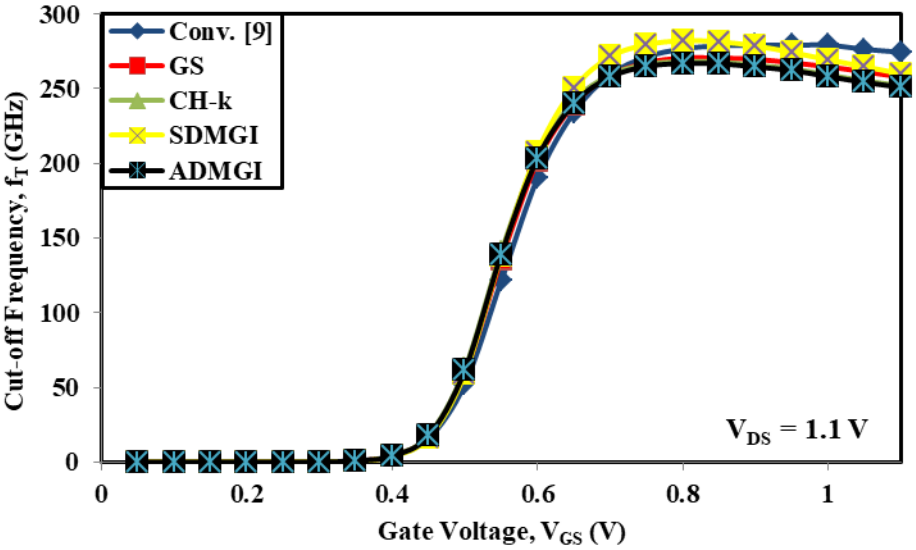


Figure. 10 Cut-off frequency Vs. Gate voltage characteristics of different structures.

From Figure 11, transconductance frequency product (TFP) versus gate voltage (V_{GS}) characteristics can be observed for different structures considered in the study. TFP depends on cut-off frequency and transconductance efficiency and is mathematically expressed in (5). TFP is key parameter when high speed system is designed. It is evident form the figure that SDMGI is suitable candidate for high speed systems due to highest value of TFP as compared to other structures.

$$TFP = (g_m/I_D) \times f_T \qquad (5)$$

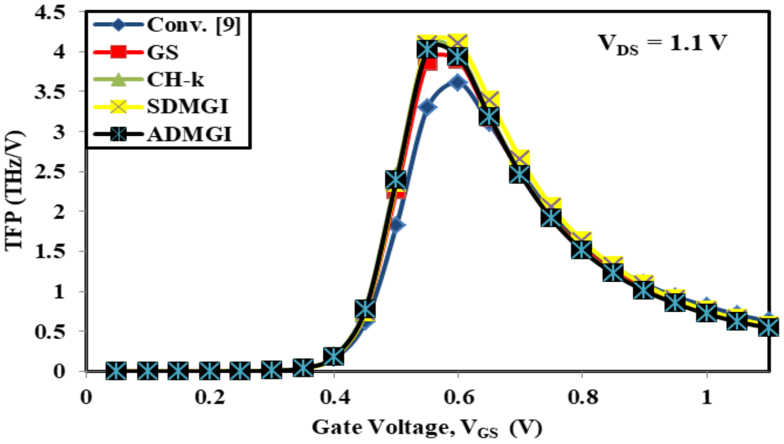


Figure. 11 Transconductance frequency product (TFP) Vs. gate voltage (V_{GS}) characteristics of different structures.

Figure 12 show gain frequency product (GFP) versus gate voltage (V_{GS}) characteristics for conventional, gate stack, high-k as gate oxide, SDMGI and ADMGI and is mathematically expressed in (6). GFP is a key parameter for devices operating as an amplifier at high frequency. It is observed from the figure that gain frequency product is highest in case of SDMGI due to high value of intrinsic gain and f_T as compared to other structures considered in our study.

$$GFP = (g_m/g_d) \times f_T \qquad (6)$$

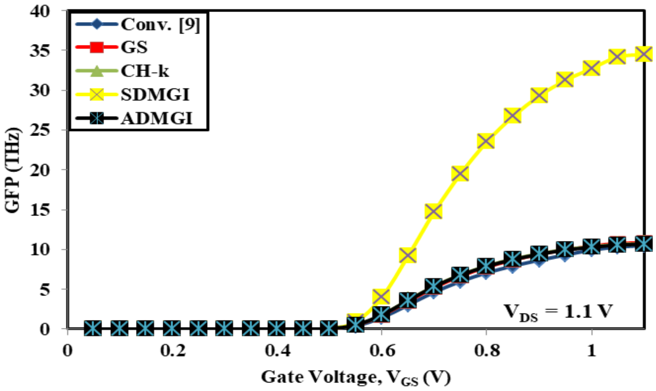


Figure. 12 Gain frequency product (GFP) Vs. Gate voltage (V_{GS}) characteristics of different structures.

Figure 13 shows gain transconductance frequency product (GTFP) versus gate voltage characteristics and is mathematically expressed in (7). GTFP is a key FOM for analog/RF circuit design to determine optimal region of operation. It is apparent from the figure that GTFP is highest in case of SDMGI.

$$GTFP = (g_m/g_d) \times (g_m/I_D) \times f_T \qquad (7)$$

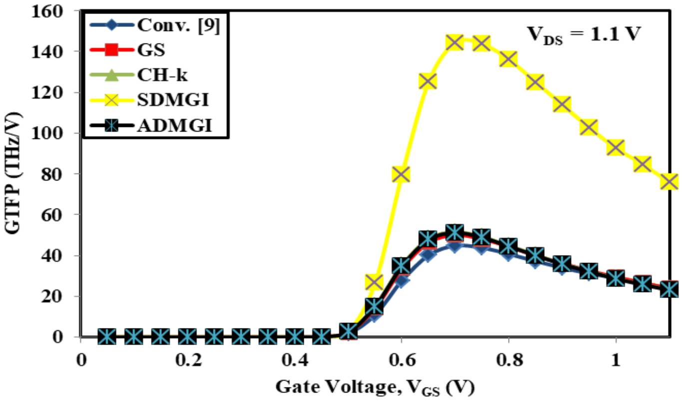


Figure. 13 Gain transconductance frequency product (GTFP) Vs. Gate voltage (V_{GS}) characteristics of different structures.

Table 2 compares peak values of DC, analog and RF parameters for different structures. Pradhan et al. reported that silicon nitride in the single layer gate stack configuration provides better RF performance as compared to other high-k dielectric materials [17]. However, after comparing GS based MOSFET structure with SDMGI it is found that SDMGI provides better performance in terms of leakage current, on-state drive current, transconductance, cut-off frequency, gain frequency product, transconductance frequency product, gain transconductance frequency product.

Table 2. DC, analog and RF performance of different devices.

FOMs	Conv. [9]	GS	CH-k	SDMGI	ADMGI
Leakage Current, I_{OFF} (pA)	6.30381	3.49064	3.01641	2.25599	3.02563
On State Drive Currrent, I_{ON} (mA)	0.907949	1.26635	1.40008	1.56916	1.4002
I_{ON}/I_{OFF}	1.44e+8	3.62e+8	4.64e+8	6.95e+8	4.62e+8
Transconductance , g_m (mS)	2.07	2.79	3.05	3.46	3.05

TGF, g_m/I_D (V^{-1})	45.78	50.59	51.95	54.74	51.92
Early Voltage, V_{EA} (V)	16.77	19.14	19.65	60.36	19.59
Intrinsic Gain , A_V (dB)	38.23	42.01	42.52	132.71	42.41
Cut-off frequency, f_T (GHz)	279.28	270.74	268.28	282.29	267.03
TFP (THz/V)	3.62	3.89	4.07	4.11	4.02
GFP (THz)	10.50	10.83	10.72	34.52	10.65
GTFP (THz/V)	44.87	50.05	51.55	144.37	51.15

The effect of varying gate insulator thickness (t_{ox}) on DC, analog and RF performance of SDMGI based MOSFET structure is analysed. The analysis is done by increasing gate insulator thickness from 1nm - 2nm keeping all other parameters constant. S. Das et al. has reported that on decreasing the insulator thickness drain induced barrier lowering (DIBL) effect gets reduced [24]. From the simulation result, it is evident from Figure 14 that when gate insulator thickness is increased in SDMGI FDSOI MOSFET, leakage current is increased whereas on-state drive current is decreased due to which I_{ON}/I_{OFF} gets decreased. It is also observed from Figure 15 and Figure 16 that the analog and RF performance of SDMGI based MOSFET structure degrades when the thickness of gate insulator is increased from 1 nm - 2 nm due to which thick gate insulator is not preferred in SDMGI FDSOI MOSFET for fast switching, high speed and high frequency applications.

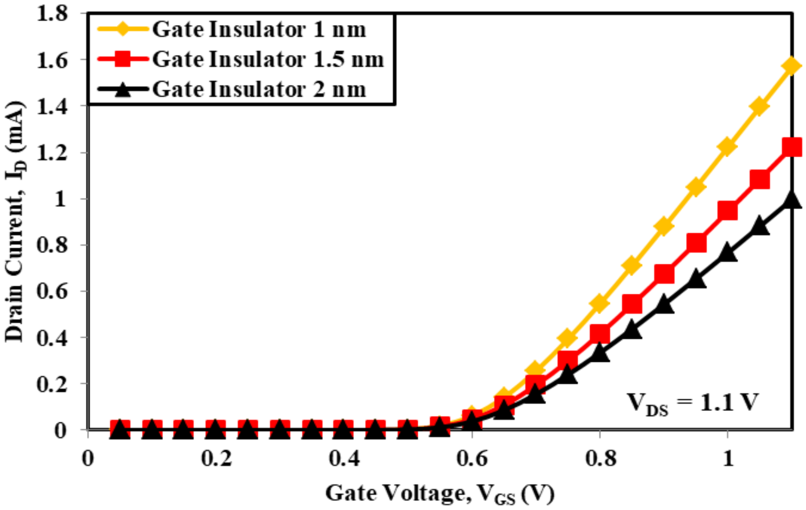


Figure. 14 Transfer Characteristics of SDMGI for different gate insulator thickness.

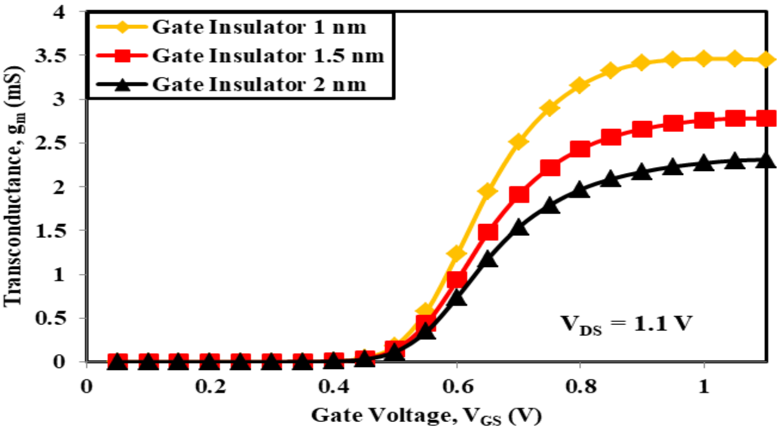


Figure. 15 Transconductance – Gate voltage (V_{GS}) characteristics of SDMGI for different gate insulator thickness (t_{ox}).

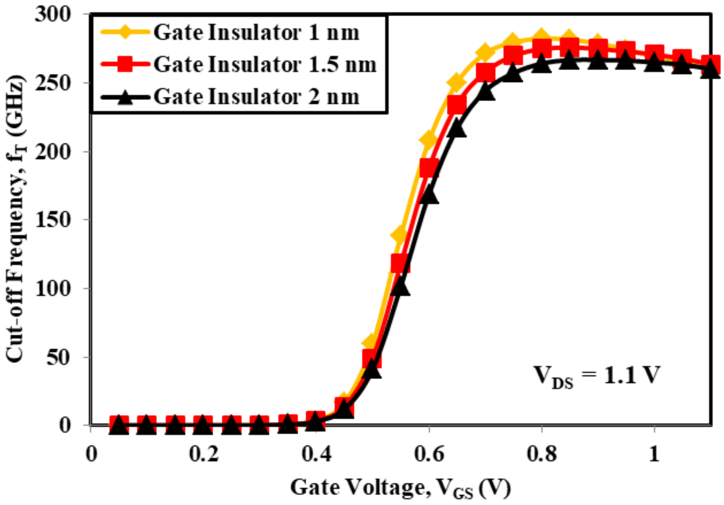


Figure. 16 Cut-off frequency (f_T) Vs. Gate voltage (V_{GS}) of SDMGI for different gate insulator thickness (t_{ox}).

The effect of using high-k material in BOX in SDMGI FDSOI MOSFET is also demonstrated by using same simulation. Figure 17 – Figure 19 shows that on-state drive current, transconductance and f_T gets reduced due to which high dielectric material in BOX is not preferred for high frequency and high speed applications and high-k must not be used in every part of IC design.

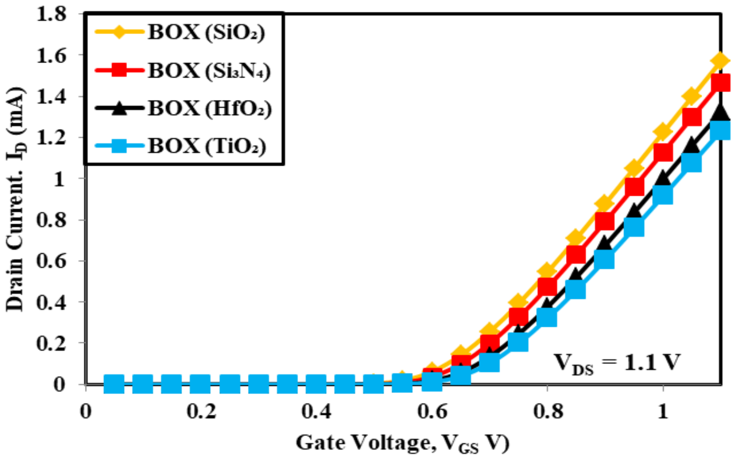


Figure. 17 Transfer Characteristics of SDMGI for different BOX material linear scale.

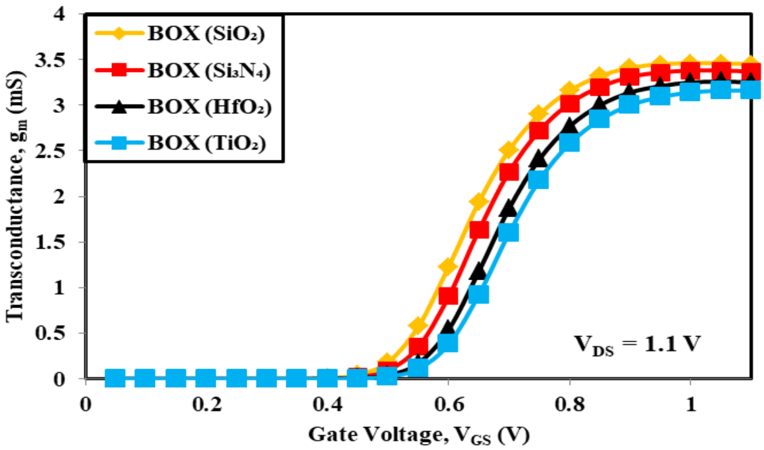


Figure. 18 Transconductance Vs. Gate voltage Characteristics of SDMGI for different BOX material.

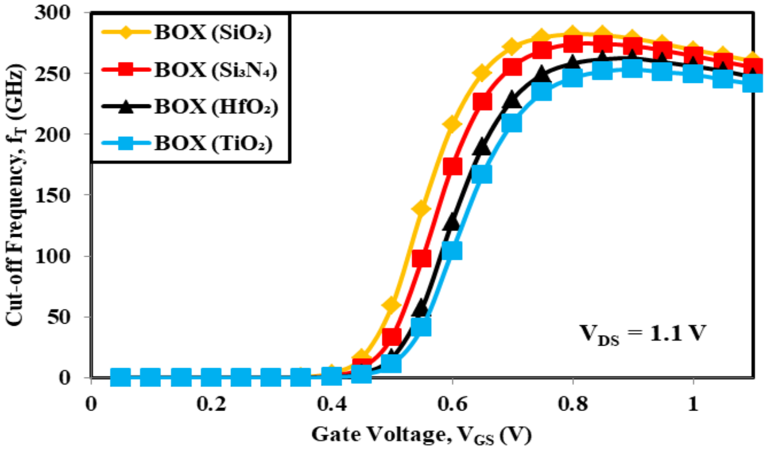


Figure. 19 Cut-off frequency (f_T) Vs. Gate voltage (V_{GS}) characteristics of SDMGI for different BOX material.

The influence on DC, analog and RF performance is analysed when BOX thickness is increased from 5 nm – 12 nm in SDMGI FDSOI MOSFET. S. Mukherjee et al. reported that bandwidth of amplifier increases when buried oxide thickness is increased [25]. It is evident from Figure 20 – Figure 22 that on-state drive current, g_m and f_T goes on increasing as we increase the BOX thickness (t_{BOX}) in SDMGI.

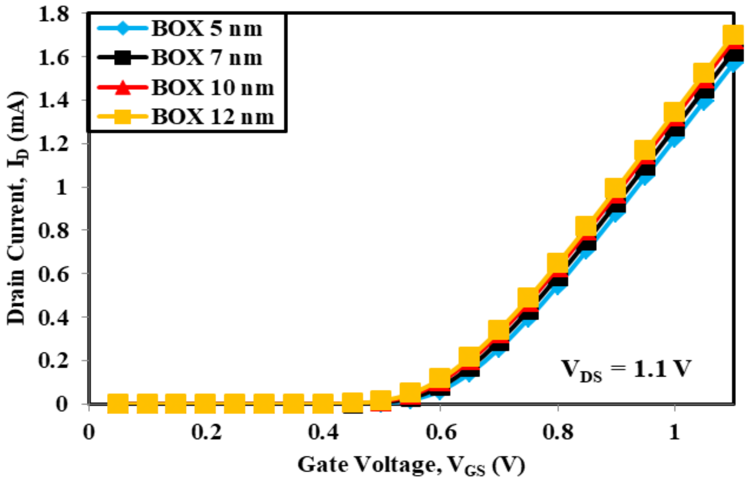


Figure. 20 Transfer Characteristics of SDMGI for different BOX thickness linear scale.

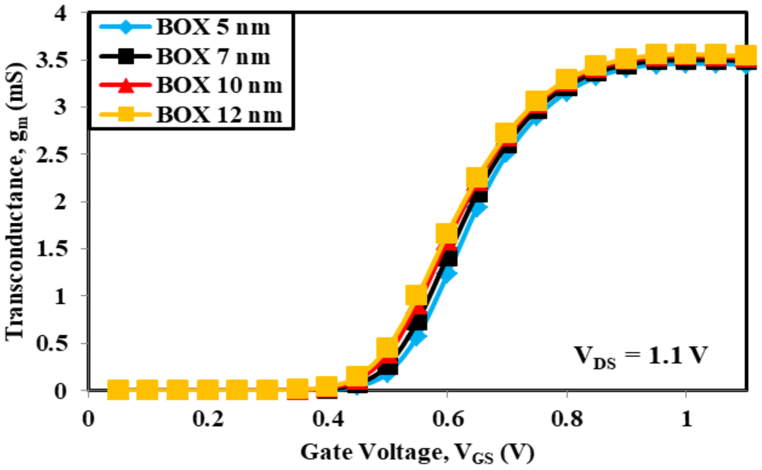


Figure. 21 Transconductance (g_m) Vs. Gate voltage (V_{GS}) characteristics of SDMGI for different BOX thickness.

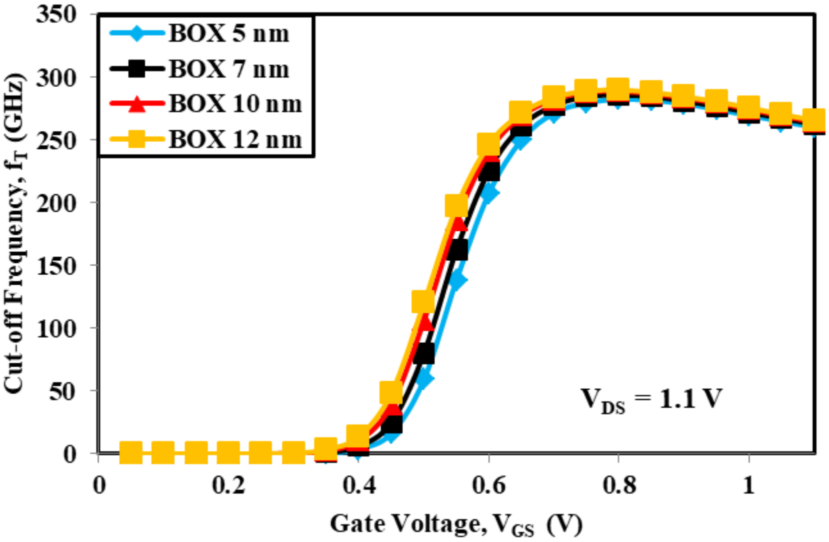


Figure. 22 Cut-off frequency (f_T) Vs. Gate voltage (V_{GS}) characteristics of SDMGI for different BOX thickness.

4. Conclusion

It is found that I_{ON}/I_{OFF} of SDMGI improves by 3.79 times, 90%, 49.78% and 50.43% as compared to conventional, GS, CH-k and ADMGI based MOS structures respectively. Hence, SDMGI is suitable for fast switching applications. For analog and RF performance, g_m, intrinsic gain, f_T, TFP, GFP and GTFP are the key parameters. From the simulation result, it is found that the g_m of SDMGI is raised by 67.14%, 24.01%, 13.44%, 13.44% , the intrinsic gain of SDMGI improves by 3.47 times 3.15 times, 3.12 times, 3.13 times, the f_T of SDMGI improves by 1.07%, 4.26%, 5.22%, 5.71%, the TFP of SDMGI improves by 13.53%, 5.65%, 1%, 2.23%, the GFP of SDMGI improves by 3.28 times, 3.18 times, 3.22 times, 3.24 times and the GTFP of SDMGI improves by 3.21 times, 2.88 times, 2.8 times, 2.82 times as compared to conventional, GS, CH-k and ADMGI based MOS structures respectively. Thus, SDMGI based MOS structure is suitable for high speed and high frequency applications. Further, analog and RF performance of SDMGI FDSOI MOSFET improves on increasing the buried oxide thickness whereas performance degrades when gate oxide thickness is increased and high-k material is used in BOX. So the designed SDMGI FDSOI MOSFET structure is a suitable candidate for fast switching, high speed and high frequency applications.

6. References

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