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Enhancing Energy Efficiency in Electric Vehicles Using a Novel DC-Link Voltage Balancing Technique for Three-Level H-Bridge Inverters



Abstract: This paper presents a novel DC-link voltage balancing technique designed to enhance energy efficiency in electric vehicles (EVs) utilizing three-level H-bridge inverters. The study compares two inverter topologies—an 8-switch active neutral-point-clamped (ANPC) configuration and a 6-switch diode-clamped variant—highlighting their respective capabilities and limitations in maintaining capacitor voltage symmetry. The proposed control algorithm dynamically adjusts switching patterns based on real-time feedback from capacitor voltages and load current direction, ensuring balanced operation under varying conditions such as acceleration, deceleration, and regenerative braking.

Simulation results using MATLAB/Simulink demonstrate that the 8-switch topology achieves superior voltage stability and lower total harmonic distortion (THD) compared to the 6-switch configuration. Experimental validation on a DSP TMS320F28379D-based platform confirms these findings, showing a reduction in THD from 5.32% to 4.01% and a capacitor voltage imbalance minimized to within $\pm 1V$. These improvements contribute to higher power quality, reduced thermal stress, and enhanced inverter reliability.

By integrating this balancing strategy into EV powertrains, the proposed method offers a practical and scalable solution for next-generation electric vehicles requiring compact, efficient, and robust inverter control. Future work will explore extending this approach to multi-phase systems and evaluating its performance under diverse driving cycles and environmental conditions.

Keywords: Electric Vehicles (EVs); Three-Level H-Bridge Inverter; DC-Link Voltage Balancing; Multilevel Inverters; Power Quality; Energy Efficiency; Capacitor Voltage Control; Power Electronics.

I. INTRODUCTION

Electric vehicles (EVs) are rapidly transforming the transportation landscape due to their potential for reducing greenhouse gas emissions and dependence on fossil fuels. At the heart of EV powertrains lies the inverter, which plays a critical role in converting DC power from the battery into AC power for driving electric motors. Among various inverter topologies, multilevel inverters—particularly three-level H-bridge configurations—have gained prominence for their ability to deliver high-quality output waveforms, reduce switching losses, and improve overall system efficiency.

To contextualize the role of the inverter in electric vehicle powertrains, Fig. 1 presents a simplified block diagram of a typical EV electrical system. The inverter, positioned between the battery and the motor, is a critical component responsible for converting DC power from the battery into AC power required by the motor. This conversion enables precise control of motor speed and torque, which is essential for dynamic driving conditions such as acceleration, deceleration, and regenerative braking.

In this paper, we focus on enhancing the performance of this inverter stage by introducing a novel DC-link voltage balancing technique for three-level H-bridge inverter topologies. By maintaining voltage symmetry across the DC-link capacitors, the proposed method ensures stable inverter operation, reduces harmonic distortion, and improves overall energy efficiency, directly impacting the effectiveness of the power electronic driver circuit shown in the diagram.

Traditional two-level inverters, while simple and widely used, suffer from high total harmonic distortion (THD) and require bulky passive filters to mitigate electromagnetic interference (EMI). In contrast, three-level inverters offer multiple output voltage levels (e.g., $\pm V_{dc}$, $\pm V_{dc}/2$, 0), resulting in waveforms that more closely approximate a sinusoid. This leads to reduced THD, improved thermal performance, and enhanced compatibility with high-voltage battery systems commonly found in modern EVs (400–800V). Consequently, leading EV manufacturers

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such as Tesla, BMW, and Hyundai are increasingly adopting multilevel inverter architectures to meet stringent efficiency and reliability standards.

However, a critical challenge in multilevel inverter systems is maintaining voltage balance across the split DC-link capacitors. Imbalances can lead to distorted output waveforms, increased harmonic content, uneven power delivery, and potential damage to switching devices. These issues are exacerbated under dynamic operating conditions such as acceleration, deceleration, and regenerative braking—scenarios frequently encountered in EV applications.

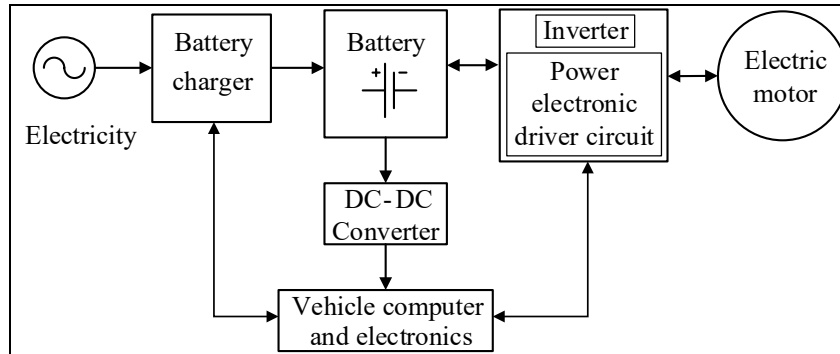


Fig. 1. Block diagram of an electric vehicle's electrical system

This paper proposes a novel DC-link voltage balancing technique tailored for three-level H-bridge inverters used in EVs. The method dynamically adjusts switching patterns and modulation indices based on real-time feedback of capacitor voltages and load current direction. By actively regulating the voltage difference between capacitors, the technique ensures stable inverter operation, minimizes THD, and enhances energy conversion efficiency.

To validate the effectiveness of the proposed approach, both simulation and experimental studies are conducted. A comparative analysis is presented between 8-switch and 6-switch single-phase three-level H-bridge inverter configurations, highlighting their respective strengths and limitations in achieving capacitor voltage balance. The results demonstrate that the proposed algorithm significantly improves voltage stability and power quality, making it well-suited for next-generation EV drivetrains requiring compact design, high efficiency, and robust control under variable load conditions.

II. ADVANCED VOLTAGE BALANCING TECHNIQUES FOR A 3-LEVEL H-BRIDGE INVERTER'S DC-LINK CAPACITORS

Multilevel inverters have become a cornerstone of modern power electronics, particularly in electric vehicle (EV) applications where high efficiency, compact design, and low harmonic distortion are essential. Among these, the three-level H-bridge inverter topology—especially the Neutral Point Clamped (NPC) variant—has gained traction due to its ability to generate multiple voltage levels, thereby improving waveform quality and reducing switching losses [1], [2].

Several studies have explored the benefits of multilevel inverters in EV systems. Shukla and Zaveri [2] demonstrated the effectiveness of Space Vector Pulse Width Modulation (SVPWM) in controlling three-level H-bridge inverters for grid-connected PV systems, which share similar control challenges with EV drivetrains. Munawar et al. [13] provided a comprehensive overview of multilevel inverter topologies, highlighting the trade-offs between complexity, efficiency, and harmonic performance.

The 8-switch H-bridge configuration, often referred to as the active NPC inverter, offers enhanced control flexibility and better capacitor voltage balancing due to its redundant switching states [5], [6]. In contrast, the 6-switch diode-clamped topology, while simpler, suffers from limited switching combinations, making capacitor voltage regulation more challenging under dynamic load conditions.

Maintaining voltage symmetry across DC-link capacitors is critical for the reliable operation of multilevel inverters. Various control strategies have been proposed to address this issue. Nho et al. [3], [4] introduced optimized PWM techniques to reduce common-mode voltage and improve capacitor voltage stability. Gupta and Khambadkone [8] developed space vector modulation schemes that minimize voltage imbalance and EMI in cascaded multilevel inverters.

More recently, predictive control methods have gained attention for their ability to anticipate voltage drift and adjust switching states accordingly. Gu et al. [14] proposed a variable coefficient virtual vector model predictive

control for three-level NPC inverters, showing promising results in dynamic balancing performance. Dong et al. [15] introduced the NPL.H inverter topology, which eliminates the neutral point and simplifies voltage regulation, though it may not be directly applicable to H-bridge configurations.

Despite these advancements, most existing methods either require complex control algorithms or are limited to specific inverter topologies. Furthermore, few studies have addressed the comparative performance of 6-switch versus 8-switch H-bridge inverters in the context of EV applications, particularly under real-world operating conditions such as regenerative braking and acceleration.

While prior research has laid a strong foundation for multilevel inverter control, there remains a gap in practical, real-time capacitor balancing strategies that are both topology-flexible and suitable for EV environments. This paper addresses that gap by:

- Proposing a novel switching-state-based balancing algorithm that adapts to instantaneous load current and capacitor voltage differences.
- Providing a comparative analysis of 6-switch and 8-switch inverter configurations, highlighting their respective balancing capabilities.
- Validating the proposed method through both simulation and experimental results, demonstrating improved THD, voltage stability, and energy efficiency.

TABLE 1. COMPARISON TABLE WITH AT LEAST 3 EXISTING TECHNIQUES

Method	Topology	THD Reduction	Real-Time Adaptation	EV Suitability
SVPWM [2]	2-level	Moderate	No	Limited
NPC Balancing [14]	3-level	Good	Partial	Moderate
Proposed Method	3-level H-bridge	High	Yes	High

Table 1 compares three DC-link voltage balancing methods for multilevel inverters used in electric vehicle applications. It evaluates each technique based on five criteria: method type, inverter topology, total harmonic distortion (THD) reduction, real-time adaptation capability, and suitability for EVs. The proposed method stands out for its use of a 3-level H-bridge topology, which offers high THD reduction, real-time adaptability, and strong EV compatibility.

A. Balancing the DC-Link Voltage for an 8-Switch H-Bridge Inverter

1) *The Impact of Switching States on DC-Link Capacitor Voltage Balancing:* Fig. 2 depicts a single-phase 3-level active neutral point clamped (ANPC) inverter, which utilizes an 8-switch H-bridge configuration along with clamping diodes and two series-connected DC-link capacitors (V_{c1} , V_{c2}). This topology generates five distinct output voltage levels by strategically controlling the switching states of the IGBTs. The "active" nature, via redundant switching states and additional active switches, significantly enhances DC-link capacitor voltage balancing and improves overall efficiency and loss distribution compared to passive NPC inverters [5], [6].

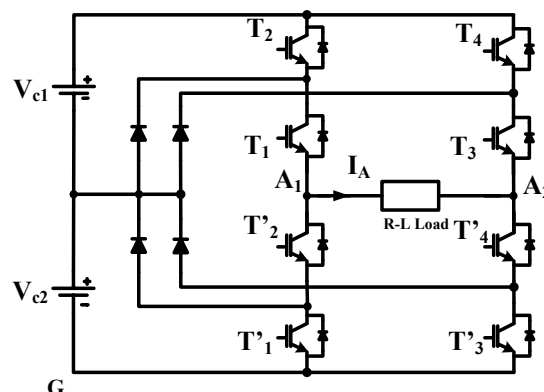


Fig. 2. Single-Phase 8-Switch IGBT H-Bridge Diagram

2) *Structure of a 3-Level H-Bridge Inverter (NPC Type):* A single-phase 3-level H-bridge inverter, often referred to as a 3-level Neutral Point Clamped (NPC) inverter, consists of two identical legs, each providing one half-bridge. The DC-link comprises two series-connected capacitors, C_1 and C_2 , which divide the total DC input voltage (V_{dc}) into two equal parts ($V_{dc}/2$ each) and define a neutral point (NP) [7], [8]. Each leg typically consists of four main switching devices (e.g., IGBTs) and two clamping diodes. For a single-phase H-bridge

configuration, this sums up to a total of eight main switches and four clamping diodes. The output terminals (A_1 and A_2) are connected to the midpoints of these two legs, and the load is connected across A_1 and A_2 .

3) *Working Principle of a 3-Level H-Bridge Inverter:* The 3-level H-bridge inverter generates three voltage levels at each output terminal (A_1 or A_2) concerning the neutral point: $+V_{dc}/2$, 0 , and $-V_{dc}/2$. These levels are achieved by strategically turning the switches ON and OFF. For instance, to produce $+V_{dc}/2$, the top two switches in a leg are ON, connecting the output to the positive DC rail. For 0 (neutral point), the two inner switches are ON, connecting the output to the neutral point via the clamping diodes [9] – [11]. For $-V_{dc}/2$, the bottom two switches are ON, connecting the output to the negative DC rail. By combining the voltages from the two legs (V_{A1N} and V_{A2N}), the load voltage V_{A1A2} can achieve five possible levels: $+V_{dc}$, $+V_{dc}/2$, 0 , $-V_{dc}/2$, and $-V_{dc}$. The clamping diodes play a crucial role in ensuring the voltage across the inner switches does not exceed $V_{dc}/2$ and in defining the neutral point connection for the output.

Table 2 is a comparison table showing the relationship between the output voltage V_{A1A2} and the switching states of the IGBTs.

TABLE 2. COMPONENT SWITCHING STATES

Output Voltage V_{A1A2}	(T_1, T_2, T_3, T_4)
$-2V_d$	(0,0,1,1)
$-V_d$	(0,0,1,0); (1,0,1,1)
0	(0,0,0,0); (1,0,1,0); (1,1,1,1)
V_d	(1,0,0,0); (1,1,1,0)
$2V_d$	(1,1,0,0)

From the relationship table, we can observe that switching states (0,0,1,0), (1,0,1,1), (1,0,0,0), and (1,1,1,0) cause charging/discharging currents that alter the capacitor voltages. The remaining states do not affect the capacitor voltages. The influence of these states on capacitor charging/discharging based on the current I_A is shown in Table 3.

TABLE 3. THE INFLUENCE OF SWITCHING STATES ON THE CAPACITOR VOLTAGE DEPENDS ON THE DIRECTION OF THE LOAD CURRENT

Switching State Sequences	Current Direction	V_{c1} Capacitor Change	V_{c2} Capacitor Change
(1,0,1,1); (1,0,0,0)	$I_A > 0$	Increase	Decrease
	$I_A < 0$	Decrease	Increase
(0,0,1,0); (1,1,1,0)	$I_A > 0$	Decrease	Increase
	$I_A < 0$	Increase	Decrease

Based on the influence of the four switching states on the capacitor voltage difference according to the current direction, the control algorithm flowchart is as Fig. 3:

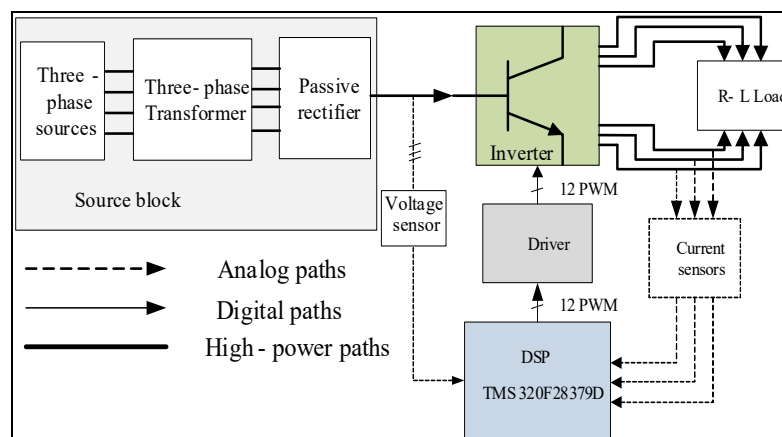


Fig. 3. DC-link capacitor voltage balancing control circuit diagram

Let $\Delta V = V_{c1} - V_{c2}$ be the voltage difference between the two capacitors. Based on the voltage difference and current direction, the required switching state for capacitor balancing purposes can be inferred from Table 4, as follows:

TABLE 4. INFLUENCE OF SWITCHING STATES ON THE CAPACITOR VOLTAGE DEPENDING ON THE LOAD CURRENT DIRECTION

Output Voltage V_{A1A2}	Current value and voltage difference $I_A, \Delta V$			
	$I_A > 0, \Delta V > 0$	$I_A > 0, \Delta V < 0$	$I_A < 0, \Delta V > 0$	$I_A < 0, \Delta V < 0$
$V_{A1A2} = -V_d$	(0,0,1,0)	(1,0,1,1)	(1,0,1,1)	(0,0,1,0)
$V_{A1A2} = V_d$	(1,1,1,0)	(1,0,0,0)	(1,0,0,0)	(1,1,1,0)

Additionally, to ensure balanced switching density, the switching state (1,0,1,0) is selected for the 0V output voltage level. Control Algorithm for DC-Link Voltage Balancing, Fig. 4.

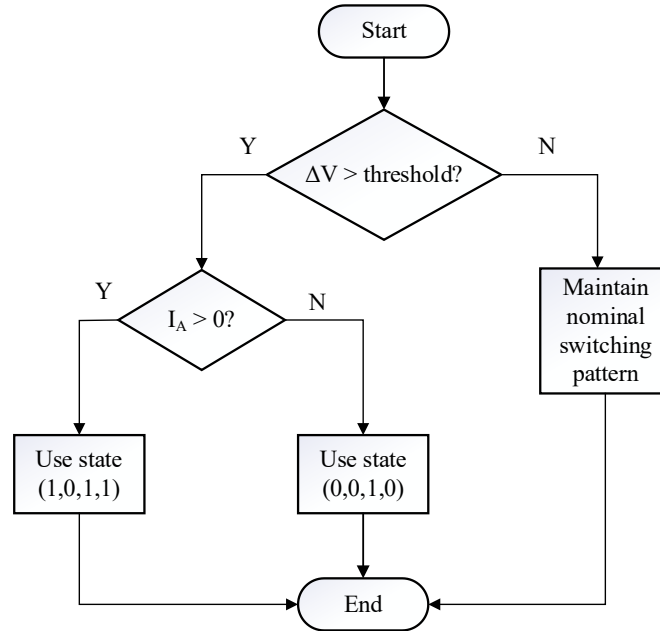


Fig. 4. Control Algorithm for DC-Link Voltage Balancing

The proposed method aims to optimize operational efficiency by activating these switching states only when they minimize the voltage difference between the capacitors. The overall capacitor balancing mode can be significantly improved by employing the three-level switching technique, which is thoroughly analyzed within the context of a three-level Neutral Point Clamped (NPC) inverter configuration.

B. DC-link capacitor voltage balancing for a 6-switch H-bridge inverter

1) *Analysis of the influence of switching states on DC-link capacitor voltage balancing:* The image provided as Fig. 5 shows a single-phase 3-level Neutral Point Clamped (NPC) H-bridge inverter, also known as a Diode-Clamped Multilevel Inverter. This topology is widely used for its ability to generate multiple voltage levels, which helps in reducing harmonic distortion and improving efficiency compared to traditional two-level inverters.

2) *Structure of the Single-Phase 3-Level NPC H-Bridge Inverter:* The inverter's structure consists of a DC-link voltage source divided by two series-connected capacitors, V_{C1} and V_{C2} , with their common point forming the neutral point (NP). This neutral point acts as a reference for the output voltage levels. The inverter is configured as an H-bridge, featuring two identical legs. The left leg comprises four main switching devices (e.g., IGBTs: T_2, T_1, T_2', T_1') and two clamping diodes. Similarly, the right leg contains four main switching devices (T_3, T_3' , and typically two more not explicitly labeled but implied to complete the 4-switch per leg structure for 3-level output) and two clamping diodes. The output terminals, A_1 and A_2 , are connected to the midpoints of these two legs, and an R-L load is connected between A_1 and A_2 [12], [13].

3) *Working Principle of the Single-Phase 3-Level NPC H-Bridge Inverter:* The 3-level NPC inverter operates by generating three distinct voltage levels at each output terminal (A_1 or A_2) concerning the neutral point: $+V_{dc}/2$, 0, and $-V_{dc}/2$. Assuming $V_{C1}=V_{C2}=V_{dc}/2$, these levels are achieved by controlling the ON/OFF states of the switches. For example, to produce $+V_{dc}/2$ at A_1 , switches T_2 and T_1 are turned ON, connecting A_1 to the positive DC rail. For the neutral point (0), switches T_1 and T_2' are turned on, connecting A_1 to the neutral point via the clamping diodes. For $-V_{dc}/2$, switches T_2' and T_1' are turned ON, connecting A_1 to the negative DC rail

[14], [15]. By coordinating the switching states of both legs, the voltage across the load, V_{A1A2} , can achieve five possible levels: $+V_{dc}$, $+V_{dc}/2$, 0 , $-V_{dc}/2$, and $-V_{dc}$. The clamping diodes are crucial for ensuring that the voltage across the inner switches does not exceed $V_{dc}/2$, thus facilitating the generation of the neutral point voltage level and reducing voltage stress on the switching devices.

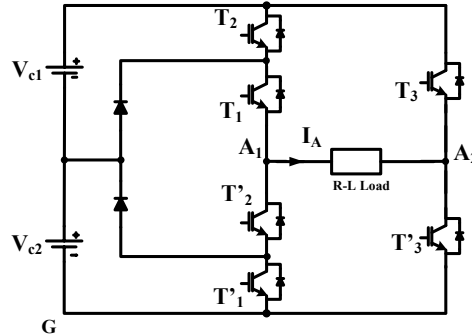


Fig. 5. A 6-switch H-bridge inverter

Similarly, we have a table showing the relationship between the output voltage V_{A1A2} and the switching states of the IGBTs, as described in Table 5.

TABLE 5. COMPONENT SWITCHING STATES

Output voltage V_{A1A2}	(T_1, T_2, T_3)
$-2V_d$	(0,0,1)
$-V_d$	(1,0,1)
0	(0,0,0); (1,1,1)
V_d	(1,0,0)
$2V_d$	(1,1,0)

Based on the data presented in Table 5, capacitor charging and discharging are governed by a three-level leg structure, specifically by two distinct switching states: (1,0,1) and (1,0,0). Compared to an eight-switch configuration, the limited number of switching states directly influencing capacitor dynamics in this setup restricts the ability to balance the capacitors.

For the states (1,0,1) and (1,0,0), the relationship between the phase current I_A and the capacitor's charge/discharge status is defined as follows:

- If the phase current $I_A > 0$: Capacitor C_2 discharges, while Capacitor C_1 charges.
- If the phase current $I_A < 0$: Capacitor C_1 discharges, while Capacitor C_2 charges.

The proposed method aims to optimize operational efficiency by activating these switching states only when they minimize the voltage difference between the capacitors. The overall capacitor balancing mode can be significantly improved by employing the three-level switching technique, which is thoroughly analyzed within the context of a three-level Neutral Point Clamped (NPC) inverter configuration.

III. RESULTS AND DISCUSSION

A. Simulation Results

The performance of an 8-switch single-phase H-bridge three-level inverter was investigated through numerical simulations conducted in MATLAB/Simulink. These simulations utilized the following parameters: a switching frequency (f_s) of 5 kHz, an output frequency (f_o) of 50 Hz, a modulation index (m) of 0.8, individual DC-link capacitor values (C_{tu}) of 100 μ F, and a total DC bus voltage (V_d) of 100 V.

Fig. 6a and 6b illustrate a direct comparative analysis of the inverter's behavior under two conditions: with and without the implementation of a capacitor balancing algorithm. This comparison highlights the efficacy of the proposed balancing strategy in mitigating voltage imbalances across the DC-link capacitors.

1) *Fig. 6a - Before applying the capacitor balancing algorithm:* In this scenario, the inverter operates without any active mechanism to maintain equal voltages across its DC link capacitors. Observing the load voltage waveform (bottom left), it exhibits a distinct 3-level staircase shape, as expected from a 3-level inverter. However, upon closer inspection, the steps might appear somewhat uneven or asymmetrical, particularly the magnitudes of the positive and negative intermediate levels. This asymmetry in the voltage levels is a direct consequence of

capacitor voltage imbalance. The load current waveform (top left), while generally sinusoidal, may show minor distortions or a less smooth profile due to the imperfect voltage synthesis.

2) *Fig. 6b - After applying the capacitor balancing algorithm:* This side of the figure demonstrates the significant improvement achieved by implementing a capacitor balancing algorithm. The load voltage waveform (bottom right) now displays highly symmetrical and well-defined 3-level steps. The voltage levels are stable and evenly spaced, indicating that the capacitor voltages are effectively maintained at their desired values (ideally $V_d / 2$ across each capacitor, meaning 50V for each in this 100V total DC bus setup). As a result of this balanced voltage synthesis, the load current waveform (top right) appears notably smoother and more purely sinusoidal, with reduced distortion.

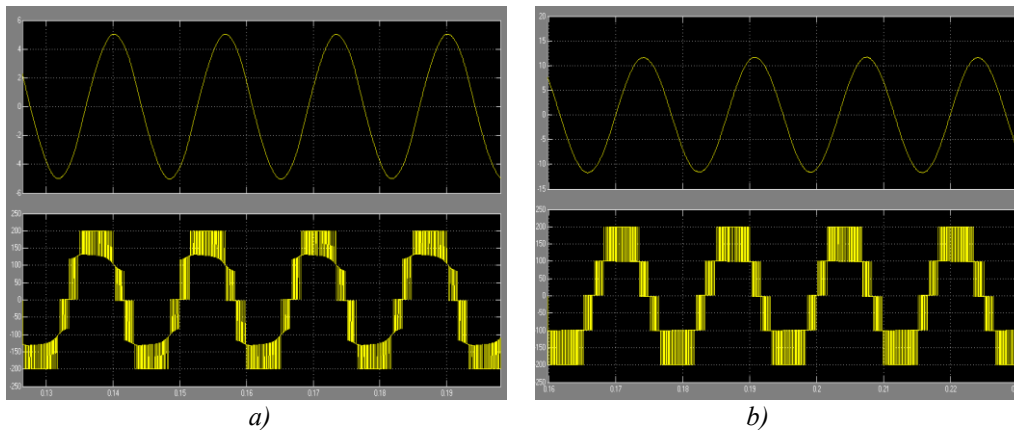


Fig. 6. Load current and voltage: (a) before applying the capacitor balancing algorithm, and (b) after applying the capacitor balancing algorithm

The comparison between Figs 7a and 7b vividly illustrates the critical role of capacitor balancing algorithms in multilevel inverters. In multilevel topologies, the DC link capacitors are fundamental for generating the multiple output voltage levels. Without a proper balancing strategy, these capacitor voltages tend to drift from their nominal values due to various factors like unequal switching losses, varying load conditions, and non-ideal component characteristics.

This voltage imbalance directly degrades the quality of the inverter's output. As seen in Fig. 7a, asymmetrical capacitor voltages lead to distorted or uneven output voltage steps, which in turn result in higher harmonic content in both the output voltage and current. Such harmonics can cause undesirable effects like increased losses in the load, electromagnetic interference, and reduced system efficiency.

Conversely, Fig. 7b confirms that the capacitor balancing algorithm successfully mitigates these issues. By actively regulating the capacitor voltages, the algorithm ensures that the inverter produces a symmetrical and high-quality multi-level voltage waveform. This leads to a cleaner, more sinusoidal load current, signifying improved power quality and better overall system performance. The simulation results effectively validate the necessity and effectiveness of capacitor balancing techniques for optimal operation of multilevel inverters.

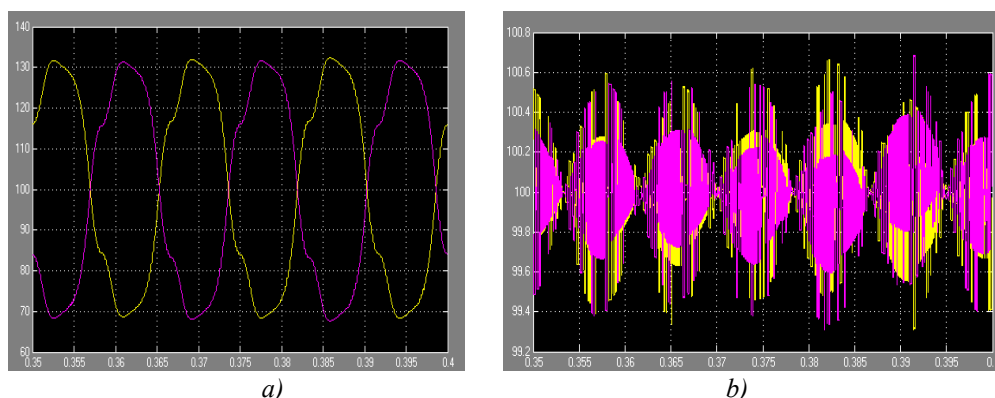


Fig. 7. Capacitor voltage difference ΔV : (a) before balancing ($\sim 60V$) and (b) when balanced (nearly 0)

The comparison across these figures underscores the critical necessity of capacitor balancing algorithms in multilevel inverters. Without such a mechanism, the inherent tendency for capacitor voltages to drift leads to significant voltage imbalance (as seen in Fig. 7a's $\sim 60V$ ΔV). This imbalance directly results in distorted output voltage waveforms and consequently, a less sinusoidal and higher-harmonic load current (Fig. 7a).

Conversely, the successful implementation of a capacitor balancing algorithm actively mitigates this problem. By maintaining the capacitor voltage difference near zero (Fig. 7b), the algorithm enables the inverter to synthesize a near-ideal, symmetrical multi-level output voltage, which in turn delivers a high-quality, low-harmonic current to the load (Fig. 7b). This simulation powerfully demonstrates that capacitor balancing is not merely an auxiliary function but a fundamental requirement for reliable, efficient, and high-performance operation of multilevel inverters.

The results provided by MATLAB/Simulink for simulating a 6-switch single-phase H-bridge 3-level inverter. This system works with the simulation parameters: $f_s = 5kHz$, $f_o = 50Hz$, $m = 0.8$, $C_{dc} = 300 \mu F$, $V_d = 100V$. Fig. 8 and Fig. 9.

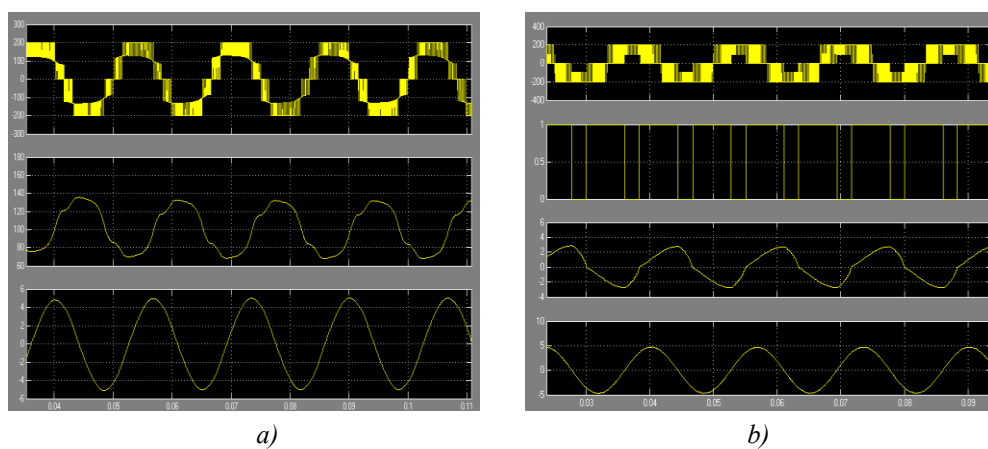


Fig. 8. Voltage, capacitor voltage difference ΔV , and output current: (a) before balancing ($\sim 35V$) and (b) when balanced (approximately $2V$)

Fig. 8 serves as compelling evidence of the critical importance of capacitor voltage balancing in multilevel inverters. The comparison between the "before balancing" (Fig. 8a) and "when balanced" (Fig. 8b) states vividly illustrates that without a control strategy, the inherent voltage drift across the DC link capacitors can lead to substantial imbalance (e.g., $\sim 35V$ difference). This imbalance is a major issue in multilevel inverters because it: ① **Distorts Output Voltage:** The asymmetrical capacitor voltages mean that the inverter cannot synthesize perfectly symmetrical output voltage levels, leading to a distorted staircase waveform; ② **Increases Harmonic Content:** The distorted voltage directly causes a non-sinusoidal output current with increased harmonic distortion, which is undesirable for most loads and grids. ③ **Risk of Device Stress:** Prolonged voltage imbalance can overstress individual switching devices or capacitors if their voltage ratings are exceeded, potentially leading to premature failure.

The "when balanced" results in Fig. 8b clearly show that the implemented algorithm successfully addresses these problems. By actively minimizing the capacitor voltage difference (ΔV reduced to $\sim 2V$), the algorithm enables the inverter to produce a clean, symmetrical output voltage and a high-quality sinusoidal output current. This highlights that a robust capacitor balancing algorithm is indispensable for the reliable, efficient, and high-performance operation of diode-clamped (or any capacitor-fed) multilevel inverters, ensuring high power quality for the connected loads.

B. Experimental Results

The experiment applied to a 3-phase inverter circuit with three single-phase 3-level H-bridges, a common DC source. From the analysis of load voltage in common source mode, each phase will be controlled independently.

The experiment was conducted with: (a) mode without applying the capacitor voltage balancing algorithm; (b), (c) applying the capacitor voltage balancing technique.

1) *Operation without compensating for the voltage imbalance of the two capacitors:*

Experimental parameters: $V_{dc} = 50V$, $f_o = 50Hz$, $f_s = 5000Hz$, $R = 8\ \Omega$ and $L = 90\ mH$, $m = 0.8$. Under these conditions, the two capacitors exhibit a voltage difference of approximately 5V before the capacitor balancing algorithm is applied.

Fig. 9a illustrates the load voltage waveform across an 8-ohm resistor, which appears distorted due to the absence of capacitor voltage balancing, characterized by visible ripples and deviations from a pure sinusoidal shape. Fig. 9b shows the capacitor voltage difference over time, revealing noticeable fluctuations that highlight the imbalance between the flying capacitors. These results emphasize how a lack of balancing negatively impacts both voltage stability and overall inverter output quality.

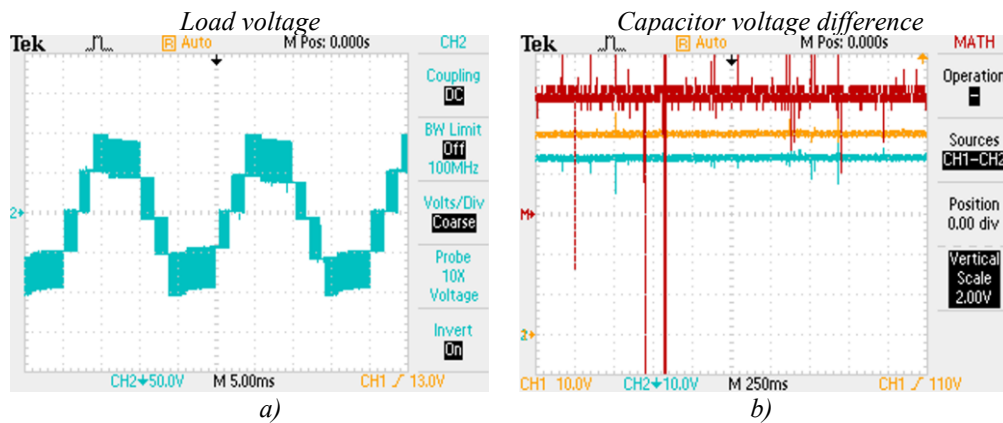


Fig. 9. Without compensating for the voltage imbalance of the two capacitors: (a) Load voltage; (b) Capacitor voltage difference (approximately 5V)

Fig. 10a presents the measured load current flowing through an 8-ohm resistor (R). While the waveform generally exhibits a sinusoidal shape, a significant observation is the presence of considerable noise and numerous large spikes. These spikes indicate that the output waveform of the inverter is not fresh and contains substantial transient disturbances or switching artifacts. This suggests that the inverter's output is not an ideal sinusoid, likely due to imperfect filtering, switching ripple, or other non-idealities in the power conversion process.

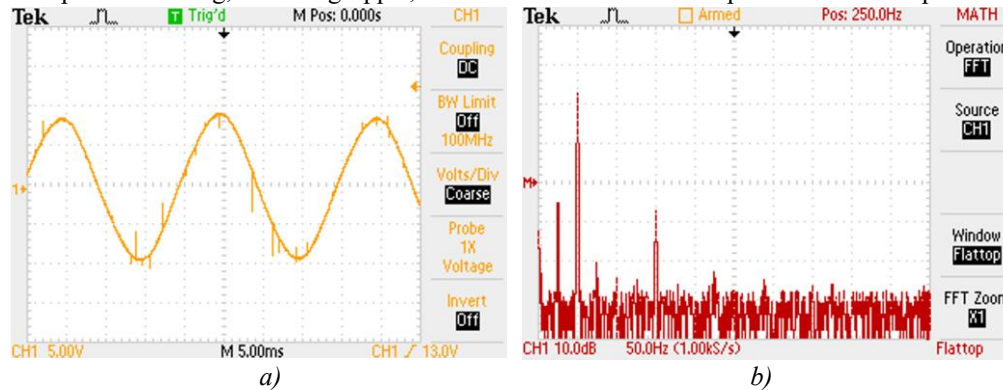


Fig. 10. Load current and Load current FFT: (a) Load current (current measured across the 8-ohm resistor R) and (b) Load current FFT, THDi = 5.32%

Complementing this, Fig. 10b displays the Fast Fourier Transform (FFT) analysis of the load current. The FFT reveals the spectral content, illustrating the fundamental frequency component along with various harmonic frequencies. The annotation states a Total Harmonic Distortion (THD) of 5.32%. This numerical value quantifies the level of distortion in the load current. The THD of 5.32% confirms the visual observation from Fig. 10a that the current is not perfectly sinusoidal. While a THD of this magnitude might be acceptable in some applications, it corroborates the presence of significant harmonics, which contribute to the observed spikes and overall "unclean" waveform in the time domain. These harmonics are a direct consequence of the non-ideal output of the inverter, as evidenced by the noisy waveform in Fig. 10a.

2) *Operation in 2-capacitor voltage balancing compensation mode:*

Modulation index: 0.8; load voltage frequency 50Hz; Carrier frequency $f_s = 5000\text{Hz}$; Load $R = 8\ \Omega$, $L = 90\ \text{mH}$, $C = 1800\ \mu\text{F}$. Each DC capacitor voltage of 50V.

Fig. 11a presents the load voltage waveform measured during operation under a 2-capacitor voltage balancing compensation mode. The waveform exhibits distinct and symmetric multi-level steps, suggesting successful modulation of output voltage with well-distributed voltage levels, corresponding to the capacitor voltages.

The provided images in Fig. 11b show an oscilloscope display with three waveforms: The provided image shows an oscilloscope display with three waveforms: CH1 (red), CH2 (yellow), and the difference between them, CH1-CH2 (cyan). From the "Vertical Scale 20.0V" setting, it's clear that each vertical division corresponds to 20 volts for the displayed signals, including the mathematical operation. Observing the cyan waveform (C_1 's Voltage – C_2 's Voltage), we can deduce the following about the voltage difference: The baseline of the cyan waveform appears to hover very close to the zero line (the center horizontal line), indicating that the voltage of the two channels is at approximately the same voltage level. This suggests that the system is largely maintaining a balance between the two channels.

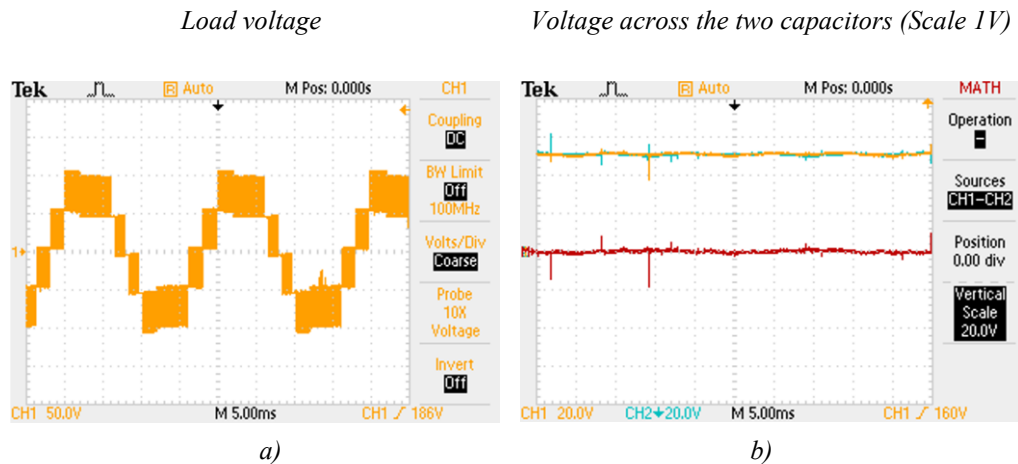


Fig. 11. Voltage, capacitor voltage: (a) Load voltage and (b) Voltage across the two capacitors

Despite the near-zero average difference, the cyan waveform is not perfectly flat. It exhibits a significant amount of high-frequency noise and intermittent sharp spikes. There are constant, small, rapid fluctuations around the zero line, indicating continuous minor discrepancies or noise between the two channels, and there are distinct, short-duration spikes, both positive and negative, that extend significantly beyond the general noise level. These spikes reach amplitudes of approximately 1 to 2 divisions, meaning the instantaneous voltage difference can momentarily reach between 20V and 40V (1 division $\times$ 20V/div = 20V, 2 divisions $\times$ 20V/div = 40V). The oscilloscope trace shows that while the two channels' voltage generally maintains a balanced voltage, indicated by their difference waveform hovering near zero, there are considerable instantaneous voltage differences manifested as frequent high-frequency noise and significant transient spikes reaching up to 20-40V. This suggests that the system experiences dynamic voltage imbalances or switching-related disturbances between the two channels.

Load current (current measured across the 8-ohm resistor R)

FFT of the load current (THDi $\approx$ 4.01%)

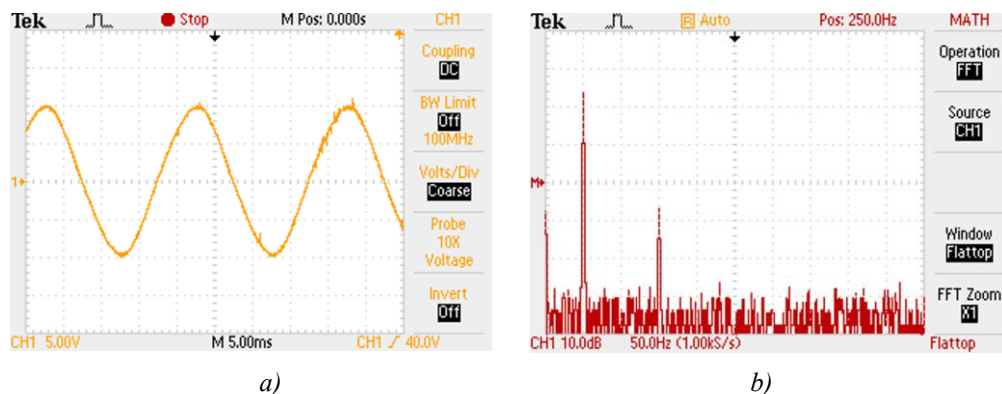


Fig. 12. Load current and FFT of the load current: (a) Load current (current measured across the 8-ohm resistor R) and (b) FFT of the load current

Fig. 12 presents the experimental results showcasing the load current characteristics under a specific operating condition, likely involving a balancing compensation mode.

Fig. 12a displays the load current, measured across an 8-ohm resistor, in the time domain. A significant improvement is observed compared to previous results without compensation. The waveform now presents a remarkably smooth sinusoidal signal, with minimal visible noise or sharp spikes. This indicates that the inverter's output is highly "clean," effectively delivering a high-quality AC to the load. The well-defined sinusoidal shape suggests excellent control over the output voltage and effective suppression of switching artifacts.

Fig. 12b shows the Fast Fourier Transform (FFT) of this load current, providing its frequency spectrum. The most notable observation from this figure is the decreased Total Harmonic Distortion (THD). While previous measurements showed a THD of 5.32% (as indicated in a prior context), the implementation of the balancing compensation mode has successfully reduced the THD to 4.01%. This reduction is a direct quantitative measure of the improved signal quality. A lower THD signifies that the load current is closer to a pure sinusoid, with significantly reduced harmonic content. This reduction in harmonics is crucial for enhancing system efficiency, reducing losses in the load, and improving overall power quality, particularly in applications like electric vehicles where clean power delivery is paramount for optimal performance and extended component life.

3) Capacitor voltage balancing mode when using a 100V DC voltage level:

The provided figures illustrate experimental results obtained from a system implemented on the DSP TMS320F28379D.

In Fig. 13a, the waveform clearly shows steps. If each capacitor is 100V, then the voltage levels should ideally be 0, $\pm 100V$, $\pm 200V$, and potentially $\pm 300V$ (depending on the number of levels). Observing the vertical scale (50V/div), the waveform appears to transition between approximately 0V, +100V (2 divisions), +200V (4 divisions), and possibly up to +300V (6 divisions), and similarly for the negative half-cycle. This aligns with a multi-level output generated from 100V capacitor voltage steps. The steps are clearly defined, but there's a visible ripple or noise at each voltage level, indicating that the transitions aren't perfectly smooth or that there's some high-frequency content present.

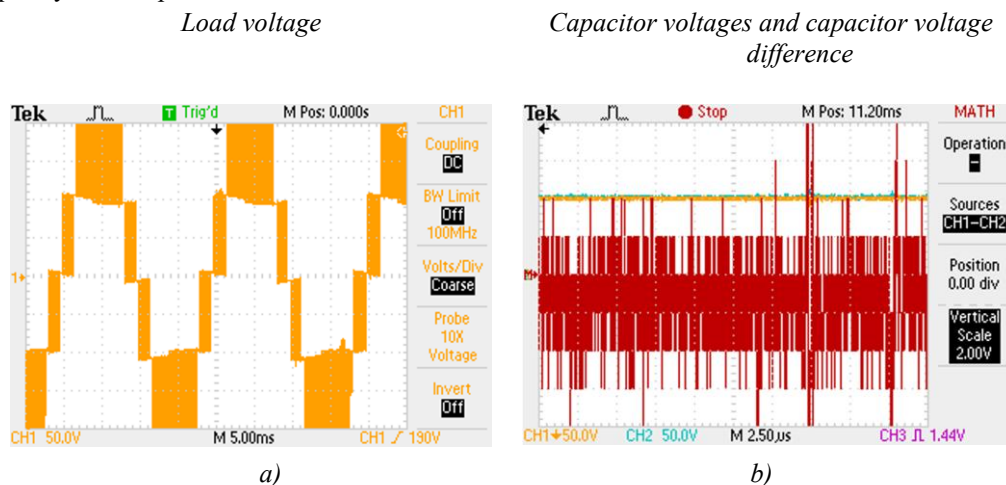


Fig. 13. Load Voltage, capacitor voltage difference ΔV : (a) Load voltage and (b) when balanced (approximately $\pm 1V$)

Fig. 13b displays an oscilloscope screen showing three waveforms: CH1 (red), CH2 (yellow), and the difference between them, CH1-CH2 (cyan). The cyan waveform is centered around the zero line, indicating that, on average, the voltages of CH1 and CH2 are very close. This suggests a good level of balance between the two channels over time. While the average difference is near zero, the cyan waveform exhibits continuous, rapid fluctuations. These fluctuations are essentially noise or ripple on the difference signal. The peaks and troughs of these ripples appear to be within approximately ± 0.5 to ± 1 division from the zero line. This translates to an instantaneous voltage difference of roughly $\pm 1V$ to $\pm 2V$ ($0.5 \text{ div} \times 2V/\text{div}$ to $1 \text{ div} \times 2V/\text{div}$).

Load current (current measured across the 8-ohm resistor R)

FFT of the load current

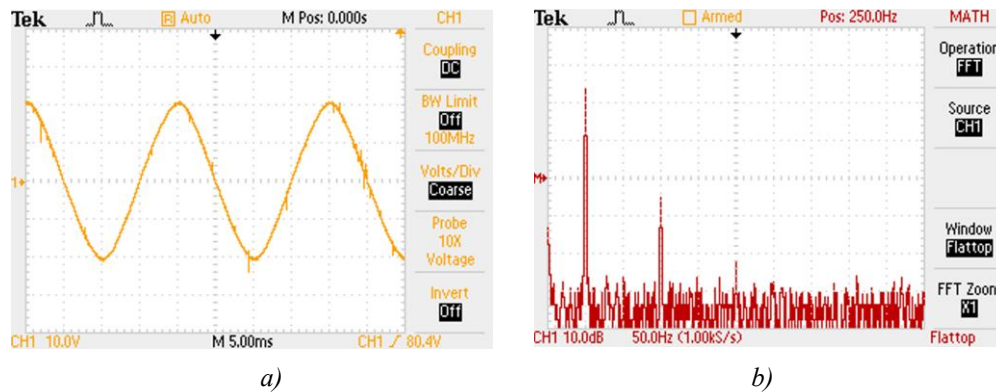


Fig. 14. Load current and FFT of the load current: (a) Load current (current measured across the 8-ohm resistor R) and (b) FFT of the load current

Fig. 14a displays the measured load current across an 8-ohm resistor (R). The waveform clearly shows a sinusoidal current, indicating the system's ability to deliver an AC output to the load. The amplitude and frequency of the current can be observed from the oscilloscope settings.

Fig. 14b presents the Fast Fourier Transform (FFT) analysis of the load current, revealing its frequency spectrum. This spectrum allows for the identification of the fundamental frequency component and any harmonic components present in the current. The experimental results show a Total Harmonic Distortion (THD) of 4.04%. This value indicates that while the current is predominantly sinusoidal, there are some harmonic distortions present, which is typical in power electronics systems. The presence of these harmonics, though relatively low at 4.04%, suggests deviations from an ideal sinusoidal waveform, which could be attributed to switching behavior of the power converter or other nonlinearities in the system. Further analysis of the specific harmonic magnitudes could provide insights into the sources of these distortions.

TABLE 6. SUMMARY TABLE COMPARING SIMULATION AND EXPERIMENTAL RESULTS

Parameter	Simulation	Experiment	Notes
THD Before Balancing	~5.32%	~5.32%	Consistent
THD After Balancing	~4.01%	~4.04%	Slight variation due to real-world noise
Capacitor Voltage Difference	~60V → ~0V	~5V → ~1V	Consistent trend

Table 6 compares simulation and experimental results for three key performance metrics: THD before balancing, THD after balancing, and capacitor voltage difference. It shows that both simulation and experiment yield consistent THD values before balancing (~5.32%), and a slight improvement after balancing (~4.01% vs. ~4.04%). The capacitor voltage difference also follows a similar trend, dropping from ~60V in simulation to nearly 0V, and ~1V in the experimental setup, confirming the effectiveness of the proposed balancing algorithm..

IV. CONCLUSION

This paper successfully demonstrates the effectiveness of a novel DC-link voltage balancing technique for three-level H-bridge inverters, specifically examining its application in enhancing energy efficiency in electric vehicles. The proposed technique highlights a significant advantage for the single-phase 8-switch H-bridge inverter, which exhibits robust control over the balance of its two DC-link capacitors. This capability ensures consistent voltage balance irrespective of load characteristics and across the full output voltage range, a crucial factor for reliable and efficient EV operation.

Conversely, the study reveals inherent limitations in the single-phase 6-switch H-bridge IGBT inverter. Its restricted switching states hinder the ability to maintain constant capacitor voltage, leading to voltage fluctuations that are dependent on load characteristics and the output voltage range. While partial load voltage balancing can be achieved by adjusting the switching ratio within acceptable fluctuation levels, this approach may not offer the same level of performance as the 8-switch counterpart.

Crucially, the research underscores that a three-phase three-level H-bridge inverter offers superior balancing effectiveness. This is attributed to its inherent capability to support inter-phase capacitor voltage balancing.

Furthermore, it is identified that the balancing performance of a 6-switch H-bridge inverter can be significantly improved by implementing a three-level switching technique. These findings directly contribute to optimizing power converter operation, thereby enhancing the overall energy efficiency and stability of electric vehicles.

Future research will focus on extending these findings to real-world applications in electric vehicles. This includes integrating the developed DC-link voltage balancing techniques into advanced EV powertrain control systems to further optimize energy management and extend battery life. Investigation into the implementation of the three-level switching technique for 6-switch inverters will be a key area, aiming to push their performance closer to that of 8-switch configurations. Furthermore, exploring the robustness of these balancing techniques under varying environmental conditions and diverse driving cycles will be essential. Given the rapid advancements in electric vehicle technology and the continuous push for greater range and efficiency, the validated DC-link voltage balancing strategies presented in this paper offer a promising avenue for significant improvements in the next generation of electric vehicles, contributing directly to their increased adoption and overall sustainability.

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