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**Regular paper**

# DBSCAN Based inductively coupled DSTATCOM for PQ improvement

This research study explains the feasibility of implementing machine learning (ML) oriented inductively coupled distributed static compensator (IC-DSTATCOM) for power quality (PQ) enhancement. The issue involved in declining the power quality (PQ) using direct coupled static compensator (DC-DSTATCOM) was identified as a hazardous disappointment. Hence, to improve the quality, coupling transformer is served in unification with DC-DSTATCOM. Also, the recent growth of machine learning (ML) systems and progression of computational resources, with unpredicted data obtainability, has inspired the researchers. In this study, density based spatial clustering of application with noise (DBSCAN) is employed by using its own learning mechanism (LM) using MATLAB/ Simulink. This controller contains six subnets. Among them, six subnets are employed for active tuned weight extraction whereas other three subnets are used for reactive part. Moreover, the abovesaid devices are triggered with the help of generated reference supply current. A case education is reviewed in detail to demonstrate the operation of both DC-DSTATCOM & IC-DSTATCOM. Finally, the IC-DSTATCOM is amplified healthier as compared to other in terms of harmonics shortening, upgrading in power factor, load balancing, and potential regulation etc. To examine the effectiveness, simulation outputs of the IC- DSTATCOM is presented by following the benchmark measure of IEEE-2030-7-2017 and IEC- 61000-1 grid code**.**

Keywords: DC-DSTATCOM, IC-DSTATCOM, DBSCAN control algorithm, and PQ.

## 1. Introduction

The prime objective of the EPDS based on the present situation is to provide secure, reliable, quality, efficient and economical source of electrical energy the consumers. As a resut, the EPDS must be appropriately planned, designed, and operated in a safe manner. EPDS is generally prone to a greater number of faults/disturbances during operation [1-3]. Increased electrical power needs, a lack of long-term planning, open access to consumers, a minimum level of security, nonlinear loads, and unexpected load switching are all contributing factors to deteriorating supply quality. As a result, power system operators require innovative strategies for increasing PQ performance [4-6].

The DSTATCOM is an important choice for current PQ concerns because of this incentive to improve PQ performance in the EPDS [7-9]. Despite the fact that DSTATCOM plays an important part in the EPDS, diversification of the DSTATCOM is becoming a rising role for the modern EPDS. As a result, the difficult issue is to provide flexibility and long-term viability for all of the above possibilities. Important voltage source inverter (VSI) selection, VSI extension, control algorithm design, IFCT design, and impedance matching are the primary study areas for PQ improvement.

For the past three decades, most academics and R&D firms have worked on various custom power devices (CPD) to alleviate PQ-related issues [15-18]. All CPDs inject reactive power at the system's point of common coupling (PCC) in a flexible, reliable, and rapid manner. Because the PCC is in close contact with the source, load, and DSTATCOM in DC-DSTATCOM, it is subjected to additional stress. As a result, there are increased

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opportunities for short circuit currents to flow, insufficient protection, and thermal losses, among other things [12].
To solve the shortcomings of DC-DSTATCOM, a new step must be made. As a result, the research direction is encouraged to move forward with a corrective approach based on IFCT. First and foremost, the design of DC-DSTATCOM for EPDS is the subject of this paper. Later, with DC-DSTATCOM, the IFCT is introduced to act as an inductive medium between the source and the load. It has a variety of advantages, including reduced switching stress, improved PCC balancing voltage, increased compensation capabilities, and other conceivable combinations. For three phase three wire (3P3W) EPDS, two level voltage source converters are considered due to the design element of the DSTATCOM [19-21]. Due of its popularity in the literature study, this three-leg VSI topology is widely advocated. The proposed architecture allows for future flexibility in terms of adding more converters and loads.
Traditional high-voltage transmission line monitoring systems focus entirely on AC measurements via voltage transformers (VTs) and current transformers (CTs), ignoring the DC components flowing on transmission lines. Other sources of harmonics in electrical grids, such as nonlinear loads or overloading transformers, may also cause harmonics to flow in the grid. Most of data are constantly collected from many sections of the power system. ML is a powerful mathematical method for analysing this data and offering useful insights to system operatives so they may make quick and efficient judgements [22-24].
Power and energy systems are one of the most promising segments, with a massive quantity of underutilised data. The available datasets can be used to analyse a variety of power system planning, operation, monitoring, and economics problems. Power grids are complex nonlinear arrangements, and cutting-edge machine learning tools can aid in the analysis and modelling of their behaviour [10-11].
Due to a lack of data and computational power in previous decades, machine learning (ML) did not gain widespread use in the business. Many practical uses of machine learning in power systems are now possible thanks to recent advances in computing technology and the distribution of improved metre infrastructures, phasor measurement units, and micro-PMU. Load prediction, skilful islanding, power system irregularity detection, security assessment, optimal power flow (OPF), fault detection, demand response, customer modelling, improving grid resiliency, and detecting frequency events are just a few of the ongoing and promising applications of machine learning [13-14].

The filtering mechanism of DSTATCOM is carried out utilising a broader mathematical approach and the DBSCAN algorithm in MATLAB/ Simulink for a healthier functioning. According on the benchmark value of the IEEE-2030-7-2017 and IEC-61000-1 grid codes, the following observations can be drawn from the proposed IC-DSTATCOM method [24-26].

- It is possible to achieve good convergence results.
- This algorithm's main features are enhanced tracking, compensatory and adaptive capabilities.
- The suggested approach enables many PQ problems, such as harmonic drop, improved potential control, healthy power factor, output load balancing, and lower DC link voltage, among others.
- It also has a flexible harmonics over current protection feature.
- It has the ability to reorganise more parameters for a better algorithm version.

The preceding section covers the case studies literature review. Section 2 delves into the specifics of circuit configuration and modelling for both DC-DSTATCOM and IC-

DSTATCOM. Modeling and design of IFCT are covered in Section 3. Section 4 contains the system structure, as well as the DBSCAN method and the MATLAB/Simulink platform. Section 5 contains the findings of the comparative simulations. Finally, section 6 summarises the system's effectiveness.

## 2. Modeling of the proposed ic-dstatcom

The arrangement of the 3P3W EPDS with DC-DSTATCOM and IC-DSTATCOM are exposed in Fig.1 & 2 respectively. The DC-DSTATCOM which contains of balanced 3-ϕ supply, DSTATCOM, 3-ϕ non-linear load (uncontrolled rectifier with resistive and inductive loading is maintained), whereas the IC-DSTATCOM which contains of a balanced 3-ϕ supply, converter transformer DSTATCOM, 3-ϕ non-linear load. The VSI based DSTATCOM linked at point of common coupling (PCC) of EPDS is exposed in Fig.3. A customized methodology of self supported capacitor based DC-DSTATCOM & IC-DSTATCOM are used as a compensator to diminish the PQ difficulties. The switching pulses for the IGBTs of the both compensators are produced by using DBSCAN control technique

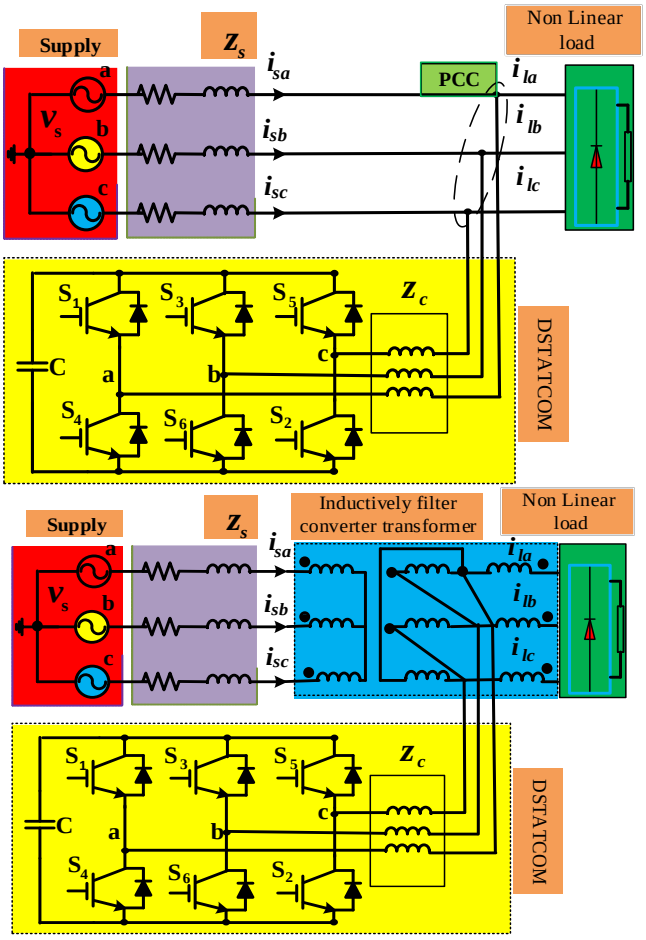



Fig.1EPDS with DC- DSTATCOMFig.2EPDS with IC- DSTATCOM

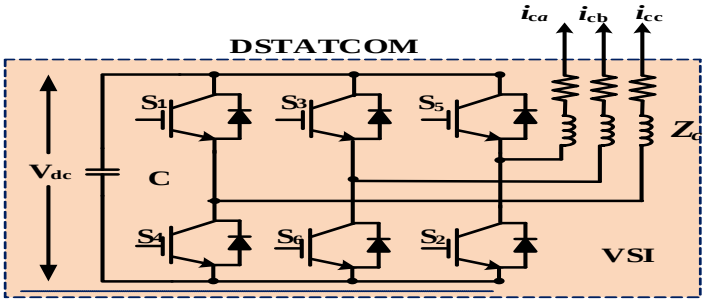



Fig.3 Two-level self-supported capacitor supported VSI based DSTATCOM

The prime agenda of this research is to select the scrupulous outline by using DBSCAN control topology.

## 3. Novelties of the proposed topology

There are numerous novelties of the proposed methodology over DC- DSTATCOM, which is enlightened below :

- *Response and reaction time:* The proposed DSTATCOM possesses better response and reaction time.
- *Component extraction:* the proposed method has the capability to extract demanded time domain component for both harmonics and inter harmonics.
- *Reduced computation time:*This technique is designed to fit parallel processing structure for each time domain component to reduce the computation time.
- *Dynamic operation of inverter*: AS VSC is operated by DBSCAN algorithm, the Hysteresis current controller (HCC) processes the Analog signal to convert in to digital signals for the generation of the firing pulses for different loading scenarios.
- *Increase in system efficiency:* The system efficiency is increased due to less iteration process is involved in the DBSCAN algorithm.
- *Discount in THD of the source current:* The THD of the supply and output load current are 2.94% and 26.69% correspondingly obtained from IC-DSTATCOM. Whereas, the THD of the supply and output load current are 4.00% and 26.32% correspondingly gained from DC-DSTATCOM.

## 4. Modelling and design of inductive transformer

The detailed winding structure of the proposed IC-DSTATCOM is exposed in Fig. 2. The proposed IC-DSTATCOM configures inductively filter converting transformer (IFCT), DSTATCOM containing voltage source inverter (VSI) and nonlinear load. The IFCT structure covers three windings over which DC-DSTATCOM and nonlinear load are joined. In three windings, the primary winding (PW) in star construction connected to grid, secondary side winding (SW) in star construction connected to non-linear load, and the filtering winding (FW) in delta construction is connected to DC-DSTATCOM. The special winding IFCT is to achieve the balanced potential among grid, load, DSTATCOM. That is to say the harmonics are inaccessible from the PW. The detailed accurate model of the IFCT and filtering system are discussed in the later sub-modules.

$$\begin{cases} N_1 \mathrm{i_{ap}} + N_2 \mathrm{i_{as}} + N_3 \mathrm{i_{af}} = 0 \\ N_1 \mathrm{i_{bp}} + N_2 \mathrm{i_{bs}} + N_3 \mathrm{i_{bf}} = 0 \\ N_1 \mathrm{i_{cp}} + N_2 \mathrm{i_{cs}} + N_3 \mathrm{i_{cf}} = 0 \end{cases} \quad (1)$$

$$\begin{cases} \begin{cases} \mathrm{i_{ap}} = \dfrac{u_{sa} - u_{apo}}{Z_{line}} \\ \mathrm{i_{bp}} = \dfrac{u_{sb} - u_{bpo}}{Z_{line}} \\ \mathrm{i_{cp}} = \dfrac{u_{sc} - u_{cpo}}{Z_{line}} \end{cases} & \begin{cases} \mathrm{i_{as}} = i_{al} + i_{zal} \\ \mathrm{i_{bs}} = i_{bl} + i_{zbl} \\ \mathrm{i_{cs}} = i_{cl} + i_{zcl} \end{cases} \\ \begin{cases} \mathrm{i_{ap}} + i_{bp} + i_{cp} = 0 \\ \mathrm{i_{as}} + i_{bs} + i_{cs} = 0 \\ \mathrm{i_{af}} + i_{bf} + i_{cf} = 0 \end{cases} & \begin{cases} \mathrm{i_{af}} = i_{cf} + i_{cat} = i_{cf} + i_{ra} + i_{za} \\ \mathrm{i_{bf}} = i_{af} + i_{cbt} = i_{af} + i_{rb} + i_{zb} \\ \mathrm{i_{cf}} = i_{bf} + i_{cct} = i_{bf} + i_{rc} + i_{zc} \end{cases} \end{cases} \quad (2)$$

$$\begin{cases} \mathrm{u_{abf}} = (i_{zb} - i_{za})/Z_o \\ \mathrm{u_{bcf}} = (i_{zc} - i_{zb})/Z_o \\ \mathrm{u_{caf}} = (i_{za} - i_{zc})/Z_o \end{cases} \quad (3)$$

$$\begin{cases} \mathrm{u_{apo}} - \dfrac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{u_{abf}} = \mathrm{i_{ap}} \mathrm{z_p} - \dfrac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{i_{af}} \mathrm{z_f} \\ \mathrm{u_{bpo}} - \dfrac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{u_{bcf}} = \mathrm{i_{bp}} \mathrm{z_p} - \dfrac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{i_{bf}} \mathrm{z_f} \\ \mathrm{u_{cpo}} - \dfrac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{u_{caf}} = \mathrm{i_{cp}} \mathrm{z_p} - \dfrac{\mathrm{N_1}}{\mathrm{N_3}} \mathrm{i_{cf}} \mathrm{z_f} \end{cases} \quad (4)$$

### 4.1 Mathematical demonstrating of the DBSCAN by PI controller

The whole topology in addition with complete mathematical modelling involved in the estimation of switching pulse generation is shown in the Fig. 3. The total strategy process is articulated below :

$$w_{pa}(n+1) = w_{pa}(n) + \mu_k e_k i_{La} u_{pa} - \sum_1^n w_{pa}(n)\xi_k \Big/ \sum_1^n w_{pa}(n) \quad (5)$$

$$w_{pb}(n+1) = w_{pb}(n) + \mu_k e_k i_{Lb} u_{pb} - \sum_1^n w_{pb}(n)\xi_k \Big/ \sum_1^n w_{pb}(n) \quad (6)$$

$$w_{pc}(n+1) = w_{pc}(n) + \mu_k e_k i_{Lc} u_{pc} - \sum_1^n w_{pc}(n)\xi_k \Big/ \sum_1^n w_{pc}(n) \quad (7)$$

$$w_{qa}(n+1) = w_{qa}(n) + \mu_k e_k i_{La} u_{qa} - \sum_1^n w_{qa}(n)\xi_k \Big/ \sum_1^n w_{qa}(n) \quad (8)$$

$$w_{qb}(n+1) = w_{qb}(n) + \mu_k e_k i_{Lb} u_{qb} - \sum_1^n w_{qb}(n)\xi_k \Big/ \sum_1^n w_{qb}(n) \quad (9)$$

$$w_{qc}(n+1) = w_{qc}(n) + \mu_k e_k i_{Lc} u_{qc} - \sum_1^n w_{qc}(n)\xi_k \Big/ \sum_1^n w_{qc}(n) \quad (10)$$

### 4.2 The mean of the weighting values for active and reactive components

The average quantity ($w_p$) of the active weighting measures of a, b and c-phase is computed as like below :

$$w_p = \frac{w_{pa} + w_{pb} + w_{pc}}{3} \quad (11)$$

The average quantity $(w_q)$ of the re-active weighting measures of a, b and c-phase is computed as like below :

$$w_q = \frac{w_{qa} + w_{qb} + w_{qc}}{3} \quad (12)$$

**4.3 Computation of in-phase and quadrature unit voltage template**

The in-phase unit voltage templates *( $u_{pa}, u_{pb}, u_{pc}$)* are the relation of phase voltages & amplitude of PCC voltage $(v_t)$ estimated as follows

$$u_{pa} = \frac{v_{sa}}{v_t}, u_{pb} = \frac{v_{sb}}{v_t}, u_{pc} = \frac{v_{sc}}{v_t} \quad (13)$$

Likewise, the quadrature unit potential patterns $(u_{qa}, u_{qb}, u_{qc})$ are the relations of phase potentials shown below :

$$\left.\begin{aligned} u_{qa} &= \frac{u_{pb} + u_{pc}}{\sqrt{3}} \\ u_{qb} &= \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}} \\ u_{qc} &= \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}} \end{aligned}\right\} \quad (14)$$

Where$v_t$ can be expressed as

$$v_t = \sqrt{\frac{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}{3}} \quad (15)$$

**4.4 Assessment of active module of reference supply currents**

The DC potential error can be attained by deducting sensed dc potential from reference dc potential and is written as

$$v_{de} = v_{dc\,(ref)} - v_{dc} \quad (16)$$

This difference is processed through the Proportional-Integral (PI) controller. The output of PI controller can be written as

$$w_{cp} = k_{pa} v_{de} + k_{ia} \int v_{de} dt \quad (17)$$

The total active modules of the reference supply current is found by totalling both output of PI controller and the mean magnitude of active module of output load current. It can be written as

$$w_{sp} = w_{ap} + w_{cp} \quad (18)$$

**4.5 Assessment of reactive module of reference supply currents**

The AC potential error can be attained by deducting sensed AC bus potential from reference AC potential and is written as

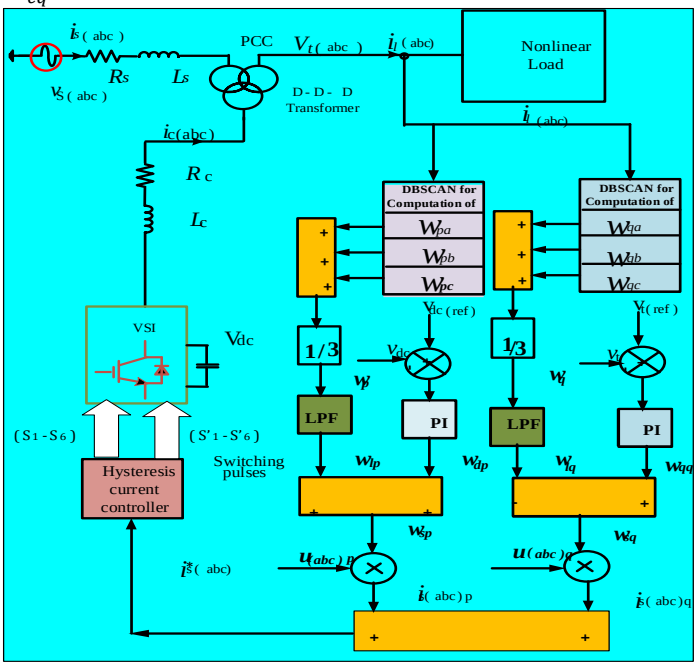
$$v_{te} = v_{t\,(ref)} - v_t \tag{19}$$

This difference is processed through the PI controller to maintain the constant ac bus voltage. The output of PI controller can be expressed as

$$w_{cq} = k_{pr} v_{te} + k_{ir} \int v_{te} dt \tag{20}$$

The total reactive modules of the reference supply current is found by deducting output of PI controller from the mean magnitude of active module of output load current. It can be written as

$$w_{sq} = w_{rq} - w_{cq} \tag{21}$$



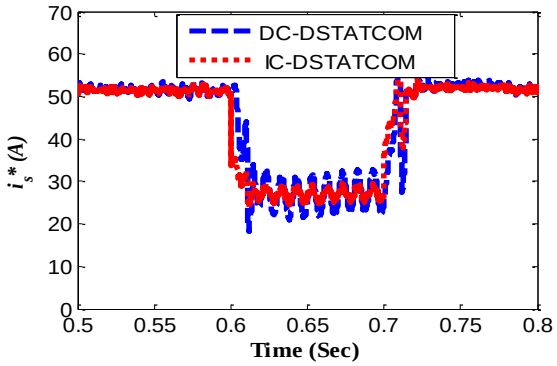




Fig.4 Switching signals generation using DBSCAN control algorithm for IC-DSTATCOMFig.5 Internal control signal of the control algorithm

### 4.6 Assessment of triggering arrangement

The instantaneous reference active module of each phase is estimated by multiplying in phase unit potential template with active current module. These are written as :

$$i_{aa} = w_{sp}u_{pa},\ i_{ab} = w_{sp}u_{pb},\ i_{ac} = w_{sp}u_{pc} \quad (22)$$

Likewise, the instantaneous reference reactive module of each phase is projected by multiplying in phase unit quadrature potential template with reactive current module. These are written as :

$$i_{ra} = w_{sq}u_{qa}, i_{rb} = w_{sq}u_{qb}, i_{rc} = w_{sq}u_{qc} \quad (23)$$

The summation of active and reactive components of current is called as reference source currents and these are obtained as

$$i^*_{sa} = i_{aa} + i_{ra}, i^*_{sb} = i_{ab} + i_{rb}, i^*_{sc} = i_{ac} + i_{rc} \quad (24)$$

The both actual source currents ($\boldsymbol{i_{sa}, i_{sb}, i_{sc}}$) and the reference source currents ($\boldsymbol{i^*_{sa}, i^*_{sb}, i^*_{sc}}$) of the respective phases arecompared then current error signals are fed to HCC. Their outputs are fed to $\mathbf{T_1}$ -$\mathbf{T_6}$insulated-gate bipolar transistors (IGBTs) used in the voltage source converter (VSC).

## 5. SIMULATION RESULTS & DISCUSSION:

The performance of EPDS with topologies are demonstrated using MATLAB/Simulink studies. Identical operating conditions and system parameters are considered to perform computer simulations. The suggested DBSCAN mechanism is implemented for reference current generation for appropriate switching pulses to the both varieties of topologies. The system parameters are listed in Table 1. Both the balanced and unbalanced performance of IC-DSTATCOM and DC-DSTATCOM based EPDS are analyzed here in the below sub-sections.

### 5.1 Simulation results of DC-DSTATCOM

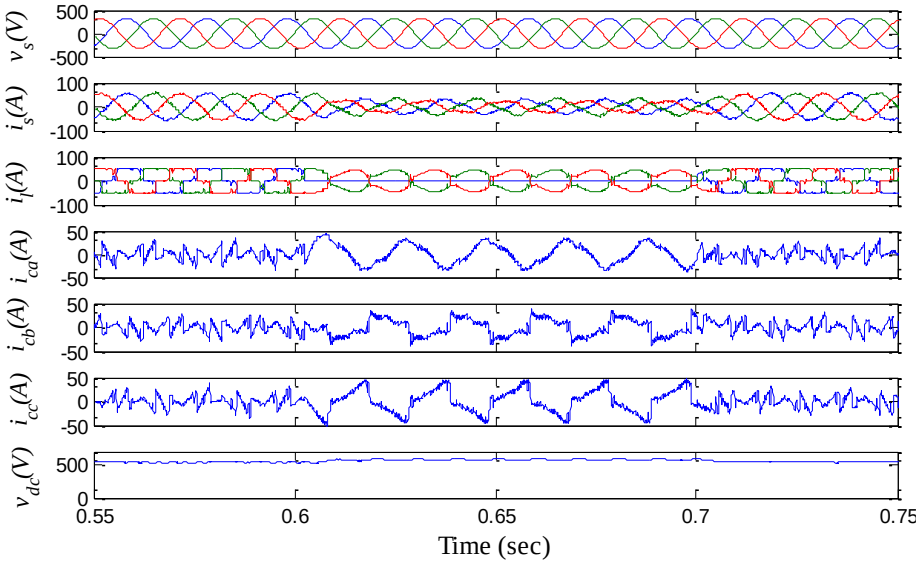



Fig. 6 a Simulation waveform of (top to bottom) three phase source voltage, source current, load current, compensating current and DC-link voltage with DC- DSTATCOM.

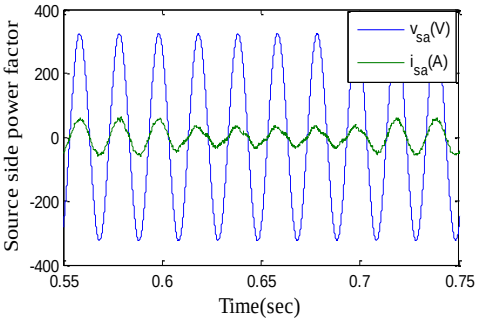



Fig.6 b Source side powerfactor with DC- DSTAT

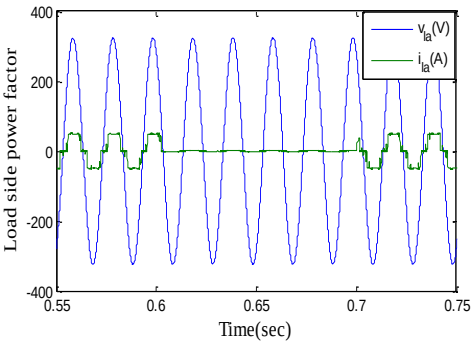



Fig. 6 c Load side powerfactor with DC- DSTATCOM

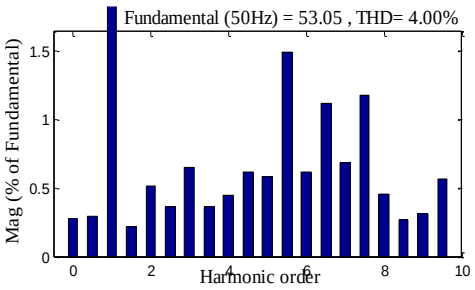



Fig.6 d Source current THD with DC- DSTATCOM

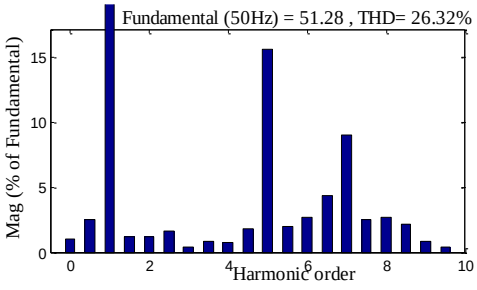



Fig. 6 e Load current THD with DC- DSTATCOM

To verify the power-quality performance during the un-balanced loading condition, DBSCAN based direct coupled DSTATCOM is considered. The simulation time in between 0.55S and 0.75S for this Power Distribution system (PDS) is choosen. Here, the single-phase load is switched off in a-phase by disconnecting the circuit breaker (CB) at 0.6 and switched on at 0.7 Sec.as depicted in fig 6 a. For this particular event, time in varying load is maintained all over the mentioned simulation time, as depicted in fig. 6 a. Several sub figuresare arranged on the common plot to show the behaviour of supply voltage ($v_s$), load current ($i_l$), source current ($i_s$), compensator current ($i_{ca,}\, i_{cb,}\, i_{cc}$) and respective DC link voltage ($v_{dc}$) respectively.By considering a-phase supply voltage and corresponding current, the power factor of the supply side is observed and shown in Fig.6. b. From this figure, the source side power factor is maintained to improve and maintained at p.f 0.97. The harmonics mitigation performance of the source and load current are shown in the fig.6 d. and fig.6 e. respectively.In fig.6 e. the THD of the load current is greatly distorted and whose THD is 26.32.%, whereas source current is significantly improved with reduced THD value (THD 4%) The voltage THD value is maintained with a smaller value than the requirement of the IEEE-519-2017 and IEC-61000-3-2 standard (i.e., THD < 5%). In addition, this control scheme maintains load balancing and voltage regulation as shown in Fig.6 a. Therefore, it can be said that the proposed control scheme is suitable for the improvement of the PQ in the PDS.

### 5.2 Simulation results of IC- DSTATCOM

To verify the power-quality performance during the unbalanced loading condition, DBSCAN based inductively coupled DSTATCOM is considered. The simulation time in between 0.55S and 0.75S for this Power Distribution system (PDS) is chosen. Here, the single-phase load is switched off in a-phase by disconnecting the circuit breaker (CB) at 0.6 and switched on at 0.7 Sec.as depicted in fig 7 a. For this particular event, time varying load

is maintained all over the mentioned simulation time, as depicted in fig.7 a. Several sub figures are arranged onthe common plot to show the behaviour of supply voltage ($vs$), load current ($\boldsymbol{i_l}$), source current ($is$), compensator current ($ica$, $icb$, $icc$) and respective DC link voltage ($v_{dc}$) respectively. By considering a-phase supply voltage and corresponding current, the power factor of the supply side is observed and shown in Fig. 7 c from this figure, the source side power factor is maintained to improve and maintained at p.f 0.99. The harmonics mitigation performance of the source and load current are shown in the fig.7 d and fig.7 e respectively. In fig.7 e the THD of the load current is greatly distorted and whose THD is 26.69%, whereas source current is significantly improved with reduced THD value (THD 2.94%) The voltage THD value is maintained with a smaller value than the requirement of the IEEE-519-2017 and IEC-61000-3-2 standard (i.e., THD < 5%). In addition, this control scheme maintains load balancing and voltage regulation as shown in Fig.7. a. Therefore, it can be said that the proposed control scheme is suitable for the improvement of the PQ in the PDS. Because of the 535V desired and consistent DC link voltage, the voltage regulation is maintained. Finally, 320V is maintained at PCC to meet the voltage balancing requirements.

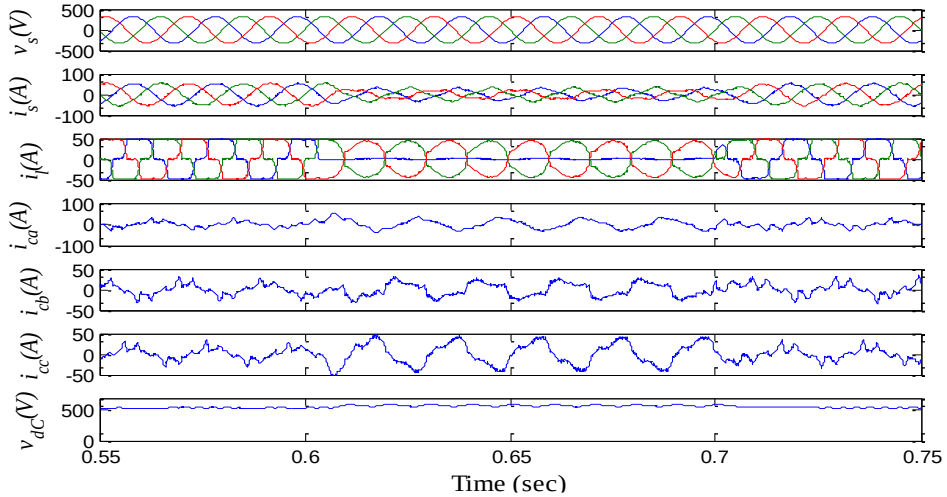



Fig. 7 a Simulated (top to bottom) three phase supplypotential, supply current, output load current, compensated current,DC-link potential with IC-DSTATCOM

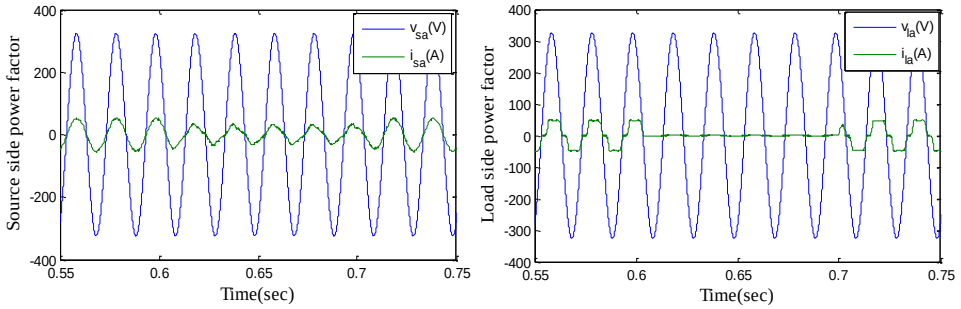



Fig. 7 b Source side powerfactor with IC-DSTATCOMFig. Fig 7 c Load side powerfactor with IC-DSTATCOM

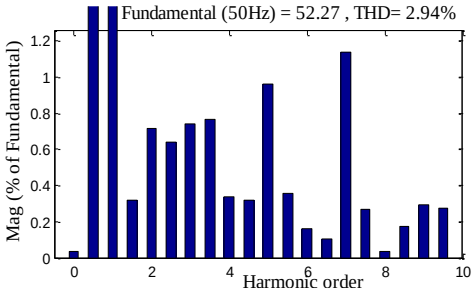



Fig. 7 d Source current THD with IC-DSTATCOMFig.

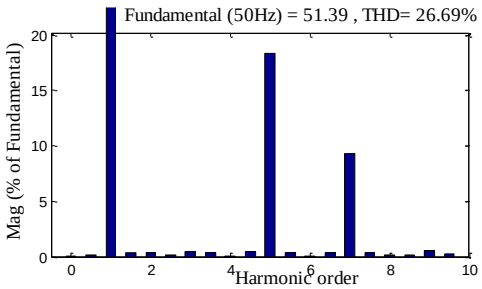



Fig 7 e Load current THD with IC-DSTATCOM

Table.1 Simulation formation parameters

| Symbol | Definition | Value |
|---|---|---|
| $v_s$ | 3- phase supply potential | 230V/phase |
| $f_s$ | Frequency | 50Hz |
| $R_s$ | Input resistance | 0.5Ω |
| $L_s$ | Input inductance | 2mH |
| $K_{pr}$ | AC Proportional controller | 0.2 |
| $K_{ir}$ | AC 'I' controller | 1.1 |
| $v_{dc}$ | DC link potential | 600V |
| $C_{dc}$ | Capaciter | 2000μF |
| $K_{pa}$ | DC 'P' controller | 0.01 |
| $K_{ia}$ | DC Integral controller | 0.05 |
| $R_c$ | VSC resistance | 0.25Ω |
| $L_c$ | VSC inductance | 1.5mH |

Table.2 Basic rating parameters of the IFCT

| | Grid side | Load side | Filtering side |
|---|---|---|---|
| **Wiring scheme** | **Wye** | **Wye** | **Wye** |
| **Nominal power and f** | **10kV, 50 Hz** | **10kV, 50 Hz** | **10kV, 50 Hz** |
| **Voltage (ph-ph), R, and L** | **230V, 0.002 (pu), 0.08 (pu)** | **230V, 0.002 (pu), 0.08 (pu)** | **230V, 0.002 (pu), 0.08 (pu)** |
| **Magnetic resistance** | **500Ω** | **500 Ω** | **500 Ω** |
| **Magnetic inductance** | **500 Ω** | **500 Ω** | **500 Ω** |

Table.3 Measured active and reactive power of IFCT

| | | |
|---|---|---|
| **Grid side** | **Active power**<br>**reactive power** | **26 kW**<br>**1.388 kVAR** |
| **Load side** | **Active power**<br>**reactive power** | **15 kW**<br>**1.388 kVAR** |
| **Filtering side** | **Active power**<br>**reactive power** | **24 kW**<br>**570 VAR** |

The performance analysis of the both DC-DSTATCOM and IC-DSTATCOM are indicated in Table-4. The proposed IC-DSTATCOM deducted a highly contaminated supply current harmonics from the EPDS as compared to other.

Table.4 Performance parameter of DC-DSTATCOM and IC-DSTATCOM

| **Performance parameter** | **DSTATCOM at PCC** | |
|---|---|---|
| | **CDC-DSTATCOM** | **CIC-DSTATCOM** |
| **$i_s$(A), %THD** | 53.05, 4.00 | 52.27, 2.94 |
| **$v_s$ (V), %THD** | 321.4, 2.23 | 321, 1.42 |
| **$i_l$ (A), %THD** | 51.28, 26.32 | 51.39, 26.69 |
| **Power Factor** | 0.94 | 0.99 |

### 5.3 Analysis and calculation of kVA rating, DF, HCR, DIN, FF, RF, HF and C-Message weights

#### 5.3.1 Analysis of kVA rating

The Volt ampere (kVA) rating can be obtained as VA rating=$\sqrt{3} * \frac{v_{dc}}{\sqrt{2}} * \frac{I_f}{\sqrt{2}}$

Where $v_{dc}$ is the DC link voltage of DSI and $I_f$ is the inverter current

kVA rating of DC-DSTATCOM = $\sqrt{3} * \frac{541}{\sqrt{2}} * \frac{12.5}{\sqrt{2}} = 5.856\ kVA$

kVA rating of IC-DSTATCOM = $\sqrt{3} * \frac{541}{\sqrt{2}} * \frac{10.5}{\sqrt{2}} = 4.919$kVA

#### 5.3.2 Calculation of Derating Factor (DF)

DF= 1-efficiency  Efficiency = $\frac{\text{output power}}{\text{input power}} * 100$

The power efficiency of DC-DSTATCOM can be calculated by the following

kVA rating of CDC-DSTATCOM = 5.85 kVA, power factor cosϕ = 0.97

kW output of the CDC-DSTATCOM = kVA* cosϕ  5.85*0.97 = 5.67 kW

Power losses of CDC-DSTATCOM = $3I_f^2 * R_c$

$I_f$ is the inverter current= 12.5 A, $R_c$= 0.25 Ω

$3I_f^2 * R_c$ = 3*$12.5^2 * 0.25$ = 117.18 W

Power input = output power + losses

= 5670+117.18 = 5787.18 W = 5.787 kW

Efficiency of DC-DSTATCOM = $\frac{5.67}{5.787} * 100$ = 97.97%

DF of DC-DSTATCOM = 1- efficiency = 1- 0.97 = 0.03

The power efficiency of IC-DSTATCOM can be calculated by the following

kVA rating of IC-DSTATCOM = 4.919 kVA, power factor cosϕ = 0.99

kW output of the IC-DSTATCOM = kVA* cosϕ

4.919*0.99 = 4.869 kW

$I_f$ is the inverter current= 10.5 A, $R_c$= 0.25 Ω

$3I_f^2 * R_c$ = 3*$10.5^2 * 0.25$ = 82.68 W

Power input = output power + losses

= 4869 + 82.68 = 4951.68 W = 4.95 kW

Efficiency of IC-DSTATCOM = $\frac{4.86}{4.95} * 100$ = 98.18%

DF of IC-DSTATCOM = 1- efficiency = 1- 0.981 = 0.019

### 5.3.3 Harmonic compensation ratio (HCR)

The HCR of DC-DSTATCOM is calculated as follows

HCR= $\frac{\text{THD\% after compensation}}{\text{THD\% before compensation}} = \frac{4.00}{26.32} = 0.151$

Similarly, the HCR of IC-DSTATCOM is given as

HCR= $\frac{THD\% after compensation}{\text{THD\% before compensation}} = \frac{2.94}{26.69} = 0.1101$

### 5.3.4 Distortion index (DIN)

Taylor series expansion for small ranks of harmonics is below

DIN = THD (1- $\frac{1}{2}$ (THD))

DIN for DC-DSTATCOM = 4.00(1- $\frac{1}{2}$ 4.00) = -4

DIN for IC-DSTATCOM = 2.94 (1- $\frac{1}{2}$ 2.94) = -1.38

### 5.3.5 Form factor (FF)

The form factor is defined as FF = $\frac{I_{rms}}{I_{avg}}$

FF for DC-DSTATCOM =

$I_{rms}$= 39.14 A $I_{rms} = \frac{\pi}{2\sqrt{2}} I_{avg}$

$I_{avg}$=35.23A FF= $\frac{39.14}{35.23}$= 1.11

FF for IC-DSTATCOM =

$I_{rms}$= 37.65 A $I_{avg}$=33.89A

FF= $\frac{37.65}{33.89}$= 1.11

### 5.3.6 Ripple factor (RF)

RF is measure of the ripple content of the waveform RF= $\frac{I_{AC}}{I_{DC}}$

RF= $\frac{\sqrt{(I_{rms})^2 - (I_{DC})^2}}{I_{DC}} = \sqrt{(FF^2) - 1}$

RF for DC-DSTATCOM = $\sqrt{(FF^2)-1}$= $\sqrt{(1.11^2)-1}$ = 0.48

RF for IC-DSTATCOM = $\sqrt{(FF^2)-1}$= $\sqrt{(1.11^2)-1}$ = 0.48

### 5.3.7 Harmonic factor (HF)

The HF of the $h_{th}$ harmonic, $HF_h = \frac{I_{rms}^{(h)}}{I_{rms}^{(1)}}$

HF for DC-DSTATCOM = $\frac{39.14}{53.05} = 0.737$

HF for IC-DSTATCOM=$\frac{37.65}{52.27}$ = 0.72

### 5.3.8 C-Message weights

The C-Message weighted index is very similar to the TIF except that the weights $c_i$ are used in place of $w_i$

C= $\frac{\sqrt{\sum_{i=1}^{\infty}(C_i I^{(i)})^2}}{\sqrt{\sum_{i=1}^{\infty}(I^{(i)})^2}}$ C= $\frac{\sqrt{\sum_{i=1}^{\infty}(C_i I^{(i)})^2}}{I_{rms}}$

C-Message weights for DC-DSTATCOM = $\frac{39.14^2}{53.05^2}$ = 0.54

C-Message weights for IC-DSTATCOM = $\frac{37.65^2}{52.27^2}$ = 0.51

Table.5 Comparative study on kVA rating, DF, HCR, DIN, FF, RF, HF and C-Message weight of DC-DSTATCOM and IC-DSTATCOM

| Sl. No. | Types of configurations | Analysis of KVA rating | DF | HCR | DIN | FF | RF | HF | C-message weight |
|---|---|---|---|---|---|---|---|---|---|
| 1 | DC-DSTATCOM | 5.856 | 0.03 | 0.151 | -4 | 1.11 | 0.48 | 0.737 | 0.54 |
| 2 | IC-DSTATCOM | 4.919 | 0.019 | 0.1101 | -1.38 | 1.11 | 0.48 | 0.72 | 0.51 |

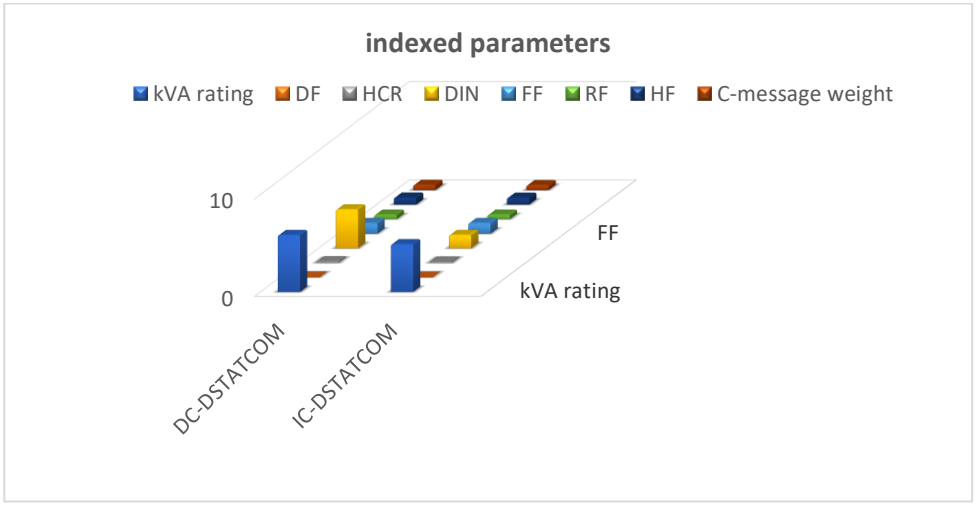



Fig. 8 Bar chart for the indexed parameters

It is observed that the proposed study reveals the applicability and suitability for the PQ improvement. Finally, the bar chart for the indexed parametersis presented in the Fig.8

## 6. Conclusion

This research work focuses on the analysis of two different types of IC-DSTATCOM and DC-DSTATCOM topologies. Firstly, this paper analysed the motivation of DSTATCOM with direct coupling, secondly, analysed the efficiency of inductively coupled DSTATCOM. Finally, the proposed DBSCAN topology could realize more effective usage in terms of power quality. The key features of the proposed topology is highlighted as follows:

- Inclusion of IFCT caused to improve the output AC voltage at inverter side as compared to other case studies.
- The advantages like low voltage stress, less switching loss and higher efficiency are observed.
- Apart from these above mentioned merits, load balancing, source current harmonics elimination, voltage regulation, pf improvement are obtained as per target value of IEEE and IEC grid code.

The simulation analysis is carried out for the selection of topology among two approaches under unavoidable circumstances of loading. With these benefits, a thorough real time analysis will be the key features for the future work.

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