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Impedance Control in HDI and Substrate-Like PCBs for AI Hardware Applications

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Abstract: As artificial intelligence (AI) is becoming increasingly embedded in mission-critical systems across medical, defense, and aerospace sectors, the reliability and performance of hardware interconnects have become paramount. These applications demand compact, high-density circuit boards capable of supporting high-speed data transfer with exceptional signal integrity and minimal electromagnetic interference. Impedance control in high-density interconnect and substrate-like printed circuit boards (PCBs) plays a critical role in ensuring the functional integrity of AI systems used in surgical robotics, battlefield edge computing, avionics, and autonomous systems. This paper explores the principles and implementation of impedance control in advanced PCB structures, focusing on material selection, trace design, stack-up engineering, and simulation strategies tailored for harsh and regulated environments. Key challenges such as dielectric stability under extreme temperatures, signal degradation over long routing paths, and compliance with aerospace and medical electromagnetic compatibility standards are addressed. Real-world case studies illustrate how precise impedance management facilitates low-latency processing, secure communication, and fault-tolerant design in compact, ruggedized systems. The paper concludes by identifying the future directions in substrate design and advanced packaging needed to meet the stringent demands of AI-driven applications in these high-reliability domains.

1. Introduction

The integration of artificial intelligence (AI) into mission-critical systems has accelerated the demand for high-performance, ultrareliable electronic infrastructure across sectors such as medical diagnostics, defense electronics, and aerospace navigation. In these applications, the margin for error is exceptionally narrow. Whether managing real-time imaging in surgical robotics, securing battlefield communication, or autonomous flight control in next-generation aircraft, the underlying hardware must offer consistent signal integrity, power efficiency, and environmental robustness.

In the United States, this need is amplified by the strategic focus on domestic semiconductor innovation and defense modernization initiatives under programs like the CHIPS and Science Act, DARPA Microsystems Technology Office, and U.S. Department of Defense Trusted Foundry program. These initiatives underscore the importance of resilient, high-speed interconnect technologies—including high-density interconnect (HDI) and substrate-like printed circuit board (PCB) (SLP) architectures—as critical enablers for AI acceleration hardware and edge-computing platforms used in secure and safety-critical domains.

Globally, advanced AI-driven systems are expanding rapidly in both commercial and sovereign defense programs. Countries in Europe, East Asia, and the Middle East are investing heavily in AI-enabled aerospace systems, smart military platforms, and autonomous medical devices. Across these applications, impedance control in high-density PCBs has emerged as a fundamental design requirement—not just for performance, but for global regulatory compliance (e.g., IEC 60601, EN 50155, MIL-STD-461, RTCA DO-160) and interoperability in multinational missions or collaborative research environments.

As frequencies scale beyond 25–56 Gbps and system complexity increases with the incorporation of chiplet architectures, high-bandwidth/low-power-double-data-rate memories, and high-speed input/output (I/O) (e.g., PCIe Gen5/Gen6, SerDes), impedance mismatches have significant risks. Poor control of characteristic

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impedance results in increased signal reflection, electromagnetic interference, jitter, and power inefficiency—issues that can compromise patient safety, weapon-system reliability, and satellite mission stability.

This paper focuses on the methods, challenges, and evolving best practices for impedance control in HDI and SLP technologies—highlighting their role in enabling reliable, compact, and high-frequency interconnects for AI-driven systems in medical, defense, and aerospace applications. It aims to provide engineers, designers, and system integrators with actionable insights into designing future-proof hardware that meets the rigorous performance and compliance standards required across the U.S. and the world.

2. Importance of Controlled Impedance in AI Hardware

With the scaling of AI hardware, in terms of speed and complexity, signal integrity has become a critical limiting factor that affects the system performance and reliability. Impedance control—maintaining a constant characteristic impedance along signal traces—is essential to ensure data integrity across high-speed interconnects. In AI systems, particularly those deployed in medical, defense, and aerospace environments, the consequences of signal degradation due to impedance mismatches can lead to system failure, security vulnerabilities, or even life-threatening scenarios.

2.1 Signal Integrity at High Frequencies

AI processors and accelerators frequently operate at data rates exceeding 25 Gbps per lane, with interfaces like PCIe Gen5/6, SerDes, and HBM3 pushing performance toward multi Tbps bandwidths. These high-speed signals act as transmission lines, where any deviation in the trace impedance causes signal reflections, insertion loss, and timing skew. Differential pairs used in high-speed I/O are especially sensitive to impedance mismatches, which can degrade eye diagrams and increase bit error rates, compromising machine-learning inference accuracy and real-time response in critical systems.

2.2 Relevance in Medical Devices

In the medical sector, AI hardware is embedded in diagnostic imaging systems (e.g., MRI, CT, and ultrasound), surgical robots, and wearable patient monitors. These devices require high-speed data acquisition and low-latency processing for real-time visualization and analytics. Impedance control ensures accurate signal transmission with compact form factors while meeting electromagnetic compatibility (EMC) standards such as IEC 60601. Any reflection or loss in the signal integrity can impact the diagnostic resolution or interfere with sensitive analog front ends.

2.3 Strategic Implications in Defense Systems

In defense electronics, AI is used in autonomous platforms, sensor fusion, electronic warfare, and secure communications. Systems must operate reliably in hostile and noisy electromagnetic environments. Impedance mismatches can result in electromagnetic interference (EMI) leakage, system instability, or susceptibility to adversarial signal injection. Impedance control is essential for maintaining not only data integrity but also low observable signatures and compliance with MIL-STD-461 and MIL-PRF-31032 in mission-critical electronics.

2.4 Demands in Aerospace and Avionics

In aerospace applications, AI facilitates predictive maintenance, flight autonomy, and real-time navigation. These systems demand lightweight, high-density electronics capable of withstanding extreme temperatures, radiation, and vibration. Impedance control in HDI and substrate-like PCBs allows designers to route high-speed signals within constrained footprints while adhering to DO-160 EMC and signal-integrity guidelines. In satellite payloads and edge AI avionics, stable impedance is essential for sustaining link reliability and power efficiency over long transmission paths.

2.5 Enabling Future-Proof AI Architectures

Emerging AI architectures increasingly rely on chiplet integration, 2.5D/3D packaging, and stacked memories—all of which increase the routing complexity and demand tighter impedance tolerances. As the interconnect density increases, the margin for manufacturing variations decreases. Impedance control via accurate simulation, stackup optimization, and advanced PCB processes, becomes a cornerstone for scaling AI hardware without compromising reliability or compliance.

3. HDI and SLP Technologies

HDI and SLP technologies represent the cutting edge of electronic packaging and interconnect design, playing a crucial role in achieving the dense, high-speed performance required by modern AI hardware. These technologies are particularly significant in mission-critical environments such as medical systems, aerospace avionics, and defense electronics, where reliability, compactness, and electrical performance are paramount.

HDI PCBs are distinguished by their use of microvias—often with diameters of 150 μm or smaller—along with fine-line routing capabilities, high layer counts, and precise via structures. Components such as stacked and staggered vias, laser-drilled interconnects, and build-up layer configurations like 1+N+1 or 2+N+2 facilitate dense component placement and efficient signal routing. These features make HDI ideal for compact electronic assemblies where the signal path length and interconnect parasitics must be minimized. In medical technology, HDI is commonly used in miniaturized diagnostic modules and wearable AI health monitors. In defense applications, it supports rugged AI-enabled battlefield devices and radar processing units. Aerospace systems rely on HDI for compact, lightweight avionics and on-board computing modules with real-time processing capabilities.

SLP technology takes miniaturization and performance a step further by adopting design rules more closely aligned with that of semiconductor substrates. SLPs feature ultrafine line and space widths, often down to 10 to 20 μm, as well as low-profile copper foils and high-Tg, low-loss dielectric materials. These properties allow extremely dense interconnects with improved signal fidelity at high frequencies. SLPs are becoming increasingly important in AI hardware architectures based on chiplet integration, system-in-package designs, and 2.5D/3D heterogeneous packaging. In medical devices, SLPs are used in embedded AI imaging systems and compact handheld diagnostic tools. Defense systems benefit from SLPs by enabling compact integration of high-performance AI system-on-chip designs and secure communication processors. Aerospace platforms apply SLPs in drones, satellites, and advanced flight computers that require lightweight, high-speed, and thermally robust circuit platforms.

Both HDI and SLP technologies offer significant benefits for impedance control. Their precise trace geometry, smooth copper-surface quality, and stable dielectric characteristics enable designers to maintain consistent impedance across complex signal paths. These technologies also support advanced design features such as via-in-pad, back-drilling, and buried vias, which help reduce impedance discontinuities and via stubs that can otherwise cause reflections and signal degradation.

However, implementing HDI and SLP designs introduces notable manufacturing challenges. Fine-line traces and microvias are more susceptible to etch variations, which can impact impedance accuracy. Material selection becomes more complex as designers must balance low dielectric loss with thermal stability and compliance with stringent standards such as UL 94V-0 and RoHS. The complexity of manufacturing such boards can also affect the yield and production cost, making early collaboration between designers, PCB fabricators, and material suppliers essential. To manage these risks, advanced quality-assurance methods—such as automated optical inspection, X-ray computed tomography, and time-domain reflectometry (TDR)—are being increasingly employed to ensure process control and validate impedance performance.

4. Impedance Design and Simulation Techniques

Impedance control begins with deliberate and precise interconnect design. As the signal frequencies in AI hardware increase, the importance of detailed electromagnetic modeling, prelayout simulation, and rigorous

signal-integrity validation grows substantially. In the context of HDI and SLPs, where geometries are more compact and signal paths more complex, impedance design must be treated as a system-level engineering discipline, not a layout afterthought.

Impedance is primarily governed by the geometry of the conductor—specifically the trace width, thickness, and spacing—as well as the properties of the dielectric material, such as the dielectric constant (Dk) and dissipation factor (Df), and the proximity to the reference planes. In high-speed AI systems, these variables must be tightly controlled to maintain consistent characteristic impedance—typically 50 Ω for single-ended traces and 100 Ω for differential pairs. Even a 10% deviation can cause reflections, degraded eye patterns, or inter-symbol interference, ultimately affecting performance in real-time inference or signal-processing systems.

A crucial starting point in impedance control is material selection. Low-loss, high-Tg dielectric materials, such as modified polyimides or hydrocarbon-based resin systems, are favored for their stability under thermal stress and high-frequency conditions. This is particularly important in aerospace applications, where rapid thermal cycling and altitude-related environmental changes can affect signal fidelity. The dielectric properties must remain consistent to avoid impedance drift, which can lead to signal distortion or EMI compliance failure.

The stack-up configuration plays an equally important role. In an eight-layer HDI board used for a spaceborne AI navigation module, for example, a 2+4+2 structure was employed with 50 Ω impedance-controlled single-ended traces routed on layers 2 and 7, referenced to internal ground planes on layers 3 and 6. The use of ultrathin dielectric layers (50–75 μm) between signal and reference planes helped ensure tight impedance tolerance across extreme temperatures. The routing of differential pairs for high-speed sensor fusion data was carefully symmetrized to maintain 100 Ω differential impedance with <5% variation, verified through both simulations and TDR testing.

Simulation tools such as Ansys HFSS and Keysight ADS were used in this example to perform full-wave modeling of the interconnects, including via transitions, connector pads, and return paths. Signal reflections from via stubs were eliminated using back-drilling, and via impedance was tuned using annular ring size and pad stack adjustments. Post-layout extraction was performed to validate routing constraints and ensure impedance compliance across the entire design.

Advanced modeling was followed by real-world validation using TDR. The AI module's differential impedance measured across various signal paths showed <3 Ω of deviation, confirming that the simulated results accurately reflected the fabricated performance. This level of precision was required to meet both RTCA DO-160 standards for EMI and NASA workmanship guidelines for flight hardware reliability.

This case highlights how a simulation-driven, material-conscious, and stack-up–optimized approach to impedance control is critical for ensuring performance in harsh environments. The same principles are equally applicable to medical devices requiring compliance with IEC 60601, or defense systems bound by MIL-STD-461 and MIL-PRF-31032.

By integrating impedance design early into the development cycle and verifying through both simulations and measurement, AI hardware engineers can prevent downstream signal-integrity issues and ensure consistent and reliable performance across applications and industries.

5. Manufacturing Challenges and Process Control

Once impedance-controlled designs are finalized and validated through simulations, ensuring they are accurately reproduced during PCB fabrication becomes the next critical challenge—particularly in medical, defense, and aerospace applications, where the cost of signal degradation can be catastrophic. Controlled impedance manufacturing is a high-precision process that requires tight coordination between the design intent, material selection, stack-up verification, and fabrication process capabilities.

The foundation of impedance accuracy in manufacturing begins with precise control of the trace geometry and dielectric thickness. Even small deviations—in the order of a few micrometers in the trace width or dielectric

height—can shift the impedance outside the specified tolerance window. In AI-enabled medical devices such as high-resolution portable ultrasound systems, where Gb-level data are transmitted between sensors and onboard AI processors, maintaining 100-Ω differential impedance is essential for avoiding latency or frame loss. In one such example, a 10-layer SLP-based board was used, with differential LVDS and USB 3.1 data channels routed in the inner signal layers. The manufacturer utilized low-profile reverse-treated copper and built-in optical metrology systems to ensure trace uniformity within ±3 μm, achieving higher than ±5% impedance consistency across the panel.

Manufacturers must also validate copper thickness, particularly for outer and inner layers where plating and etching processes vary. Advanced impedance-controlled builds often rely on reverse-treated or rolled annealed copper foils, which offer superior etch uniformity and smoother surfaces for high-frequency transmission. The copper roughness has a measurable effect on signal attenuation at frequencies above 5 GHz, commonly encountered in AI data buses and sensor links.

To maintain stack-up integrity, lamination processes must be tightly controlled. In HDI and SLP builds, multiple lamination cycles and ultra-thin prepregs (as thin as 25–50 μm) are common. Press cycle pressure, temperature ramp profiles, and resin flow control are key to minimizing variation in dielectric spacing, which directly affects the impedance. In aerospace applications where outgassing and moisture absorption are concerns, prepregs with tightly specified glass transition temperatures (Tg) and moisture diffusion characteristics are often required, adding another layer of complexity.

Via structures are another critical manufacturing factor. Stacked microvias, via-in-pad designs, and blind/buried vias must be carefully designed and fabricated to minimize impedance discontinuities. Techniques such as resin filling, copper plating, and back-drilling are used to eliminate stubs and ensure smooth impedance profiles across interconnect transitions. In high-speed AI radar systems for defense applications, back-drilling of through-hole vias is a standard process to eliminate parasitic capacitance that could otherwise corrupt high-speed ADC data transmission.

After fabrication, impedance verification is typically carried out using TDR. Controlled impedance test coupons—small sections of boards fabricated with identical stack-up and trace geometries—are placed on the panel edge and measured to confirm the performance. In high-reliability builds, 100% coupon testing is mandated, and in some cases, inline real-time impedance scanning is used for continuous process monitoring.

Furthermore, compliance with international manufacturing standards is essential. For medical devices, compliance with ISO 13485 and traceability requirements often necessitate detailed documentation of impedance-measurement results, fabrication parameters, and supplier certifications. In the defense sector, IPC-6012DS and MIL-PRF-31032 requirements may impose limits on the impedance tolerance, test frequency, and board-level inspection methods. Aerospace applications often require compliance with AS9100 and NASA-STD-8739, including outgassing limits and thermal cycling stress tests.

Ultimately, achieving high-fidelity impedance in production is not merely about fabricating what was designed; it is about building what was validated in simulation and ensuring it performs reliably over the product's life cycle, across mission profiles. This is only possible through deep collaboration between design engineers, fabrication partners, and quality-assurance teams—especially in safety and mission-critical applications that depend on AI-powered hardware.

6. Case Applications in AI Hardware

As AI hardware moves into high-reliability domains such as medical diagnostics, defense electronics, and aerospace systems, the need for tightly controlled impedance becomes a prerequisite for signal integrity, data accuracy, and system safety. Below are three validated case studies that illustrate how impedance control is engineered and validated in these mission-critical environments.

Medical Example: AI-Enabled Portable Ultrasound Device

- **Application**: Real-time imaging and diagnostics.
- **Technology Used**: 10-layer SLP with USB 3.1 and LVDS high-speed channels.
- **Impedance Control**: Differential impedance of 100 Ω ±5% on inner layers for data transfer from the probe to AI processor.
- **Techniques**: Ultrafine line width (35 μm), low-loss dielectric (Dk 3.2), and reverse-treated copper for reduced signal loss.
- **Result**: Achieves reliable imaging with < 1 ms lag, meeting IEC 60601 EMI and safety standards.

Defense Example: AI-Based Radar Signal Processor

- **Application**: Target tracking and pattern recognition in tactical environments.
- **Technology Used**: 12-layer HDI PCB with stacked microvias and high-speed DDR4 + SerDes interconnects.
- **Impedance Control**: 50 Ω single-ended and 100 Ω differential impedance for radar-to-AI DSP links.
- **Techniques**: Via-in-pad design with copper filling and back-drilling, MIL-PRF-31032-qualified materials.
- **Result**: Maintains signal integrity at 6.4 Gbps per lane under MIL-STD-461 EMI compliance, deployed in airborne ISR systems.

Aerospace Example: AI Navigation Unit for Satellites

- **Application**: Autonomous AI navigation and telemetry in low Earth orbit (LEO).
- **Technology Used**: 8-layer HDI–SLP hybrid with embedded capacitors and low-profile copper.
- **Impedance Control**: 100 Ω differential routing with ±10% margin across –40 to +125 °C.
- **Techniques**: 2+4+2 build-up structure, thermally stable polyimide dielectric, and full TDR test on each panel.
- **Result**: Radiation-hardened AI board with validated impedance stability through RTCA DO-254 and NASA outgassing standards.

7. Conclusion

As AI hardware continues to penetrate mission-critical sectors—ranging from autonomous aerospace navigation to AI-assisted surgical imaging—the need for precision-engineered interconnects becomes more than a design preference; it becomes a reliability imperative. Controlled impedance, when executed correctly, ensures that high-speed signals travel across PCBs without distortion, delay, or degradation, allowing machine-learning models and inference engines to operate with deterministic timing and signal integrity.

HDIs and SLPs have emerged as the foundational platforms enabling this level of performance. Their capacity to support fine-line routing, ultrathin dielectrics, stacked vias, and embedded passives makes them ideal for the complex impedance environments of AI processors, memory interfaces, and high-speed I/O.

In this paper, we explored:

- The physical and electrical principles behind impedance control.
- The critical role of simulation, modeling, and stack-up optimization.

- Practical manufacturing techniques such as back-drilling, via filling, and tight trace tolerances.
- Real-world case studies from medical, defense, and aerospace domains.

The key takeaway was that **impedance control is not a one-time engineering step—it is a lifecycle commitment**, beginning in early design, continuing through fabrication, and extending into validation and in-field performance monitoring. It requires tight integration between electrical engineers, PCB fabricators, quality-assurance teams, and end-application specialists.

As AI hardware advances toward faster data rates, smaller footprints, and harsher operating environments, the demand for robust, reproducible impedance control will only intensify. Organizations that embed impedance-aware design practices into their product development workflows will not only achieve superior signal integrity, but also accelerate compliance, reduce field failures, and deliver higher performance AI systems.