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Enhancing Five-level Resonant Boost Converter for High Voltage Applications

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Abstract: - This work proposes a five-level LLC boost DC-DC resonant converter with a reduced switch count, designed to achieve wide input voltage ranges, high efficiency, and constant output voltage across various input and load conditions. The converter utilizes two diode-bypassed inverter topologies, reducing the switch count, size, and cost of the multilevel inverter while maintaining performance. The voltage gain is selected to provide an output of 1000V from an input range of 200V to 300V, with a switching frequency range of 57.10kHz to 158.64kHz. Simulations in MATLAB/Simulink confirm that the converter operates with a switching frequency consistently below the resonance frequency under all conditions, similar to five-level cascaded H-bridge inverters. The frequency controller ensures a stable 1000V output, achieving a full load efficiency of 93.66%. The diode-bypassed DC-link inverter is preferred over the diode-bypassed neutral-point inverter due to its higher efficiency at load currents below 3A, and comparable efficiency above 3A, all with a reduced switch count of five. The results show a 37.5% reduction in switch count, a 45% decrease in power loss, and a 5% improvement in efficiency with the diode-bypassed DC-link inverter.

Keywords: DC-DC Resonant Converter, Multilevel Inverter, Diode-bypassed Inverter.

I. INTRODUCTION

The demand for DC-DC resonant converters (RC) has increased in most medium and high-voltage applications, especially in sectors such as renewable energy, electric vehicles, and power distribution systems [1-2]. This is because of their benefits and proven performance compared to conventional DC-DC converters, which encounter significant challenges such as increased switching losses, higher voltage stresses for switches, and reduced efficiency when applied to high-voltage applications. These problems can be mitigated by applying the LLC resonant boost converter (RC) using a multi-level inverter (MLI) which ensures soft switching, lower switch stress, low EMI emission, high efficiency, etc. [3]. Although MLIs offer advantages in topology and control schemes, they have the undeniable limitation of requiring a relatively higher number of power switches as the output voltage level increases. This, in turn, increases the cost, size, and control complexity [4]. Therefore, applying reduced-switch MLIs to RC is required for benefits: less component count, less space consumption and cost-effectiveness [5]. By comparing with other MLI topologies, the cascaded H-bridge MLI (CHBMLI) is studied [6-7] due to its lower component count. Hence, a RC using a CHBMLI is used for comparison to the proposed reduced-switch multilevel RC. A five-level inverter is selected for this project rather than other voltage level, because of its lesser circuit complexity and almost equal THD level compared to a seven-level inverter when both used a LC filter [8].

This paper focuses on reducing the switch count of a five-level LLC resonant DC-DC boost converter. The proposed modification reduces the switch count of the existing cascaded five-level LLC boost converter with eight switches by at least 25%. Although the switch count reduction is advantageous for cost-effectiveness, an increased voltage stress concern is introduced on certain switches for short durations. Moreover, a higher blocking voltage rating for power switches and diodes is expected [9]. Furthermore, the modification introduces diode-bypassed DC-link and neutral-point inverter topologies [10], reducing the control complexities with fewer switches. A variable frequency controller was implemented to achieve both ZVS and ZCS for the switches and rectifier diodes over a wide input voltage and load range. The two proposed converters have been tested in simulation under various load and input voltage conditions to determine the performance and behavior. Besides, a RC simulation model using a CHBMLI with the same specifications and control mechanism at a different inductance ratio was designed and tested under various input voltage and load conditions for the behavior and performance comparison of the multilevel LLC resonant boost voltage converter.

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II. CIRCUIT CONFIGURATION

The proposed five-level inverter aims to produce a five-level output waveform (-Vin, -½Vin, 0Vin, ½Vin, Vin), where each step voltage is ½ Vin. The LLC resonant tank and transformer gain curve must stay within the maximum (*Mg_max*) and minimum (*Mg_min*) limits, allowing determination of the normalized switching frequency at both minimum (*Fn_min*) and maximum (*Fn_max*) values. The full-bridge rectifier is designed to produce a constant DC voltage with a ripple factor of 0.5%. The system control specification targets the variable frequency controller's performance when simulating the five-level diode-bypassed DC-link converter (5L-DBDLRC) under varying input and load conditions. Once the frequency controller is finalized, the five-level diode-bypassed neutral-point converter (5L-DBNPRC) and five-level cascaded H-bridge converter (5L-CHBRC) are simulated and their results evaluated for comparison.

A. Proposed Five-level Multilevel Inverter Topologies

The diode-bypassed five-level DC-link inverter circuit as constructed in Fig. 1**Error! Reference source not found.**, requires two isolated symmetric input DC sources with a magnitude of 125V (half the nominal 250V input voltage). The switching frequency of the gate pulse generator is set to 100kHz. The gate pulse generator consists of a triangle signal generator in Fig. and the comparator circuit in Fig. (a). The gate terminal of switches S1, T1, T2, T3 and T4 is triggered at a specific duty cycle as depicted in Fig. . The output voltage is measured across the Ro. The simulation stop time of the circuit is set to 30µs in Simulink software.

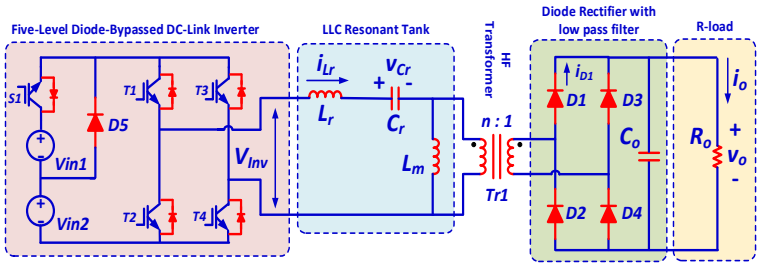


Fig. 1. The proposed five-level diode-bypassed DC-link converter

The steps are repeated for the diode-bypassed five-level neutral point inverter circuit as constructed in Fig 2**Error! Reference source not found.**. It requires four isolated symmetric input DC sources with a magnitude of 125V (half the nominal 250V input voltage). The same triangle signal generator is applied but the comparator circuit is shown in Fig. (b), where the gate terminal of switches S1, S2, T1, T2, T3 and T4 is triggered at a specific duty cycle.

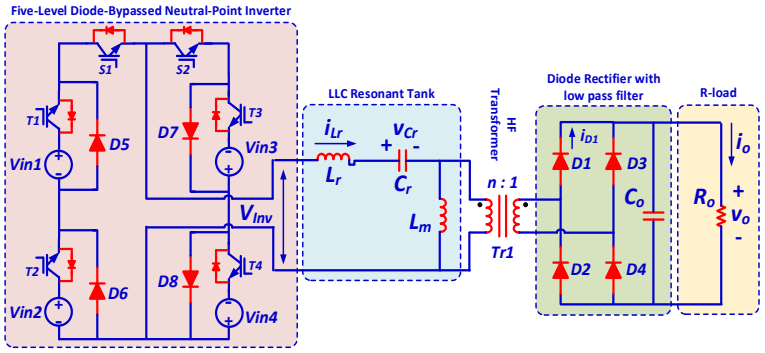


Fig. 2. The proposed five-level diode-bypassed neutral-point converter

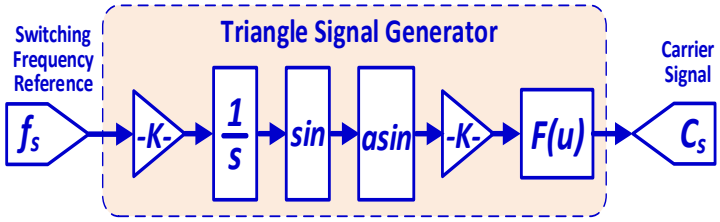
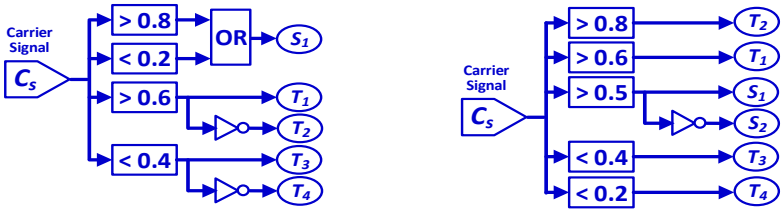


Fig. 3. Block diagram of the frequency modulation



(a) (b)

Fig. 4. Block diagram of comparators of the five-level diode-bypassed (a) dc-link inverter and (b) neutral-point inverter

B. LLC Resonant Tank and Transformer

The parameters of the resonant tank are computed based on the design specifications of the suggested converter as listed in Table 1**Error! Reference source not found.**. The LLC resonant converter has two resonant frequencies, *fr*1 and *fr*2 which can be computed as shown:

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{2}$$

where *Lr* is the resonant inductance, *Cr* is the resonant capacitance, *Lm* is the magnetizing inductance.

The LLC RC's DC voltage gain function, consisting of the normalized switching frequency, *Fn*, inductance ratio *Ln*, and load quality factor *Q*, can be expressed as:

$$M_{gain}(F_n, L_n, Q) = \frac{F_n^2 \times L_n}{\sqrt{\left((L_n+1)\times F_n^2 - 1\right)^2 + \left(F_n \times (F_n^2-1) \times L_n \times Q\right)^2}} \tag{3}$$

$$L_n = \frac{L_m}{L_r} \tag{4}$$

$$F_n = \frac{f_s}{f_r} \tag{5}$$

$$Q = \sqrt{\frac{L_r}{C_r}} \times \frac{1}{R_{ac}} \tag{6}$$

where *Fn* is normalized switching frequency, *fs* is the switching frequency, and *Ln* is the inductance ratio between *Lm* and *Lr*.

$$n = \frac{V_{\text{in}_{\text{nom}}}}{V_{out}} \times M_{\text{nom}} = \frac{250}{1000} \times 1.05 = 0.2625 \tag{7}$$

The n is the transformer turns ratio, M_{nom} is the required gain of LLC resonant tank at nominal output power at nominal input (Vin_{nom}) and rated output voltage (V_{out}). M_{nom} should be 1 or slightly above 1 which is 1.05 in this design.

$$M_{\text{min}} = \frac{n \times (V_{\text{out}} + 2V_F)}{V_{\text{in}_{\text{max}}} + V_F} = 0.87356 \tag{8}$$

$$M_{\text{max}} = \frac{n \times (V_{\text{out}} + 2V_F + V_{\text{loss}})}{V_{\text{in}_{\text{max}}} + V_F} \times 1.1 = 1.5139 \tag{9}$$

The rectifier diode forward voltage (VF) is set to be 1.24V for both the inverter circuit and secondary side rectification. The M_{max} is multiplied by 1.1 to allow the converter to operate within the inductive zone with a 110% overload-current capability. A full-load efficiency of 95% is assumed for the converter. With the output voltage of 1000V, then the 5% power loss at a full-load current of 5A would contribute to the output voltage drop of

$$V_{\text{loss}} = \frac{\frac{5000\ W}{95\%} \times 5\%}{5\ A} = 52.6316V \tag{10}$$

By referring to the turn ratio, n in step 1, the equivalent load resistance that gets reflected from the secondary side can be calculated as:

$$R_{ac} = \frac{8n^2}{\pi^2} R_L = \frac{8(0.26)^2}{\pi^2}(200) = 10.9589\ \Omega \tag{11}$$

An attainable peak gain (*Mg_ap*) curve is plotted to show the *Mg_ap* at different values of *Ln* and *Q*. Based on the *Mg_ap* curves with a gain value always higher than the required *Mg_max* value at a particular *Qmax*, the possible range of *Ln* values can be determined. Fig. shows the plotted *Mg_ap* curves above the *Mmax* of 1.5139. At the *Qmax* value of 0.3, the gain curve at *Ln* values of 3, 4, 5 and 6 are plotted. Fig. shows the gain curve where *Fn_min* = 0.55 and *Fn_max* = 1.528 at *Qmax* = 0.3 and Ln = 5.

Hence, the *Qmax* and Ln values have been chosen to be *Qmax* = 0.3 and *Ln* = 5 to achieve a sufficient voltage gain, targeted performance and the expected characteristics of the proposed converter.

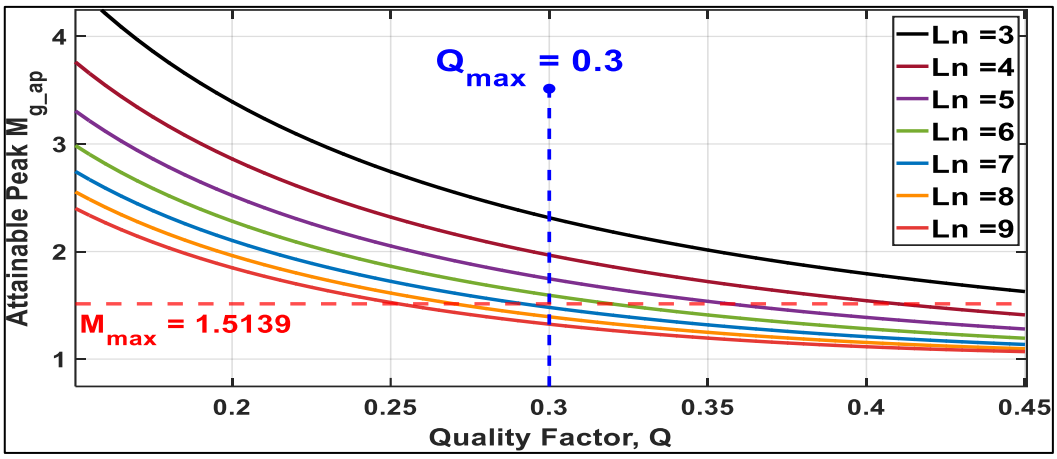


Fig. 5. M_{g_ap} curve for different values of L_n at Q_{max} = 0.3

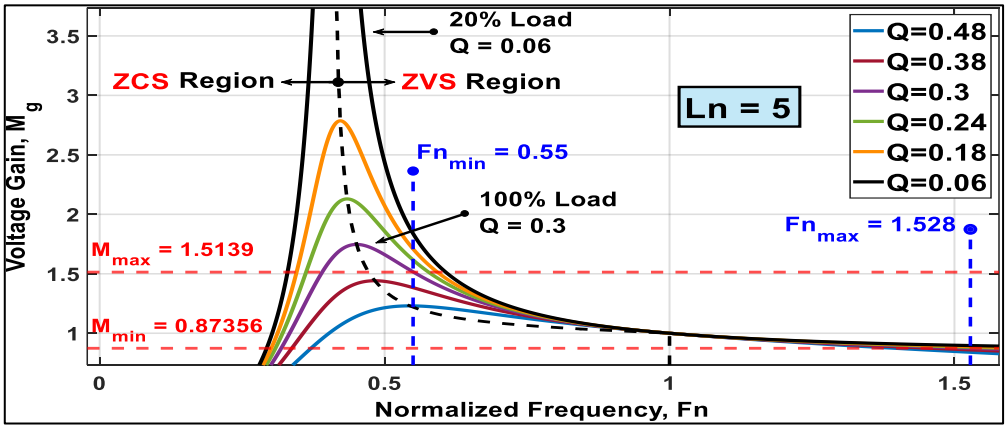


Fig. 6. Voltage gain curves of the proposed converter at varying load factors (Q) with constant Ln = 5

TABLE 1. Specifications of proposed converter

Parameter	Symbol	Values
Maximum Input Voltage	$V_{in,\ max}$	300 V
Rated Input Voltage	$V_{in,\ nom}$	250 V
Minimum Input Voltage	$V_{in,\ min}$	200 V
Output Voltage	V_{out}	1000 V
Output Current	I_{out}	5 A
Output Resistance	R_{out}	200 Ω
Output Power	P_{out}	5000 W
Resonance Frequency	f_r	100kHz

Estimated Efficiency	E_{ff}	95%

Based on the gain curve in, the resulting minimum and maximum operating frequencies can be calculated by multiplying Fn_min = 0.55 and Fn_max = 1.528 with the fr1 = 103.82kHz, resulting in fs,min = 57.10kHz and fs,max = 158.64kHz.

C. Variable Feature Controller

The proposed variable frequency controller shown in Fig. , built in Simulink for the 5L-DBDLRC and 5L-DBNPRC, ensures a constant output voltage despite input and load changes while maintaining ZVS for switches and ZCS for rectifier diodes. It adjusts the switching frequency based on the voltage error between the target 1000V and the output. The gate pulse generator generates signals for each switch, with the switching frequency limited to 57.10kHz to 158.64kHz. The PI compensator uses proportional and integral gains (Kp = 22.057, Ki = 49703) to improve open-loop response. A 300ns time delay simulates the switches' dead time. Further details on transfer functions and equations are in [11].

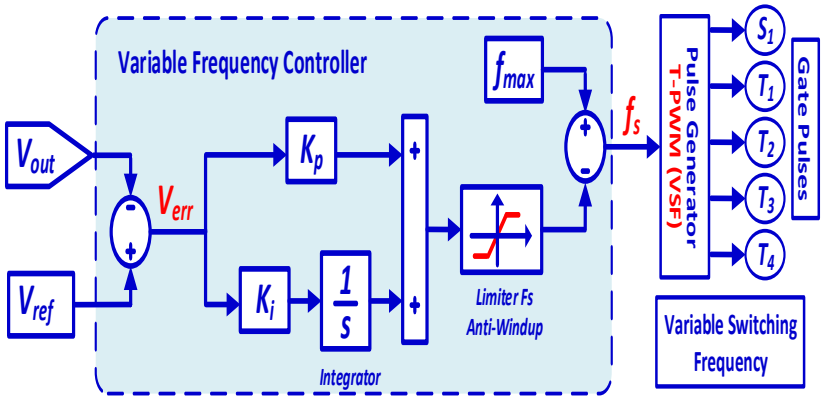


Fig. 7. Block diagram of the closed-loop control strategy for the proposed system

TABLE 2. List of input and load-changing conditions

Input Voltage, V_{in} (V)	Load Condition, I_{out} (A)
250 to 200	100% Load (5A)
250 to 300	100% Load (5A)
250	100% (5A) to 20% (1A) Load
250	20% (1A) to 100% (5A) Load

III. RESULTS AND DISCUSSION

A. Proposed Five-level Inverter Topology

After the simulation time of 30μs, both diode-bypassed DC-link and neutral-point inverter circuits generate the five-level voltage waveform as shown in Fig. 8. Hence, the number of switches is reduced to 5 to obtain the five-level output voltage waveform (+2Vdc, +Vdc, 0Vdc, −Vdc, −2Vdc) where each step voltage (Vdc) is 125V which halves the input voltage of 250V.

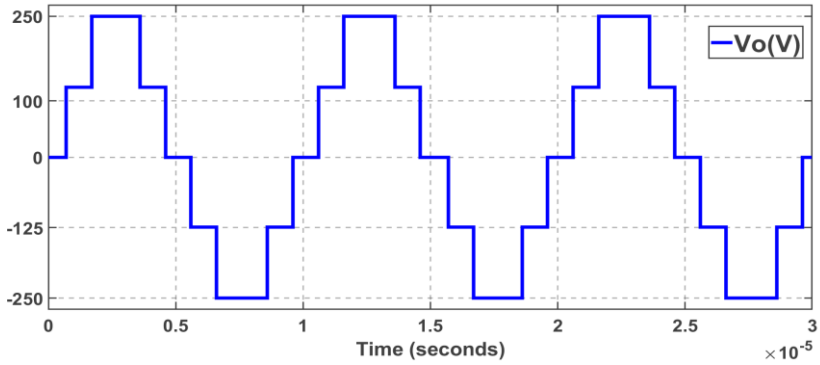


Fig. 8. Output voltage waveform of both five-level diode-bypassed DC-link and neutral-point inverters

B. Proposed Resonant Converter

1) Five-level DC-link resonant converter

The *Kp* and *Ki* values are set to 290 and 75000 to improve control performance. Fig. 9 shows the gate-to-emitter (VGE) and collector-to-emitter (VCE) waveforms for all switches (T1, T2, T3, T4, S1) at a 250V input and full load with *fs* at 73.13kHz. VCE drops to zero before VGE turns on T1, T2, T3, and T4, but S1's VCE remains at 125V due to a 300ns dead time. All switches theoretically operate under ZVS conditions.

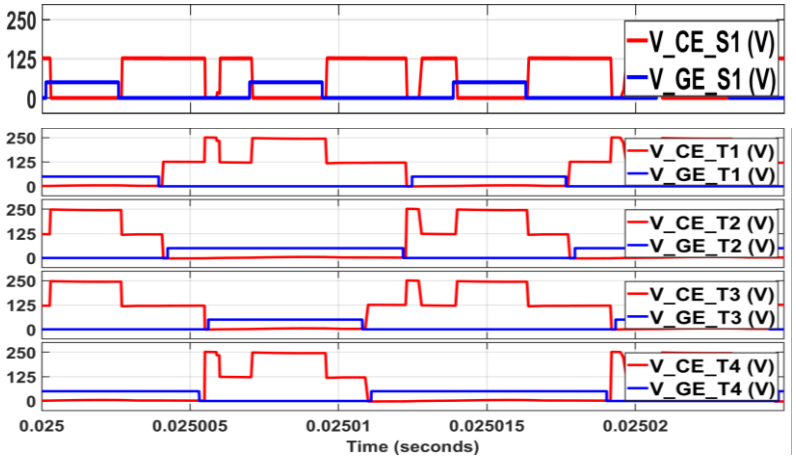


Fig. 9. The VGE and VCE simulation waveforms of switch T1, T2, T3, T4, S1

Fig. 10 shows diode voltage (VD) and current (iD) waveforms, demonstrating ZCS for all diodes, with iD waveforms multiplied by a gain of 25.

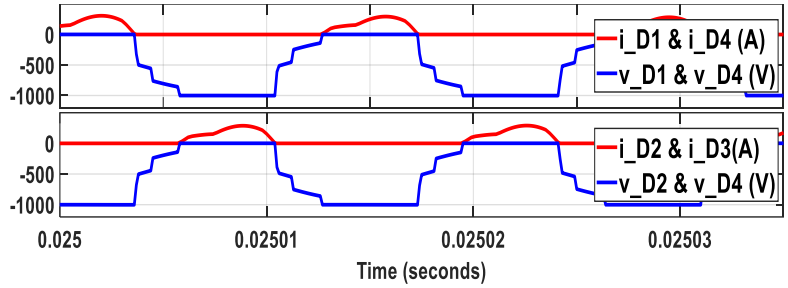


Fig. 10. Diode voltage (VD) and diode current (iD) simulation waveforms of diode D1, D2, D3 and D4

Fig. 11 shows the resonant tank simulation waveforms for the five-level DBDLRC, including inverter output voltage (*VInv*), resonant inductor current (*iLr*), resonant capacitor voltage (*VCr*), and transformer primary voltage (*VLm*). The VInv waveform has distortion at +Vdc and -Vdc levels, achieving reduced switch count but increasing VLm to 263.4V. The *iLr* and *VCr* waveforms peak at 59A and 234.6V. Fig. 12 presents the output simulation waveforms (fs, VO, IO, PO), demonstrating that the controller maintains a consistent 1000V output, 5000W power, and 5A current. The switching frequency stays stable at 73.12kHz, below the resonance frequency, indicating proper operation.

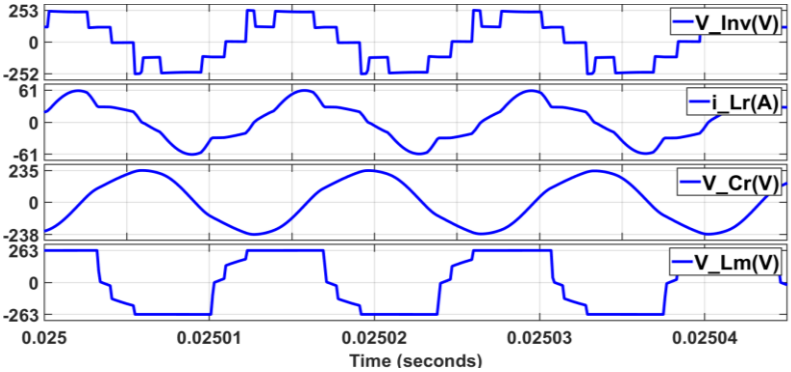


Fig. 11. VInv, iLr, VCr, and VLm simulation waveforms at 250V input and full load condition

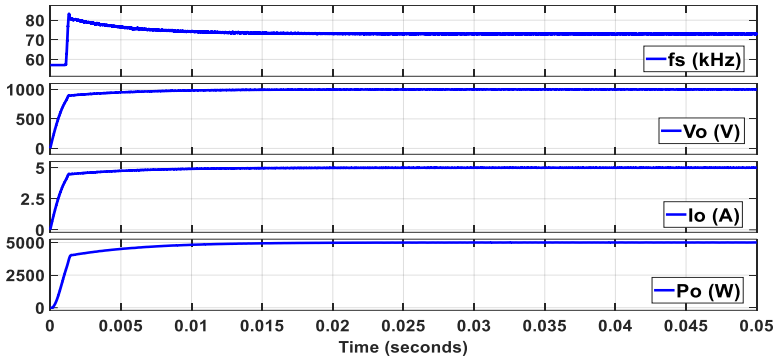


Fig. 12. The fs, VO, PO and IO simulation waveforms

To evaluate control stability, the system was tested with varying input voltages at full load. In the first case, Vin decreased from 250V to 200V at 0.03s. Fig. 13 shows that fs decreased from 73.13kHz to 60.42kHz, with Vo dropping by 46.446V and recovering in 3.298ms. In the second case, Vin increased from 250V to 300V at 0.03s. Fig. 14 shows fs increased from 73.09kHz to 87.98kHz, with Vo rising by 48.56V and stabilizing in 3.693ms. These results demonstrate that the switching frequency adjusts to input variations, maintaining a constant 1000V output.

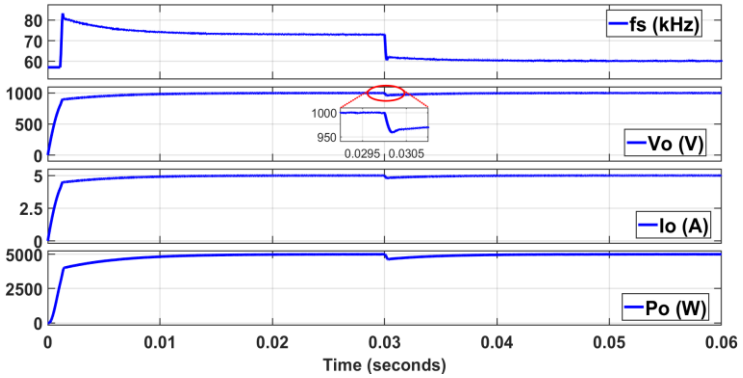


Fig. 13. The dynamic response of the proposed control when Vin is changed from 250 V to 300 V; fs, VO, IO and PO

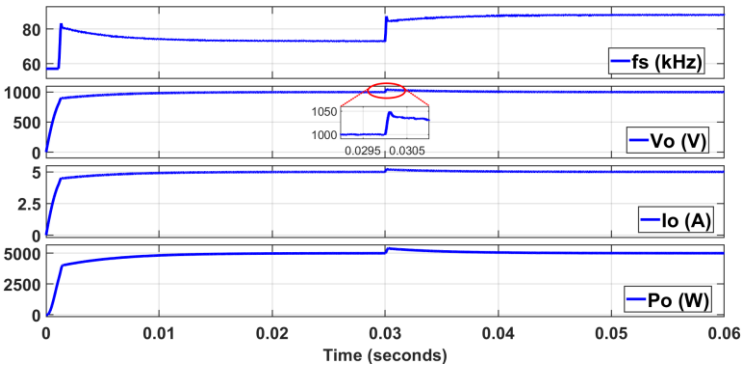


Fig. 14. The dynamic response of the proposed control when Vin is changed from 250 V to 300 V; fs, VO, IO and PO

The converter is also tested against two load-changing conditions with a Vin of 250V to determine the stability of the proposed controller. The first case is the simulation starts with a full load of 5A and reduces the load to 20% at 1A at 0.03s of the simulation. Fig. shows that the switching frequency is reduced from 73.09kHz to 87.61kHz. An output voltage overshoot of a maximum of 32.4V is observed. Moreover, about 3.492ms is used to go back to a steady condition. The second case started with a 20% load of 1A and proceeded with a load increment to a 100% load of 5A at 0.03s. When the load increases to 100%, the switching frequency of 87.66kHz is reduced to 73.05kHz as shown in Fig. . The output voltage drops by 43V and takes about 3.758ms to return to a steady condition of 1000V within ±20V.

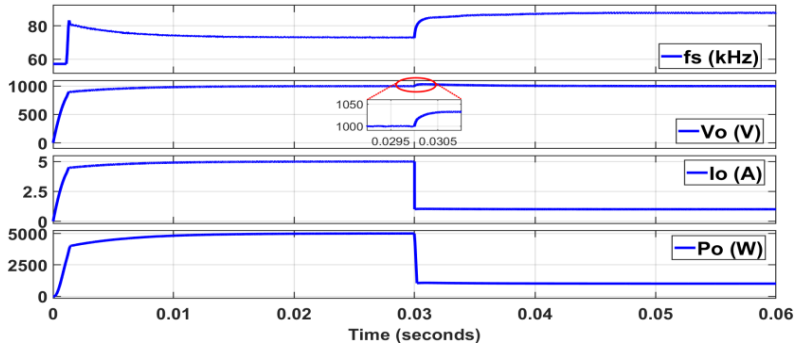


Fig. 15. The dynamic response of step-down load condition (from 100% load to 20% load), switching frequency fs, output voltage VO, output current IO, and output power PO

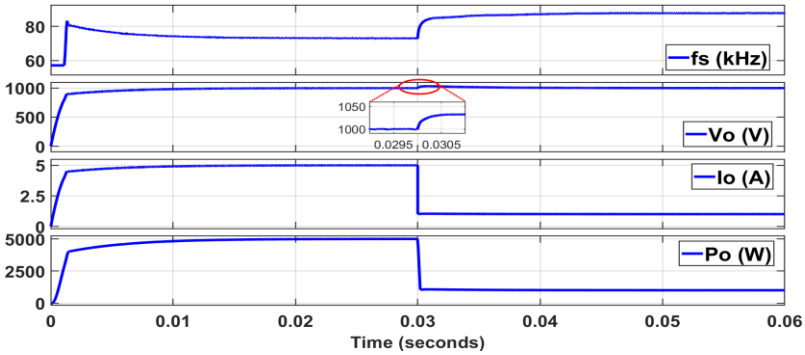


Fig. 16. The dynamic response of step-up load condition (from 20% load to 100% load), fs, VO, IO, and PO

2) Five-level neutral point resonant converter

The 5L-DBNPRC simulation results are similar to the 5L-DBCLRC, with the key difference being that a 1000V output cannot be achieved at the minimum switching frequency of 57.10kHz when Vin drops from 250V to 200V. To address this, fs,min was set to 51.91kHz, increasing the maximum voltage gain as shin in Fig. 17.

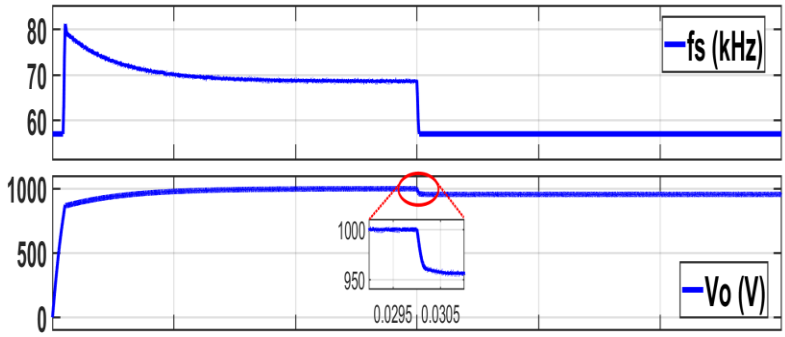


Fig. 17. The dynamic response of the proposed control for 5L-DBNPRC when Vin is changed from 250 V to 300 V; fs, VO, IO and PO

3) Five-level cascade H-bridge resonant converter

Since the voltage gain of Ln = 5 at minimum switching frequency is not enough to maintain the Vo of 1000V, the *Kp* and *Ki* values of the controller are recalculated and adjusted based on Ln = 4 to increase the boost gain. Thus, the Lm value is set to 20µF. Fig. shows the resonant tank waveforms, consisting of the VInv, iLr, VCr, and *VLm* for the 5L-CHBRC. The five-level *VInv* waveform is slightly distorted overall. It is believed to increase the maximum value *VLm* to 263.2V rather than the expected voltage of 250V. The *iLr* and *VCr* have peak values of 70.26A and 269V, respectively.

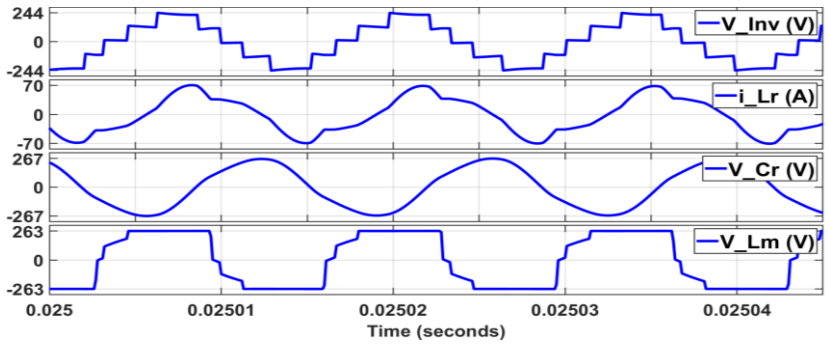


Fig.18. VInv, iLr, VCr, and VLm simulation waveforms at 250V input and full load condition

The multilevel LLC RC behavior was tested using a five-level cascaded H-bridge inverter under input voltage variation and full load. In the first test as depicted in Fig. 19, Vin was reduced from 250V to 200V at 0.03s, causing the switching frequency to drop from 74.27kHz to 62.89kHz. The output voltage decreased by less than 46V and stabilized in 3.772ms. In the second test, Vin was adjusted from 250V to 300V, increasing the switching frequency from 74.27kHz to 87.34kHz. The output voltage rose by 51.83V, with a transient response time of 4.227ms to reach a steady 1000V as illustrated in Fig. 20.

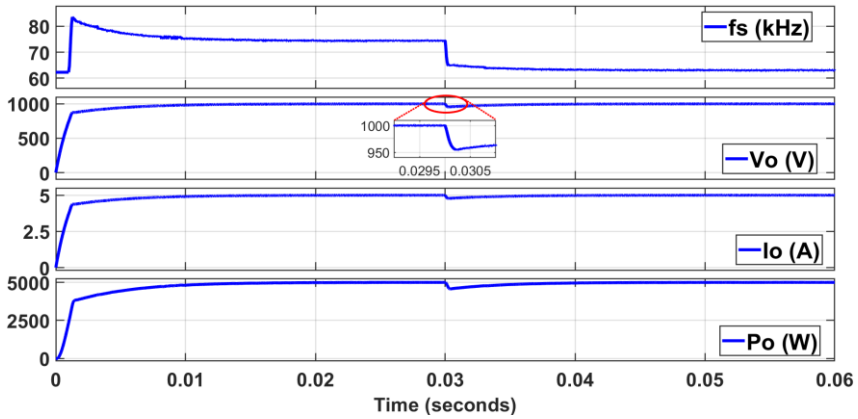


Fig. 19. The dynamic response of the proposed control when Vin is changed from 250V to 200V; switching frequency fs, output voltage VO, output current IO and output power PO

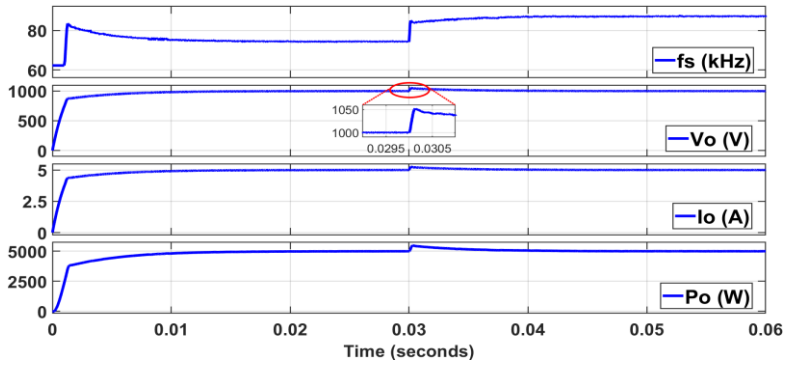


Fig. 20. The dynamic response of the proposed control when Vin is changed from 250V to 300V; switching frequency fs, output voltage VO, output current IO and output power PO

Fig. represents the power loss distribution of the proposed converters (5L-DBDLRC and 5L-DBNPRC) and the 5L-CHBRC at full-load condition in terms of the total IGBT conduction power losses, 291.79W (DBDLRC) and 283.04W (DBNPRC) are less than 592.59W (CHBRC) by at least 50%, proving the IGBT conduction loss reduction by reducing the switch count. The diode losses of the two proposed converters consist of bypassed and rectifier diodes, instead of only rectifier diode losses in the CHBRC. Therefore, the diode losses of 28.14W (DBDLRC) and 37.90W (DBNPRC) are at least 50% more than the 13.58W (CHBRC).

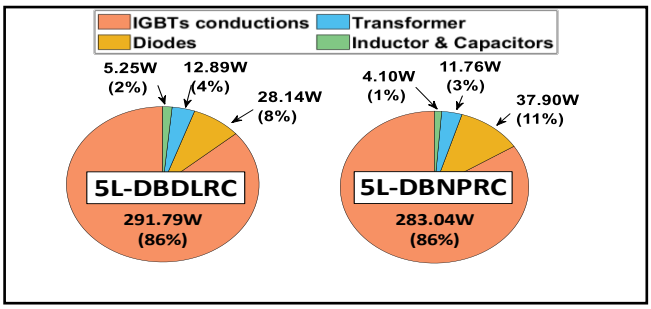


Fig. 21. Power loss distribution of the five-level DBDLRC, five-level DBNPRC, and five-level CHBRC at full load condition

Fig. 22 shows the efficiency of the DBDLRC, DCNPRC, and CHBRC at a nominal input voltage of 250V under varying loads. The maximum efficiency of the five-level DBDLRC (94.51%) and DBNPRC (94.40%) surpasses the CHBRC (89.29%). At full load, the 5L-DBDLRC and 5L-DBNPRC achieve efficiencies of 93.66% and 93.68%, respectively, compared to 88.86% for the CHBRC. The maximum efficiency difference between the proposed converters and CHBRC is 8.81% at 0.5A load and 5.28% at 5A load. The 5L-DBDLRC achieves 93.66% full-load efficiency using just five switches and one bypass diode, compared to the 5L-DBNPRC, despite a 0.02% efficiency difference. The 5L-DBDLRC shows higher efficiency than the DBNPRC across load conditions, with an increase of 0.14% to 1.69% for 0.5A to 3A loads, and a slight decrease of 0.02% to 0.2% for 3.5A to 5A loads. Overall, the 5L-DBDLRC appears to be a more practical option for industrial and high-voltage applications.

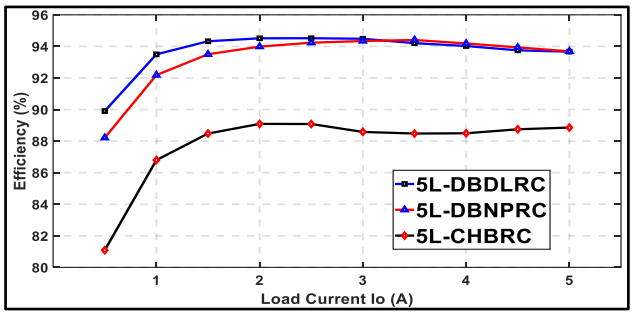


Fig. 22. Efficiency measurements vs different loading conditions for the converter configurations at 250V input

The simulation results for both 5L-DBDLRC and 5L-DBNPRC revealed that the behavior of the LLC circuit with a five-level diode-bypassed DC-link and neutral-point inverter is the same to its typical performance with cascaded H-bridge inverters. Specifically, the switching frequency (fs) is always lower than the resonance frequency, regardless of load and input conditions, as shown in Table 3.

TABLE 3. Comparison between converter configurations under different input voltage and the full load condition

Input Voltage Ranges, Vin	Switching Frequency, fs (kHz)		
	5L-CHBRC	5L-DBDLRC	5L-DBNPRC
High Input Voltage (300V)	87.34	88.98	83.16
Nominal Input Voltage (250V)	74.27	73.09	68.76
Low Input Voltage (200V)	62.89	60.42	52.88

IV. CONCLUSION

This paper presents a reduced-switch five-level LLC resonant DC-DC boost converter with a variable frequency control strategy for high-voltage applications. The converter design uses a lower switch count to improve efficiency, with a higher inductance ratio (Ln) of five in the resonant circuit compared to the CHBRC's Ln of four, reducing resonant current and conduction losses. Although ZVS is not achieved for all switches, ZCS is obtained for all rectifier diodes in both proposed converters. The converters show similar resonant behavior to the 5L-CHBRC, with operating frequencies always below the resonant frequency. They were tested under varying input voltages (200V to 300V) and load conditions (20% to full load), demonstrating a fast response to maintain a

constant 1000V output. Simulink simulations verified the design, showing the five-level DBDLRC achieves 93.66% full-load efficiency with fewer switches and bypass diodes, making it a more suitable solution for high-voltage applications.

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