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Design of High-Speed 16-Bit Flash ADC for OFDM Receiver Channel Estimation

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Abstract: - This research presents a highly efficient 16-bit two-step flash ADC for optimum receiver channel estimation in OFDM systems. The ADC employs an innovative architecture based on multiplexers, including low-power latched comparators, multiplexers, and a multiplexer-based encoder, which results in fewer comparators and higher performance while keeping a compact design and low power consumption. It delivers an outstanding signal-to-noise ratio, effective resolution, and figure of merit at a given sampling rate. The research provides an innovative approach for improving accuracy and resource economy in OFDM systems: integrating compressive sensing with a 16-bit flash ADC. This hybrid approach improves high-resolution OFDM channel estimation, allowing for exact estimate with fewer samples and less memory. The 16-bit flash ADC delivers great performance, with low power consumption, a smaller in size, and fast operation. Moreover, integrating compressive sensing significantly improves accuracy and resource efficiency in OFDM channel estimation, allowing for precise estimation with reduced comparators about 130 and computational needs. These advancements hold great promise for enhancing OFDM system performance, especially in resource-constrained scenarios.

Keywords: 16bit flash ADC, Low power comparator, Multiplexer, Low power ADC, Low area ADC, High speed ADC, OFDM receiver channel estimation, Compressive Sensing Technique.

I. INTRODUCTION

In the field of digital communication, Orthogonal Frequency Division Multiplexing (OFDM) stands out for its efficiency and resistance to fading and interference. Accurate channel estimate in OFDM systems is dependent on the high resolution and speed of Analog-to-Digital Converters (ADCs). This paper emphasizes the need of 16-bit flash ADC architecture and high-resolution channel estimation.

The research begins by providing a collaborative method to Distributed Compressed Sensing (DCS). This method strikes a delicate balance between efficiency and data quality by utilizing feedback via residuals and grouping the reconstruction of common and novel signal components. The collaborative approach reduces reconstruction measurements while increasing efficiency and accuracy, making it an effective solution for DCS applications [1].

Moving on, the study explores into the world of MC-CDMA systems. These systems, which are known for their high data throughput and spectrum efficiency, confront issues as a result of carrier frequency offset. To overcome this issue, the study presents a unique residual CFO compensated adaptive subcarrier power distribution technique. This strategy optimizes power allocation to subcarriers with high channel-to-noise power ratios, resulting in increased system capacity and picture compression for high-quality multimedia transmission (2). Another feature of MC-CDMA systems is that they are sequential. While necessary for broadband wireless networks and LTE standards, these systems face the negative consequence of carrier frequency offset (CFO), which introduces intercarrier interference (ICI). The work presents the receiver phase rotated conjugate cancellation (RPRCC) technique, which successfully reduces ICI, particularly in circumstances with several closely spaced CFOs. This strategy surpasses prior algorithms and provides a useful solution for MC-CDMA systems [3]. Finally, the study discusses the difficulties encountered by Multiple Input Multiple Output (MIMO) systems utilising orthogonal frequency division multiplexing (OFDM). The existence of a carrier frequency offset (CFO) causes intercarrier interference, which affects system performance. To address this, the study proposes a pilot-aided interpolation method for estimating and correcting CFO and channel effects. This method improves the bit error rate performance and carrier-to-interference power ratio (CIR) of MIMO-OFDM systems, resulting in improved overall system performance [4].

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The proposed technology combines compressive sensing with a two-step 16-bit flash ADC architecture that uses multiplexers to decrease the number of needed components. This technique simplifies the ADC design while ensuring accurate channel estimate in OFDM systems. Specifically, designing system requires $2^{(N-3)}+2$ preamplifiers and $2^{(N-2)}+1$ comparators averaging approach [5], whereas traditional design requires $2^{N}-1$ of each. By using fewer components, our system has a smaller overall size, lower energy consumption, and quicker operation due to lower input capacitance. Figure 1 depicts the block diagram of an 8-bit Flash ADC with multiplexers.

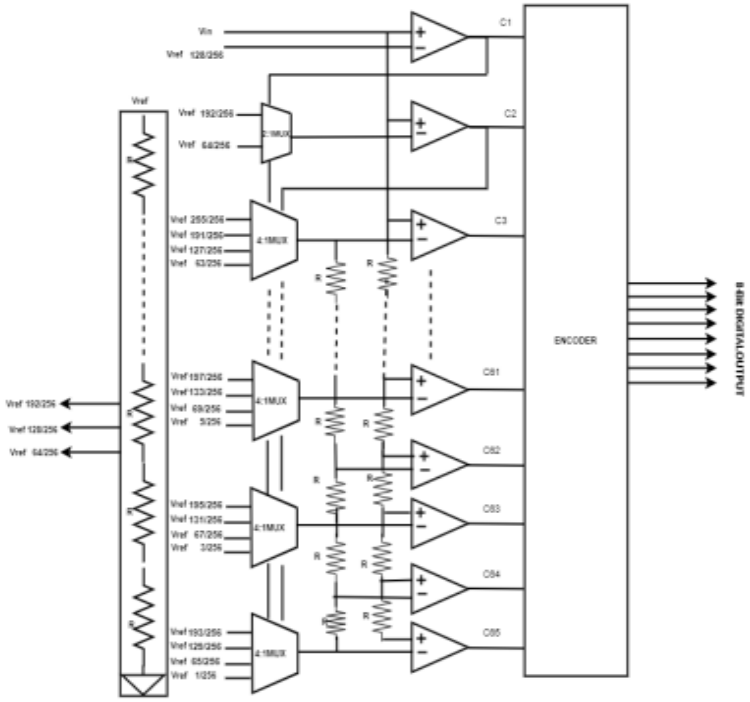

Figure 1: Mux based 8bit flash Analog-to-digital converter novel architecture

The system is made comprised of various components, including a reference ladder [6], a passive track and hold (T/H) circuit, preamplifiers, comparators, multiplexers, and logic gates for register and encoding. In the aforementioned architectural design, the first comparator, C1, determines the most significant bit (MSB) by comparing the input signal to a reference level. The MSB signal controls the multiplexers, while the second comparator, C2, selects various reference values using a (2:1)-MUX. The remaining comparators, C3-C65, get their reference voltages from (4:1)-MUXs. Additionally, an interpolation approach using two resistors is used to minimize the number of components. The interpolation approach with two resistors generates intermediate reference voltages, allowing for precise analog-to-digital conversion while reducing the number of comparators and reference levels in the ADC. The comparators' outputs are encoded, and digital bits are output simultaneously.

According to the power consumption of ADC is

$$P_{ADC} = 2^{b} \times F_{s}$$

Where 'b' represents quantization accuracy and 'Fs' represents sampling rate, reducing 'b' exponentially decreases power consumption in flash ADCs. Additionally, lowering the number of comparators in these ADCs helps to reduce power usage. High-resolution ADCs have minimal hardware costs and implementation complexity. Furthermore, processing and sending data represented by fewer bits is simpler, easing quality expectations for radio frequency (RF) and interface circuits, resulting in decreased power consumption.

OFDM System

The analogue signal cannot be utilized directly in the OFDM receiver's FFT portion because the FFT circuit only analyses discrete-time signals. Figure 6 shows the A/D converter transforming analogue signals into discrete-time OFDM signals.

High-resolution channel estimate [7] is critical for accurately estimating the wireless channel's frequency response in an OFDM system, as seen in Figure 2. Traditional solutions based on high-resolution ADCs might increase complexity and power consumption. To solve these issues, researchers have considered alternate ways, such as creating high-resolution Flash ADCs with few components. Compressive sensing-based channel estimation approaches use the sparsity of the frequency domain channel response to achieve accurate estimate with less sampling. Algorithms such as Basis Pursuit and Orthogonal Matching Pursuit are used to estimate the sparse channel while minimizing hardware complexity and energy usage. These approaches are appropriate for practical application in OFDM systems, particularly in resource-constrained contexts like as mobile devices.

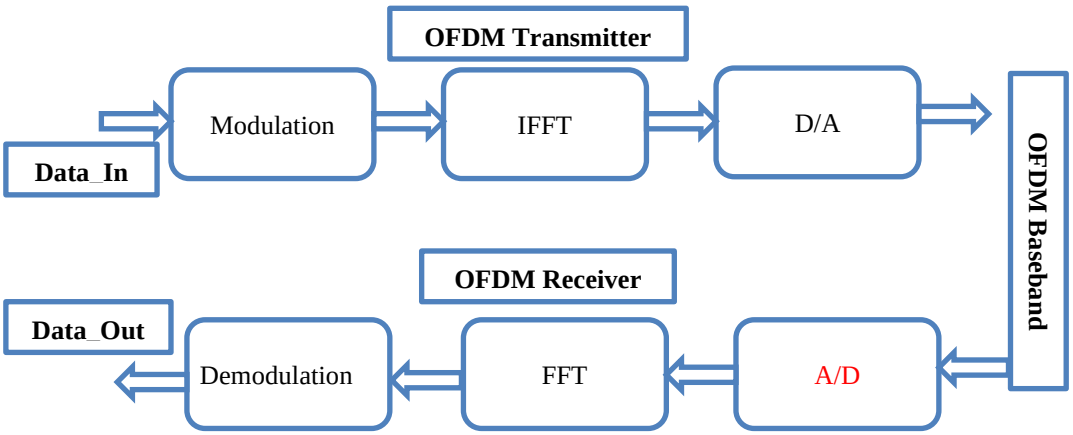

Figure 2: Basic block diagram of OFDM system Tx and Rx

The modulated signal X(k) includes a known pilot signal, guard band, and N-point. To reduce inter-subcarrier interference, a cyclic prefix is used. The Inverse Fast Fourier Transform (IFFT) transfers the signal to the time domain, providing x(n), where n ranges from 1 to N. A digital-to-analog converter (DAC) converts the time domain signal to analogue before it is sent. The analogue signal is then sent with a clock frequency of 1/Ts, where Ts is the sampling period.

$$h(n) = \sum_{p=1}^{p} \propto_p \delta\left(n - \tau_p T_s\right), \quad \text{n=1,2, 3,..N,} \quad (1)$$

The channel response of a communication system consists of P propagation pathways. This answer is represented as a complex-baseband vector in the time domain, with P taps corresponding to the various pathways. The multipath component is restricted by the delay Tp, defined as $0 < Tp \leq Tg$, where Tg represents the period of an OFDM signal, as indicated in equation (1). Because of the concentration of non-zero impulse response at the start, signals having many pathways, represented by h = [h1, h2,..., hN, 0,..., 0], can only have N non-zero values. The receiver receives the channel response signal after removing interference and considering the channel response pulse noise.

$$z(n) = x \otimes h + \xi \qquad (2)$$

The high-resolution flash ADC receives a pulse noise signal formed by convolving the modulated signal 'x' and the impulse response 'h' with sampled Gaussian noise. The cyclic prefix is eliminated, and the resultant signal Z(n) is sampled to get the samples y(m), with n ranging from 1 to N and m ranging from 1 to M. The conventional channel estimate algorithms used in OFDM systems generally employ M=N. If M is smaller than N, the signal y is down sampled from Z and transformed to Y(k), where k varies between 1 and M, after eliminating the guard band and pilot signal. Finally, a final M-point FFT is performed to obtain 'X', which is then developed and reconstructed from 'Y' using the pilot signal for channel estimation [8-14].

Compressive Sensing

Compressive Sensing (CS) techniques exploit channel impulse response sparsity for efficient channel estimation in OFDM systems. Using a 16-bit ADC enhances resolution and dynamic range, improving accuracy and reducing quantization noise. The flexibility of a higher-resolution ADC allows for system optimization by adjusting transmitter DAC sampling rates or reducing receiver ADC speed. CS-based channel estimation with a 16-bit ADC is valuable for 5G and advanced systems, accurately recovering sparse signals and effectively capturing channel

sparsity. According to references [15-16], Compressive Sensing (CS) theory allows for exact reconstruction of a sparse signal (h) with S non-zero coefficients using linear measurements ($y = \Phi h + \xi$). In this equation, Φ is a matrix with M rows and N columns, where M is the number of measurements and N is the signal length. $M < N$.

The CS framework aims to minimize the $\ell 1$-norm of the sparse signal h, enabling stable recovery of the original signal under certain conditions. In classical CS, the matrix Φ, suitably scaled, is assumed to satisfy the restricted isometry property (RIP). The RIP condition guarantees that Φ preserves the norm of sparse signals, ensuring that $(1 - \delta) \|h\|_2^2 \leq \|\Phi h\|_2^2 \leq (1 + \delta) \|h\|_2^2$ for all S-sparse signals h, where $\delta > 0$ is the RIP parameter. To elaborate, the pilot symbol X(k) is sampled individually, with F representing the discrete Fourier transform. Using the convolution theory, x ⊗ h = F^ (-1) (F(h)·F(h)), whereas x = F^ (-1) (X). Thus, x ⊗ h equals F^ (-1) diag(X)Fh. Therefore, the measurement y may be stated as follows:

$$y = \downarrow \Omega \, (Ch + \xi) = \downarrow \Omega \, (F^{-1} diag(X) Fh + \xi) . \quad (3)$$

The equation (3) is referenced to be part of a mathematical model commonly used in communication systems literature, particularly in the context of channel estimation. The literature citations [17-21] suggest that this model is part of established practices and methodologies within the field.

II. SURVEY OF LITERATURE

[22] In this paper, a new Q-OFDM receiver architecture is introduced, which incorporates a robust linear OFDM channel estimator and the generalized Turbo framework. The architecture includes automatic gain control, noise power estimation, and synchronization schemes, enabling reliable data transmission using low-resolution analog-to-digital converters. Numerical simulations and over-the-air experiments validate the efficacy of the proposed approach. [23] In this paper, a novel approach using deep learning is presented for joint pilot design and channel estimation in mixed-ADCs mm Wave massive MIMO systems. The method utilizes a pilot design neural network, a model-driven densely connected network, and an end-to-end architecture inspired by autoencoders. Through simulations, it is demonstrated that the proposed method surpasses traditional channel estimators and state-of-the-art networks in terms of performance. [7] In this paper, an innovative OFDM channel estimation technique is introduced, incorporating compressive sensing to minimize the number of probing measurements and reduce ADC speed requirements. The proposed system combines $\ell 1$ minimization, iterative support detection, and limited-support least-squares methods to achieve accurate and high-resolution channel estimation even with low-speed ADCs. Through simulations, it is shown that this approach results in a substantial enhancement in signal-to-noise ratio compared to conventional methods. [24] In this research paper, a 3.1-10.6 GHz ultra-wideband receiver is designed and integrated, employing 500 MHz-wide sub-banded BPSK pulses. The system consists of a custom-designed planar antenna, direct-conversion RF front-end, 500 MS/s analog-to-digital converters, and a parallelized digital back-end. Experimental tests reveal the successful establishment of a 100 Mb/s wireless link with a bit error rate (BER) of 10^-3 at a received power level of -80 dBm. [25] In this paper, an innovative online adaptive timing mismatch error estimation technique is introduced for time-interleaved ADCs in an IR-UWB receiver. The proposed method effectively estimates timing errors in various channel conditions and successfully compensates for them, resulting in significant enhancements in the bit error rate (BER). [26] In this paper, a background calibration technique for time-interleaved ADCs is introduced, employing communication protocol redundancy. The technique utilizes pseudorandom modulation sequences embedded in OFDM pilot tones to measure and correct analog circuit imperfections. Through simulations, significant enhancements in signal-to-noise and distortion ratio (SNDR) are demonstrated, with a tracking time constant of 85 ms. [27] This paper introduces a receiver structure for pulsed OFDM systems that reduces complexity by utilizing ADCs with a sampling rate below the Nyquist rate. Through simulations, it is demonstrated that the proposed approach outperforms full-rate sampling and selection diversity combining, while also reducing complexity and power consumption. Additionally, the study suggests that a subset selection algorithm based on training sequences provides minimal performance enhancement.

III. DESIGN METHODOLOGY

The 16-bit two-step Flash ADC employs an 8-bit coarse Flash ADC, an 8-bit current steering DAC, a comparator, a residue amplifier, and a fine 8-bit Flash converter. This architecture enhances resolution and accuracy. Additionally, the proposed N-bit ADC requires fewer preamplifiers and comparators compared to traditional flash

ADCs, resulting in a smaller size, lower power consumption, and improved speed. For example, compared to conventional 8-bit flash ADCs, the proposed architecture reduces preamplifiers by 84% and comparators by 73% (Table 1). The proposed N-bit ADC architecture requires significantly fewer preamplifiers and comparators compared to traditional flash ADCs. Specifically, it needs only $2^{(N-3)}+2$ preamplifiers and $2^{(N-2)}+1$ comparators, whereas a conventional flash ADC requires 2^N-1 preamplifiers and comparators. This reduction in the number of components leads to a smaller size, lower power consumption, and improved operation speed. In fact, compared to conventional 8-bit flash ADCs, the proposed architecture achieves a reduction of 84% in preamplifiers and 73% in comparators (as shown in Table 1).

Table I: Illustrates the comparison of comparators for conventional flash and the proposed structure at various bit resolutions.

Bit Resolution	**Conventional flash**	**Proposed Flash**	**Two-step flash of bits**
n	**2^N-1**	**$2^{N-2}+1$**	**$2(2^{N/2-2}+1)$**
4	15	5	2
6	63	17	6
8	255	65	10
10	1024	257	18
16	**65535**	**16385**	**130**

The MUX-based encoder, which utilizes a MUX and employs a binary search algorithm for encoding, exhibits lower bubble error suppression compared to both the Wallace tree and folded Wallace tree encoders. However, it offers advantages such as reduced hardware requirements and a shorter critical path, making it well-suited for circuits that prioritize lower power consumption.

Instead of using a generic algorithm, the technique is designed to take use of the OFDM system's features. This includes the unique structure of h and the existence of noisy observations in y. The goal is to retain simplicity, minimal complexity, and hardware compatibility. The procedure starts by merging two constraints into one by defining the variable $\tilde{h}$ as [h1, h2,..., h$\tilde{N}$], deleting the other components of h. The matrix (φ) is created using the first N columns of $\tilde{\varphi}$. By simplifying the restrictions to $\tilde{\varphi}\ \tilde{h} = y$, the issue becomes more manageable.

The CS-OFDM method is designed to manage noisy measurements. The inspiration comes from the iterative support detection (ISD) approach introduced in, which is noted for its efficacy even when dealing with noisy data. The method uses ISD and includes a final denoising phase. The primary iterative loop estimates a support set I based on the present reconstruction and provides a new candidate solution. This is accomplished by addressing the minimization issue.

Algorithm: Compressive sensing OFDM

Input: φ, y;

Initialization: Set $\tilde{\varphi}$ as the first $\tilde{N}$ columns of φ.

Set I^0 ($\leftarrow 0$) as an empty set. Set w_i^0

Loop: While the stopping condition is not met, do

- *For i = 1 to $\tilde{N}$:*

Subproblem:

Solve $\tilde{h} \leftarrow arg\ min\ |\widetilde{hi}|$, *s.t.* $\tilde{\varphi}\ \tilde{h} = y$

for ***i*** *not in* $\boldsymbol{I}^{j}$.

- *Support Detection: Update* $I^{j+1} \leftarrow \{i: |\widetilde{h_i^j}| \geq 2\text{^}(-j) * max(|\tilde{h}i|)\}$.
- *Weights Update: Update* w^{j+1}.

Final Least-Squares:

- *Let T be the set* $\{i: |\tilde{h}i| > threshold\}$.
- *Solve* $\tilde{h}_T \leftarrow arg\ min\ ||\tilde{\varphi}T\ \tilde{h}\ -\ y||_2^2$
- *Set* $\tilde{h}_T c \leftarrow 0$.

Return: $\tilde{h}$

The iterative updating of index set I identifies missing spikes and eliminates false spikes. This technique is based on the weighted 1 norm but outperforms it, as proven by the study and numerical results provided. Given that measurements are intrinsically noisy, flawless reconstruction is impossible. The approach includes a final denoising phase that uses a least-squares optimization on the final support set T. This stage seeks to reduce tiny spikes that are likely caused by noise. The pseudocode for the algorithm is described in Algorithm.

OPTIMIZATION

The architecture aims to maintain high speed, low power consumption, low area, and high resolution. The two-step method improves accuracy, and the DAC ensures precise analog voltage representation. Optimization of power and delay as follows from

$$Power\ =\ f_{CLK}\ *\ C_L\ *\ V_{dd}^2\ +\ V_{dd}\ *\ I_{\ leakage} \qquad (1)$$

$$I_{residue\_stage} = I_{t,comp} + (2^{m+1} - 2)I_{comp} \qquad (2)$$

The output peak-peak voltage DAC from the Figure 5 is given by $V_{dac_{p-p}}\ =\ I_{FS}\ *\ R$ (3)

The total impedance observed by the DAC is denoted as R, while I_{FS} represents the full-scale output current

$$V_{loadrms}\ =\ \frac{V_{load_{p-p}}\ )}{(2\ *\ sqrt(2)} \qquad (4)$$

The power at load is given by

$$P_{load}\ =\ \frac{(V_{loadrms})^2}{RL} \qquad (5)$$

$$P_{dBm}\ =\ 10\ *\ log\ \left(\frac{P_{load}}{1mW}\right) \qquad (6)$$

$$Ptotal =\ C_L.\ V_{dd}.\ V_{out}.f_{clk}\ +\ I_{SC}.V_{dd}\ +\ I_{leak}.V_{dd} \qquad (7)$$

The total power consumed by every MUX style can be evaluated using the Eq. 7.

IV. RESULT ANALYSIS

The 16-bit two-step Flash ADC is composed of several components, including an 8-bit coarse Flash ADC, an 8-bit current steering DAC, a residue amplifier, and a fine 8-bit Flash ADC. The 8-bit coarse Flash ADC utilizes 65 comparators to convert the analog input voltage into an 8-bit digital code. The 8-bit current steering DAC converts the output code from the coarse ADC into an analog signal. The residue amplifier amplifies the difference between the DAC output and the input voltage.

Residue amplifier output $V(out) = \begin{Bmatrix} 0, Vin < Vref \\ 1, Vin > Vref \end{Bmatrix}$

This amplified signal is then used as the analog input for the fine 8-bit Flash ADC, which generates the 8-bit least significant bit (LSB) digital output code. Coarse-fine ADC is a technique used in Analog-to-Digital Converters (ADCs) to improve the overall performance and resolution of the conversion process. It involves the use of two stages: a coarse ADC followed by a fine ADC as shown in **Figure 3**.

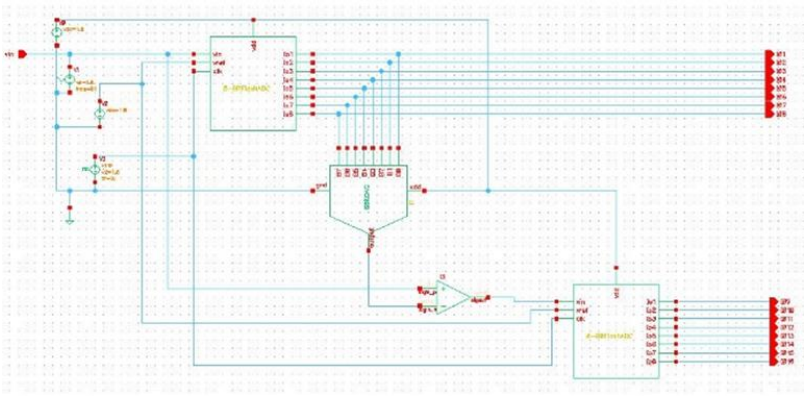

Figure 3: Schematic of two-step 16bit flash analog-to-digital converter

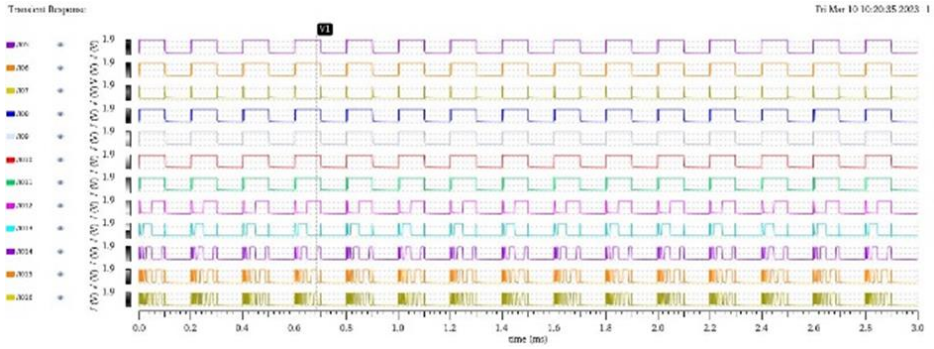

Figure 4: Output response of two-step 16bit flash analog-to-digital converter

Figure 4 represents the output response of a 16-bit flash ADC, whereas Figure 5 depicts the FFT spectrum produced from simulation for a 160K-MHz input signal sampled at 320 KS/s. The simulation results show that the signal-to-noise distortion ratio (SNDR) and spurious free dynamic range (SFDR) are 38.5 and 49.2 dB, respectively.

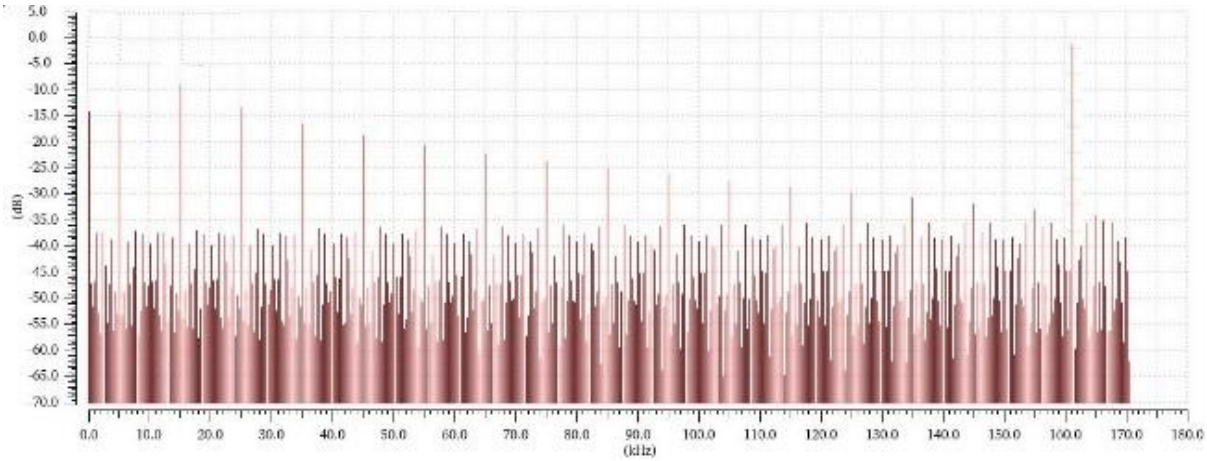

Figure 5: Output response of two-step 16bit flash analog-to-digital converter

In the process of converting the Discrete Time OFDM Signal from Serial to Parallel (S/P Conversion), carriers were eliminated from the OFDM signals, achieved through a serial to parallel conversion. The resulting signals are displayed in **Figure.6**. On the transmitter side, a guard interval was added to each symbol to mitigate Inter-Symbol Interference (ISI). In a subsequent step, the guard periods were removed from the symbols. Furthermore, the parallel discrete-time domain signals underwent conversion to the discrete frequency domain through the application of the FFT operation.

Shifting to the receiver's final stage, its role is to retrieve the original binary data. Initially, a de-mapping operation was conducted on the complex frequency domain symbol corresponding to each sub-carrier, as illustrated in **Figure.7**. Subsequently, these parallel data underwent processing through a parallel-to-serial converter, culminating in the recovery of the original binary data stream, demonstrated in **Figure.8**.

The Compressive Sensing algorithm, demonstrated through the Basis Pursuit algorithm simulation, showcases how it can reconstruct a sparse signal from a reduced number of measurements. In the context, of sparse channel recovery, the L1-norm refers to the sum of the absolute values of the elements of a vector. It is used as a measure of sparsity or "compressibility." MATLAB simulations demonstrate successful sparse channel recovery and accurate estimation by minimizing the L1-norm, promoting sparsity in the estimated solution. In other words, the L1-norm of a vector x is calculated as the sum of the absolute values of its individual elements:

$$\left|\left|x\right|\right|_1 = |x_1| + |x_2| + \ldots + |x_n| \qquad (4)$$

This (Compressive Sensing algorithm) approach enables efficient signal reconstruction, even when the original signal is heavily under-sampled, as illustrated in **Figure 6.**

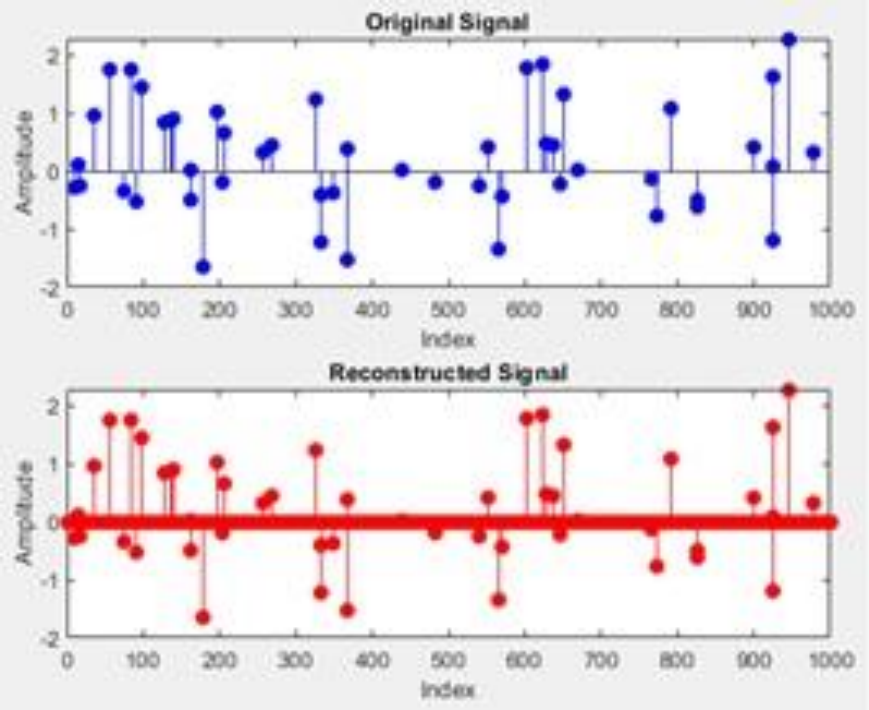

Figure 6: Original and received signal using compressive sensing algorithm for N, M and K

The simulation evaluates the performance of a BPSK communication system with equalization techniques to mitigate intersymbol interference caused by a multipath channel. The techniques used are Zero Forcing (ZF) and Minimum Mean Square Error (MMSE) equalizers. The simulation compares the bit error rates under different Eb/N0 conditions to assess the effectiveness of the techniques.

The Analog-to-Digital Converter (ADC) is a crucial component in the channel estimation process of an OFDM receiver with ultra-low-resolution quantization. Low-resolution ADCs eliminate amplitude information [8], making traditional methods ineffective. To address this, a high-resolution ADC is introduced for signal power measurement, Automatic Gain Control (AGC), and noise power estimation. The ADC helps in measuring received

signal power, recovering average channel gain, estimating noise power, and aiding in automatic gain control. The analog baseband signal is split into two streams, processed by an ultra-low-resolution ADC and a high-resolution ADC at a lower sampling rate. The AGC module adjusts signal amplitude, and channel estimation is done using the GTurbo-LMMSE algorithm. The final estimated channel response is used for data detection in the receiver as shown in Figure 7.

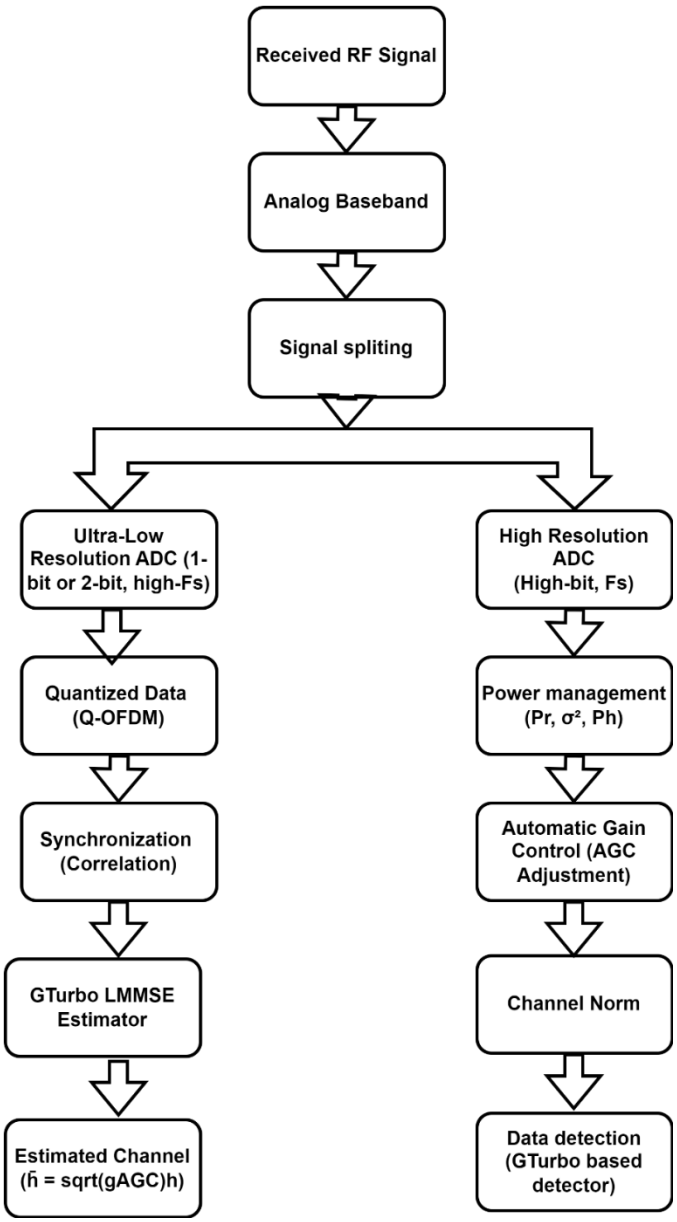

Figure 7: Block diagram of Channel Estimation flow with high bit resolution ADC on OFDM

The quantized received pilot signal in the time domain is given by

$$qp = Q_c(\sqrt{gAGC}\ (F^H diag(p)h + n))$$

Where:

Qp= Quantized received pilot signal

Qc(.)=Quantization function

gAGC=Automatic Gain Control factor

F= DFT matrix

P=Pilot sequence in frequency domain

h= Channel frequency response

n= AWGN noise

Let it be defined here x=diag(p)h, $z=F^H x$,

Where

x=Noiseless received signal in frequency domain

z= Noiseless received signal in time domain

The algorithm iteratively estimates 'h' using Module 'A'(Nonlinear processing) and Module 'B'(LMMSE) based refinement).

GTurbo-LMMSE Algorithm:

Initialization:

- Initialize prior estimate

$$z_A^{pri}(1) = 0,\ v_A^{pri}(1) = 1 - gAGC^{\hat{\sigma}^2}$$

- Initialize other variables

$$x_B^{pri} = 0,\ x_B^{pri} = 0$$

Iterative Process:

For t=1, 2,……T_{max}:

Module-A: Coarse Estimation from Quantized Observations

- **Compute posterior mean and variance for each j-th element**

$$z_{j,A}^{post} = E[z_j|q_{j,p}]$$

$$v_{j,A}^{post} = Var[z_j|q_{j,p}]$$

Using Gaussian approximations (Bussgang Theorem), these are computed as:

$$E[z_j|q_j] = z_A^{pri} + v_A^{pri}\frac{\emptyset(\beta_1) - \emptyset(\beta_2)}{\varphi((\beta_1) - \varphi(\beta_2))}$$

$$Var[z_j|q_{j,p}] = v_A^{pri} - \frac{{v_A^{pri}}^2}{2(v_A^{pri} + \sigma^2}$$

Where (β_1), β_2 are related to the quantization levels.

- **Compute extrinsic information from Module-A:**

$$v_A^{pri} = \frac{\mathbf{1}}{\boldsymbol{N}}\sum_{\boldsymbol{j=1}}^{\boldsymbol{N}} v_{j,A}^{post}$$

$$v_B^{pri} = v_A^{ext} = (\frac{1}{v_A^{post}} - \frac{1}{v_A^{pri}})^1$$

$$x_A^{ext} = v_A^{ext}(\frac{Fz_A^{post}}{v_A^{post}} - \frac{Fz_A^{pri}}{v_A^{pri}})$$

$$x_A^{pri} = x_A^{ext}$$

Module B: LMMSE Channel Estimation

- LMMSE Estimation of h:

$$\hat{\mathrm{h}}\mathrm{d} = \mathrm{W}_{\mathrm{LMMSE}}\mathrm{diag}^{-1}(\mathrm{pd})\mathrm{x}_{\mathrm{B}}^{\mathrm{pri}}$$

Where W_{LMMSE} is precomputed as $W_{LMMSE} = R_{hh_d}(R_{hdhd} + \gamma^2 I)^{-1}$

Here, R_{hh_d} and R_{hdhd} are correlation matrices.

- Compute extrinsic information from Module-B:

$$x_B^{post} = diag(p_d)\hat{\mathrm{h}}\mathrm{d}$$

$$x_A^{pri} = x_B^{ext} = c(x_B^{post} - \alpha x_B^{pri})$$

$x_A^{pri} = x_B^{ext} = \frac{1}{N_d}\sum_{j=1}^{N_d} |x_B^{ext} - x_B^{post}|^2$

Where α and c are chosen to minimize error and ensure stability

$$\alpha = \frac{1}{N_d} tr(\mathrm{W}_{\mathrm{LMMSE}}\mathrm{diag}^{-1}(\mathrm{pd}))$$

$$c = \frac{x_B^{pri,H}(x_B^{post} - \alpha x_B^{pri})}{|x_B^{ext} - x_B^{post}|^2}$$

Channel Gain Normalization using ADC:

If one 1-bit is used, normalize the estimated channel: $\hat{\mathrm{h}}\mathrm{d} = \sqrt{P_h}\frac{\hat{\mathrm{h}}\mathrm{d}}{||\hat{\mathrm{h}}\mathrm{d}||}$

Where P_h is estimated from received signal power:

$$P_h = (P_r - \sigma^2)\frac{N}{N_d}$$

Then the estimated channel: $h_d = \sqrt{gAGC}\hat{\mathrm{h}}\mathrm{d}$

Use in data detection: h_d is passed to GTurbo-based detector for OFDM demodulation. This algorithm is robust to quantization effects and enables reliable OFDM channel estimation even with-low and high-resolution ADCs.

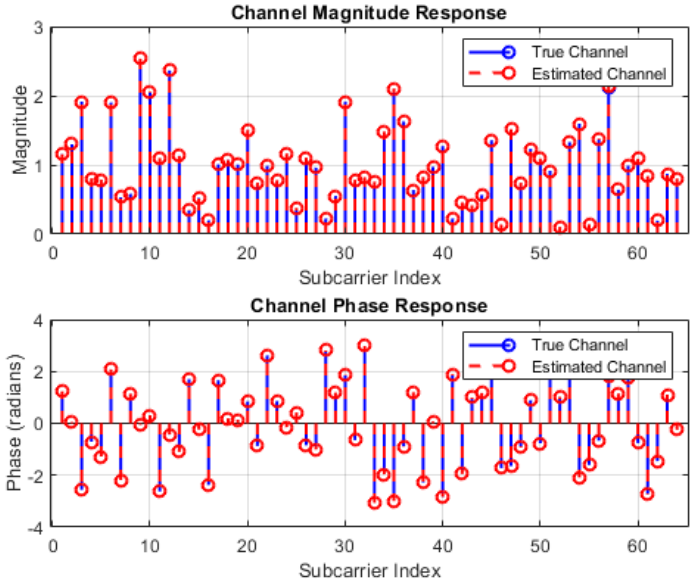

Figure 8(a): Channel Magnitude-Phase response at SNR of 10.9dB

Mean square error (MSE) is determines the accuracy of estimated channel, the MSE is as follows with

$MSE = \frac{1}{N}\sum_{i=1}^{N}(y_i - \hat{y}_i)^2$, where N-number of symbols

Yi-actual value, Yi^ -Estimated value, and the estimated MSE is 2.037.

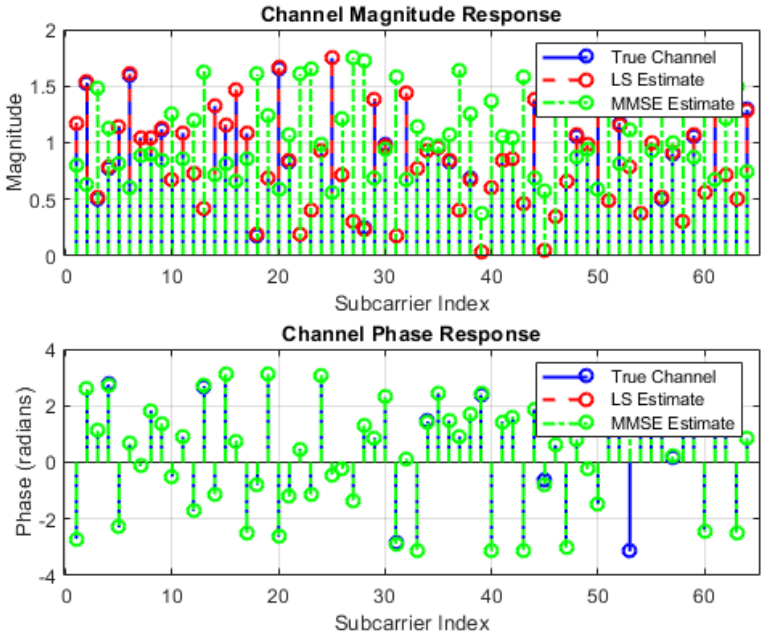

Figure 8(b): Channel Magnitude-Phase response at SNR of 10.9dB for MSE, LSMSE, MMSE

Mean Squared Error (MSE): 2.037

LS Estimation MSE: 4.0363e-05

MMSE Estimation MSE: 0.62302

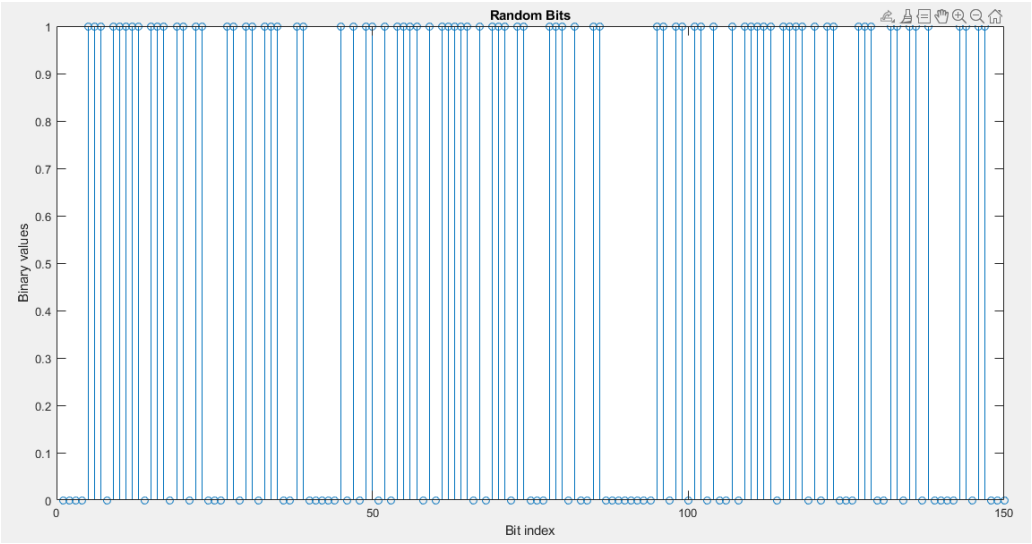

Figure 9: Channel Input stream of BPSK

The simulation evaluates the performance of a BPSK communication system with equalization techniques to mitigate intersymbol interference caused by a multipath channel. The techniques used are Zero Forcing (ZF) and Minimum Mean Square Error (MMSE) equalizers. The simulation compares the bit error rates under different Eb/N0 conditions to assess the effectiveness of the techniques.

The input pilot random data is applied to the OFDM transmitter, which then transmits this generated data, as depicted in Figure 9. At the receiver section, the received data undergoes fading, and the resulting data is shown in Figure 8.

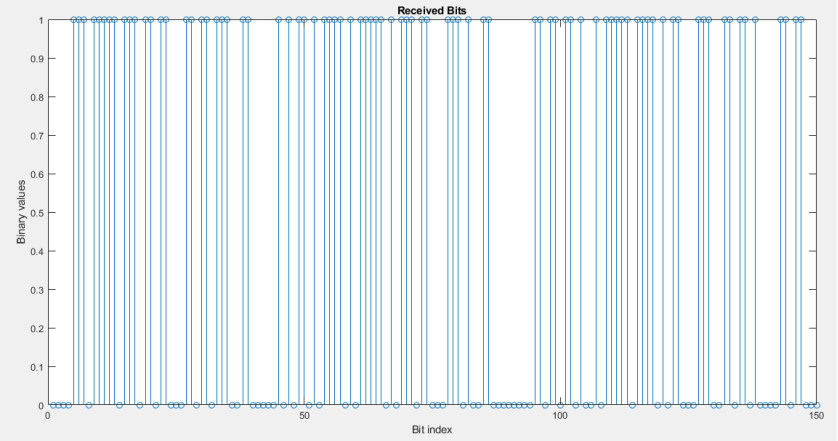

Figure 10: BPSK modulation with Rayleigh noise and MMSE equalizer

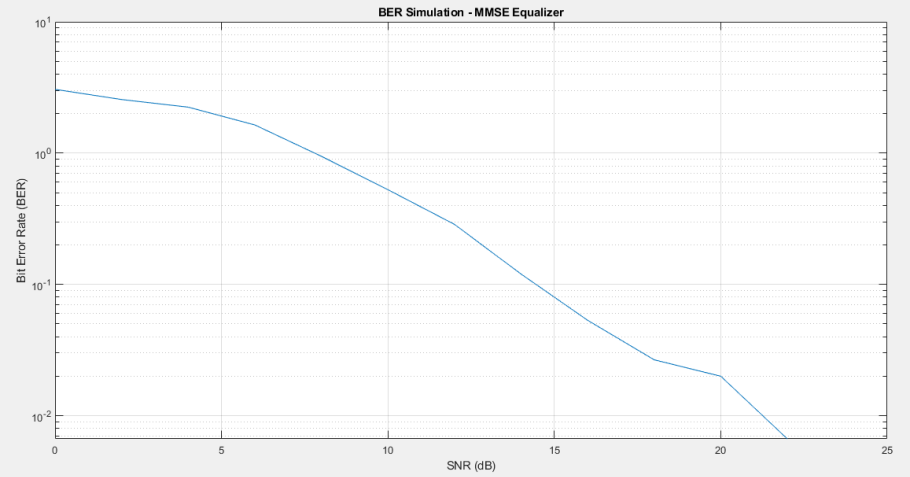

Figure 11: BPSK modulation with Rayleigh noise and MMSE equalizer

Figure 11 Illustrates the BER performance of a BPSK modulation system with an MMSE equalizer in the presence of Rayleigh noise. The graph shows the BER values for different SNR levels, with the SNR represented in dB on the horizontal axis. As the SNR increases, the BER performance of the BPSK system improves, approaching the theoretical BER curve for BPSK in an AWGN channel.

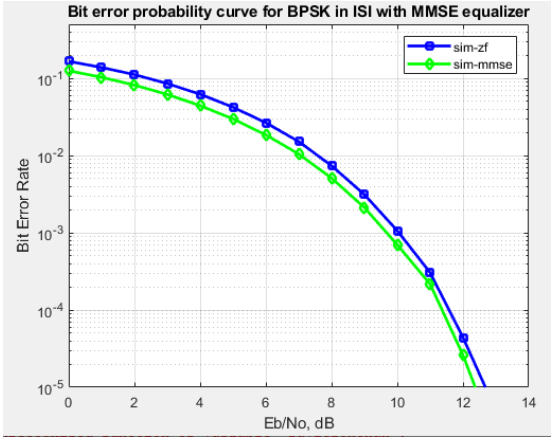

Figure 12: Bit error probability curve for BPSK modulation ISI with MMSE equalizer

The simulation evaluates the performance of BPSK modulation in a Rayleigh fading channel by determining the Bit Error Rate (BER) for various Eb/N0 values. The procedure entails synthesizing random bits, using BPSK modulation, adding white Gaussian noise, and establishing a Rayleigh fading channel. Channel division equalization and hard decision decoding are applied to the received signal. The BER is calculated by counting the number of errors between transmitted and decoded bits. The simulation compares the simulated BER curve to theoretical curves for AWGN and Rayleigh fading channels to assess the efficacy of BPSK modulation in the Rayleigh fading channel, as seen in Figures 12 and 13.

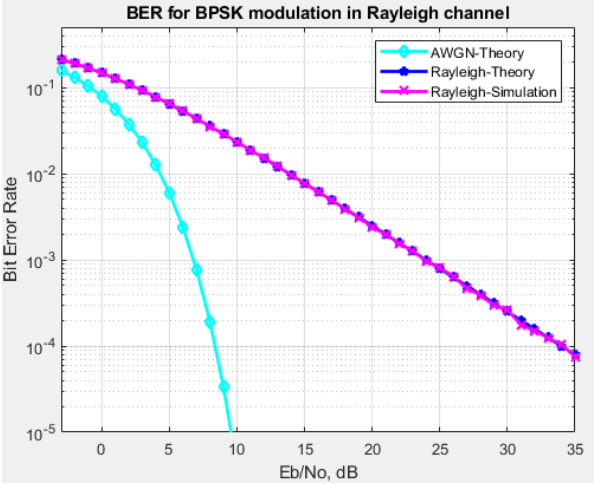

Figure 13: BER for BPSK modulation Rayleigh channel

Table 2: Comparison of this work with literature parameters

Ref's.	[5]	[6]	[7]	[15]	[16]	**work**
Technology	250nm	180nm	55nm	40nm	90nm	180nm
Resolution	18	18	16	14	13	16
Type of architecture	Pipe SAR	Pipe SAR	SAR	SAR	SAR	FLASH
Vdd (V)	2.5	1.8	1.2	1.2	1.2	1.8
Power [mw]	1.5	30.5	6.95	54.5	4.2	0.820
SFDR (dB)	82	100	100	99	85	105.26
SNDR (dB)	80	99	81	75	71	95.26
Sampling (s/s)	12.5M	5M	1M	35M	50M	1G
INL (LSB)	-2.5/2.5	-2/2	-0.8/0.8	-0.9/0.7	-1.3/2	0.45
DNL (LSB)	1	0.8	0.8	0.7	0.7	0.61
FoM	157.7	177.7	159.6	159.5	166.8	173.7fJ/Con-step
Area [m^2]	4.5	5.74	4.1	0.24	0.097	16.71263p
Delay						16.2154 µsec
Noise						2.2384pV**2/Hz

V. CONCLUSION

The proposed methodology combines a 16-bit two-step flash ADC with compressive sensing technique for accurate high-resolution channel estimation in OFDM systems. MATLAB simulations demonstrate successful sparse channel recovery and accurate estimation using L1-norm minimization. The high-speed flash ADC captures fine details, enhancing accuracy and implemented design and layout for practical integration. Overall, the contributions of this paper offer promising advancements in OFDM channel estimation, with the efficient ADC design and integration of compressive sensing showing potential for enhanced accuracy and resource utilization in future OFDM systems. Further research is needed for different channel conditions and enhancements in

compressive sensing techniques and algorithm efficiency for improvement in the future potential areas. Despite limitations, the proposed method offers promise for practical integration in wireless communication applications.

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