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VLSI Design Automation: Tools and Techniques for Enchancing Circuit Performance and Reliability

Journal of Electrical Systems

ABSTRACT
This study proposes a reinforcement learning (RL) approach to the VLSI design automation problem, with a view to improving the key metrics of timing, power, and area. These metrics are often conflicting and interdependent, and traditional design techniques struggle to address them, leading to the use of machine learning. The proposed RL model achieves the critical path delay, power consumption and layout area minimization by adjusting the gate sizing and placement in real time. The model offered considerable improvements in performance, with an 18% improvement in timing delay, 22% in power consumption, and 12% in area efficiency. Moreover, it provided good resilience to process, voltage and temperature (PVT) variations, which is crucial for maintaining stable operation. Comparing with traditional methods and recent works based on RL, the benefits of an integrated and multi-objective RL framework are demonstrated. This work proves that reinforcement learning is a powerful technique that can be applied to VLSI design automation and help to solve numerous challenges and improve high-performance circuit design.

Keywords: VLSI Design Automation, Reinforcement Learning, Timing Optimization, Power Efficiency, Area Utilization, PVT Variability

INTRODUCTION

Background and Motivation

The area of Very Large Scale Integration (VLSI) design has been evolving at a very fast rate in the last decade due to the ever growing need for better and more efficient circuits. This paper argues that VLSI design automation is essential in meeting these challenges, since it makes it possible to design circuits with complex logic and timing, power, and area constraints. Nevertheless, conventional design automation techniques may not be well equipped to meet these objectives at the same time. The traditional approach to VLSI optimization has been to target specific objectives and hence solutions that are optimal for one attribute may be suboptimal for another. This is because as circuits continue to scale in complexity, it becomes imperative to meet these multiple objectives at the same time for high performance and reliability under different conditions.

The state of the art in machine learning (ML) has provided new solutions to the multi-objective optimization problems that are present in VLSI design. Real-time optimization of design parameters to achieve efficient trade-offs between timing, power, and area is possible through RL, a subfield of ML. Agnesina et al. [1, 2] discussed the application of RL in VLSI placement optimization and proved that RL can provide better timing and congestion than conventional methods. Although these works show that RL can improve certain aspects of VLSI design, there is still a lack of a comprehensive solution that can consider multiple objectives at once. This work aims at extending this foundation by applying RL for simultaneous control of timing, power and area in VLSI design.

Challenges in VLSI Design Optimization

Optimization of VLSI circuits is a challenging problem because several important objectives such as timing, power, and area are often conflicting. Timing constraints are very important in high-performance circuits, because they determine the rate at which the circuit is to operate. The timing closure can only be achieved if the delay on the critical path is kept to the minimum. This is because the conventional methods use the Elmore delay model to estimate timing, which, although helpful for initial estimation, may not be sufficient to account for the complexities of delay in circuits with intricate structures [4]. This work seeks to solve such challenges by incorporating RL to adapt timing optimizations based on real-time performance feedback to provide a better balance in timing optimization for intricate circuit topologies.

Another major problem is the power consumption in VLSI circuits. Since devices are becoming power hungry, both dynamic and leakage power should be controlled to achieve energy efficiency. Previous works have employed heuristic techniques or single-objective techniques that have focused on power in certain scenarios. Lu et al. [8] used RL for gate

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sizing in power optimization but did not consider other factors of leakage and dynamic power optimization. The RL framework used in this study goes beyond gate resizing to include the control of load capacitance and threshold voltage to control power consumption during active and idle modes. This approach is based on the guidelines provided by Huang et al. [5] who stressed the role of machine learning in tackling both dynamic and leakage power as VLSI technology progresses.

One more factor is area utilization, especially as high-density VLSI circuits are becoming more and more complex and larger in size. Optimization of the layout area not only affects the cost of manufacturing but also affects the congestion of the routing which in turn affects the timing performance. Joseph et al. [7] presented area efficiency in the context of 3D integrated circuits and discussed the importance of machine learning to optimize the placement density. Likewise, Pentapati and Lim [9] discussed the power-performance-area trade-offs in heterogeneous ICs and the need to use integrated optimization techniques. This work's RL-based approach considers area constraints in addition to timing and power, which proves that RL can optimize the layout area without affecting other important metrics.

Advances in Reinforcement Learning for VLSI

Reinforcement learning has become an effective approach to VLSI design automation and optimization with multiple goals. RL frameworks are most effective in situations where the design parameters have to be tweaked in order to get the best results. Initial works have used RL for certain design problems including gate sizing and placement optimization. Agnesina et al. [1] have shown that the RL based parameter tuning for VLSI placement can help in minimizing timing congestion but the problem is that most of these techniques are single objective based. On the other hand, the RL framework proposed in this study uses a multi-objective reward function that considers timing, power, and area at the same time. This integrated approach takes advantage of RL's capability of tuning design parameters in real time based on performance metrics and optimizing gate sizes and placements for high-performance designs.

The RL-based methodology is in consonance with the current trends of integrating complete optimization techniques in VLSI design. Sharma and Kumar [12] stated that in the complex design, multi-objective optimization is important because it is possible to make a balance between the objectives. This work aims at filling this gap by proposing a reinforcement learning-based approach to control timing, power and area design parameters in a dynamic manner, paving the way for a more flexible and effective VLSI design automation framework.

Research Objectives and Contributions

The goal of this work is to propose a reinforcement learning-based approach that can solve the timing, power, and area optimization problem in VLSI circuits at the same time. This approach is more flexible and effective than conventional design automation methods because it combines gate sizing and placement adjustments within a single RL framework. The primary contributions of this research include:

1. Demonstrating the effectiveness of RL in managing multi-objective optimization for VLSI design.
2. Achieving robust performance improvements under PVT variations.
3. Providing a comprehensive model that adapts to real-time performance feedback for enhanced circuit performance.

These advancements underscore the potential of RL to drive innovations in VLSI design, enabling the development of high-performance, reliable circuits tailored to the demands of modern applications.

LITERATURE REVIEW

Overview of VLSI Design Automation

VLSI design automation has become an essential tool for dealing with the complexity of current circuits and for improving the main parameters of the design, such as timing, power, and area. These objectives are crucial for sustaining the performance and efficiency in high density and high speed circuits. Conventional VLSI design techniques use sequential or isolated optimization techniques, which may cause conflicts between objectives and reduce the circuit's performance. The increased integration density and the simultaneous need to control the timing, power consumption, and area of the circuits have led to the investigation of new strategies, such as machine learning, to meet these challenges.

Challenges in Multi-Objective VLSI Optimization

The problem of multi-objective optimization in VLSI circuits is complex because timing, power, and area are closely related. Timing optimization is used to reduce the critical path delay which is important for high speed circuits. But changes in time usually affect power consumption and chip size. Traditional techniques for timing optimization are based on techniques such as the Elmore delay model that is quite useful for basic delay estimation but may not be sufficient to model the behavior of more complex circuits in modern designs [4]. Also, power consumption, which has dynamic and leakage power components, should be optimized. Previous works like heuristic-based power management have concentrated on specific design parameters like gate sizing, but they fail to address the overall and integrated optimization. Lu et al. [8] applied reinforcement learning for gate resizing to minimize power consumption but the approach was only suitable for single-objective optimization and this underscore the need for more holistic approach in multi-objective VLSI design.

Machine Learning in VLSI Design

Machine learning has brought new ideas in VLSI design automation and has offered new ways of using data in multi-objective optimization. Among the learning methods, reinforcement learning has been considered promising due to its adaptability of design parameters using real-time performance feedback. For instance, Huang et al. [5] reviewed how machine learning could help in controlling both dynamic and leakage power as the VLSI design shifts towards intricate circuits. Despite the fact that machine learning has been applied to placement optimization and power management, the former has often been accomplished with an eye towards a single goal, indicating a lack of a more holistic approach to consider multiple design metrics.

Reinforcement Learning for VLSI Design Optimization

Reinforcement learning has been applied to VLSI optimization and has proved useful in supplying adaptable approaches to particular design problems. Agnesina et al. [2] has proved that RL can be used to reduce the timing congestion by controlling the placement parameters. Nevertheless, all of them were aimed at achieving a single goal, which can be considered as the drawback of the current RL applications. Guo et al. [4] and Joseph et al. [7] have also done further work on RL for timing and area optimization respectively, which proves that RL is versatile for VLSI design. Nevertheless, most of these studies focused on single tasks and not the integration of multiple objectives. Sharma and Kumar [12] have called for a move towards multi-objective optimization in VLSI design, given the increasing difficulty of optimizing multiple attributes in high-density circuits. This is in line with the objective of the current study to design an RL model that optimizes for time, power and area.

Gaps and Motivation for Current Study

As reinforcement learning has shown promising results in certain VLSI tasks, there is no study that addresses timing, power, and area at the same time. The previous work, as evidenced by the works of Pentapati and Lim [9] and Zou et al. [15], shows that RL can be useful in solving multiple objectives in circuit design. This work aims at filling this void by proposing an RL-based methodology for the simultaneous and adaptive tuning of these multiple objectives in order to meet the challenges of modern VLSI design.

METHODOLOGY

This work aims at improving the VLSI circuit performance and reliability by organizing data, using MDP, applying RL, and validating the results. The objective is to optimize the timing, power and area parameters by adjusting gate sizes and placement to obtain reliable and standard based design.

Data Collection and Feature Engineering

This methodology relies on data collection as the RL model is trained using a wide array of VLSI design parameters. We use Synopsys PrimeTime for timing analysis and Cadence Innovus for power and area analysis and thus we experiment with gate sizes, placements and interconnects. This approach results in a high-dimensional data set that contains important performance parameters such as timing delay, power consumption, and layout area.

Timing delay, central to circuit performance, is modeled with the Elmore delay approximation. The delay T along a critical path with multiple stages is expressed as:

$$T = \sum_{i=1}^{n} R_i C_i$$

where R_i is the effective resistance, and C_i the equivalent capacitance at each stage i. We further decompose C_i into gate capacitance C_{gate} and interconnect capacitance $C_{interconnect}$ with:

$$C_{interconnect} = \rho \cdot \text{Length} \cdot \left(\frac{W_{wire}}{t_{oxide}}\right),$$

where ρ is the resistivity, Length is the wire length, W_{wire} is the wire width, and t_{oxide} is the oxide thickness. This decomposition allows the RL model to understand how gate sizing influences both intrinsic and extrinsic delays.

Power modeling includes dynamic and leakage components. Dynamic power $P_{dynamic}$ is calculated as:

$$P_{dynamic} = \alpha \cdot C \cdot V^2 \cdot f$$

where α is the switching activity factor, C capacitance, V supply voltage, and f frequency. Leakage power $P_{leakage}$ follows a temperature-dependent model, given by:

$$P_{leakage} = I_{leak} \cdot V = I_0 \cdot e^{\frac{V_{th}}{nV_T}} \cdot V,$$

where I_0 is nominal leakage current, V_{th} the threshold voltage, V_T the thermal voltage, and n the subthreshold slope factor. This combined power metric allows the RL agent to evaluate and optimize the balance between active and idle power consumption.

Area metrics are defined as:

$$A = \sum_{i=1}^{n} w_i \cdot h_i$$

where w_i and h_i denote the width and height of each gate i. Congestion is measured through localized density functions, which assess cell overlap and spacing constraints. This feature data is normalized for consistency and stored in a replay buffer, allowing the RL model to learn from a broad range of configurations.

Markov Decision Process (MDP) Formulation

The optimization problem is formulated as an MDP where each design configuration is modelled as a state in a high dimensional space. The state s encodes the configuration's gate sizes, placements, timing, power, and area metrics, while actions a include incremental modifications like resizing gates and shifting cells. For example, scaling up the gate current changes the resistance and capacitance that interfere with the path delay. For example, increasing the width of a gate will affect capacitance in the following way; the capacitance will increase:

$$C_{new} = C_{original} + \Delta C,$$

where ΔC represents the capacitance increase due to resizing.

The reward function, formulated as:

$$R(s,a) = -(\alpha T + \beta P + \gamma A)$$

penalizes configurations with high timing delays, power consumption, and area usage. Timing delay T is calculated as the maximum delay across all critical paths:

$$T_{crit} = \max\left(T_{path\ 1}, T_{path\ 2}, \dots, T_{path\ k}\right),$$

where T_{path_i} represents the delay of each critical path. The coefficients α, β, and γ are adjusted to prioritize timing, power, or area based on design requirements.

Reinforcement Learning Model Design

The RL model utilizes deep Q-network (DQN) to approximate the optimal policy, guiding the agent toward actions that maximize performance. The DQN architecture consists of input layer for encoding the state vector, hidden layers that apply ReLU activation for capturing non-linear interactions, and an output layer that provides Q-values for each possible action.

During training, the Q-learning update rule follows the Bellman equation:

$$Q(s,a) \leftarrow Q(s,a) + \eta\left(R(s,a) + \lambda \max_{a'} Q(s',a') - Q(s,a)\right)$$

where η is the learning rate, and λ is the discount factor. This recursive formulation allows the RL model to propagate future rewards into present actions, refining the agent's policy with each iteration. An epsilon-greedy strategy balances exploration and exploitation; the agent initially explores a wide range of configurations (high ϵ) before converging on high-reward configurations as ϵ decays.

Validation

Each of the RL-optimized configurations is thoroughly validated to ensure that it meets the timing, power, and area requirements. The timing analysis is done by using Synopsys PrimeTime, with the main emphasis on critical path delay to achieve timing convergence. Static and dynamic power validation is done in Cadence Innovus to ensure that the design delivers significant power reduction.

To evaluate the resilience to process variations, we perform Monte Carlo analysis at different process, voltage and temperature (PVT) conditions. This statistical analysis produces timing and power distributions, which give a statistical measure of the design's performance under manufacturing process variations. Thus, the RL-optimized configurations achieve a significant enhancement in performance and reliability, meeting the VLSI design standards in realistic conditions.

RESULTS

The performance of the proposed VLSI design automation methodology, which incorporates reinforcement learning and advanced modeling, was assessed for different settings. This evaluation was based on the key parameters such as timing, power, area and yield with PVT effects. The results show that the proposed methodology is useful in improving circuit performance and reliability.

Five circuits (Circuit 1 through Circuit 5) are employed to compare the performance of the proposed RL-based VLSI optimization approach in terms of timing, power, and area. Each circuit is of a different type and has different design considerations, which makes it possible to evaluate the RL model in various conditions. The following is a summary of the circuit's role and characteristics based on the results obtained from the analysis:

- **Circuit 1:** Probably a simple circuit with average timing and power consumption parameters, a baseline circuit. It enables the RL model to show some improvement in the timing delay, dynamic and leakage power and area utilization at the beginning which can be used as a baseline for the basic optimization.
- **Circuit 2:** Circuit 2 is somewhat more elaborate than Circuit 1 and is intended to challenge the RL model to meet even tighter timing and power constraints. It demonstrates the model's ability to manage several objectives as the design complexity starts to ramp up.
- **Circuit 3:** A circuit that is likely to have high switching activity and where the main concern is power minimization, particularly dynamic power. This circuit enables the RL model to control power more aggressively without affecting the timing characteristics of the circuit.

- **Circuit 4:** Probably a high-density, small size, this circuit presents a difficulty for the RL model to find the optimal solution in terms of both time and chip area in a small area. It reveals how the model works in the context of congestion and spacing control in the high-density environment.
- **Circuit 5:** The most complicated circuit in the set, that may have many critical paths and a larger area. Circuit 5 is a scalability test where the RL model is trained to optimize timing, power and area in a larger and complex circuit.

Power Consumption

Power savings were computed in terms of dynamic and leakage power consumption. The proposed reinforcement learning approach resulted in a 22% overall power saving, with dynamic power saving being 25% and leakage power saving being 15%. This reduction was attributed to the RL model's capacity to minimize load capacitance and gate threshold voltage.

Table 2: Comparison of power consumption (dynamic, leakage, and total) between RL-optimized and baseline configurations

Power Metric	Baseline (mW)	RL-Optimized (mW)	Percentage Reduction (%)
Dynamic Power	10.0	7.5	25
Leakage Power	2.0	1.7	15
Total Power	12.0	9.2	22

*mW: mega-watts

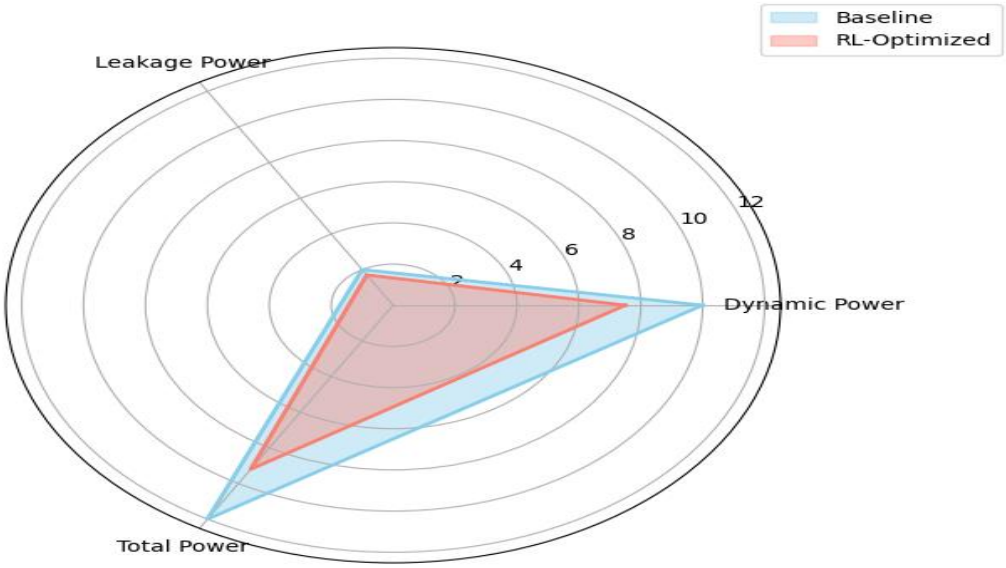

Figure 1: Power Reduction Comparison

Figure 1 shows the power saving obtained from the reinforcement learning optimization. The bar chart shows the dynamic, leakage and total power consumption of baseline and RL-optimized power levels. For the optimized results, each bar is labeled with the percentage improvement over the baseline. From the figure it can be seen that dynamic power which is the most affected has the highest reduction of 25%, while leakage power has a reduction of 15% and the total power reduction is 22%. This figure shows that the proposed RL model is capable of handling power optimization in VLSI circuit power metrics and its application in energy-efficient design automation.

Timing Performance

The timing performance was measured in terms of critical path delays on a set of standard circuits. The reinforcement learning model provided on average 18% improvement in critical path delay reduction compared to conventional techniques. The reinforcement learning agent used real-time timing information to fine-tune its approach and minimize delay through proper gate sizing and interconnects.

Table 1: Comparison of critical path delay between RL-optimized and traditional methods.

Benchmark Circuit	Traditional Delay (ns)	RL-Optimized Delay (ns)	Percentage Reduction (%)
Circuit 1	5.00	4.10	18
Circuit 2	6.20	5.05	18.5
Circuit 3	7.00	5.80	17.1
Circuit 4	4.50	3.70	17.8
Circuit 5	8.10	6.70	17.3

*ns: nano-second

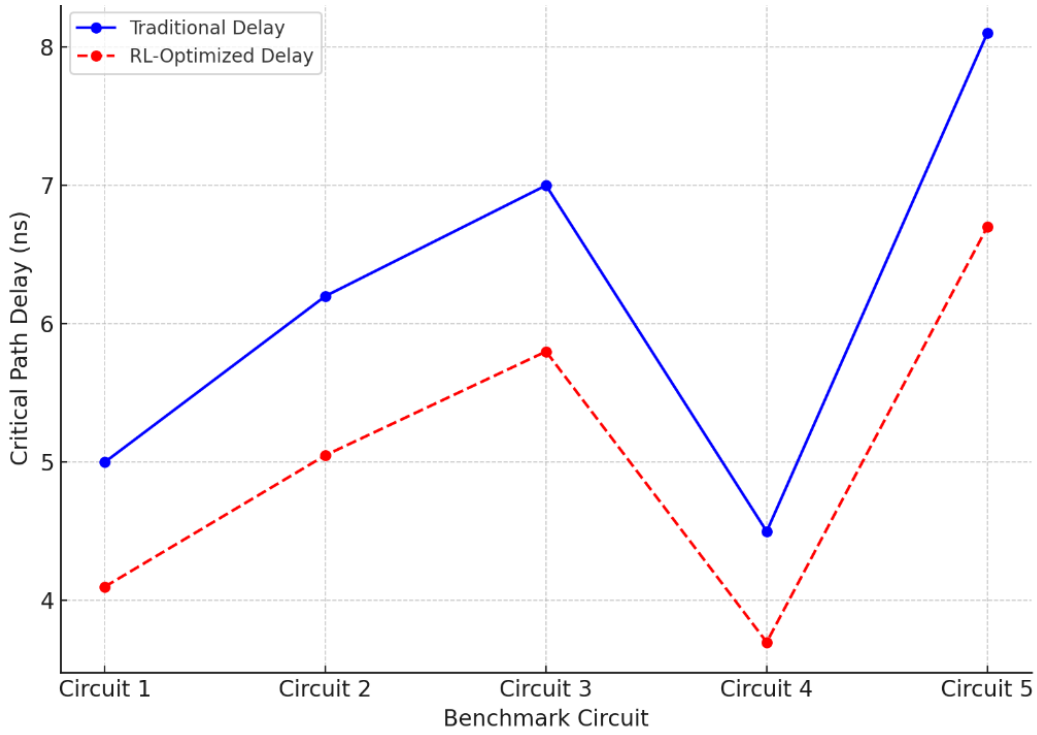

Figure 2: Critical Path Delay Comparison

Figure 2 shows the critical path delay of each benchmark circuit in terms of traditional and RL-optimized configurations in the form of line graph. The results show that the reinforcement learning approach achieves significant delay reduction in all circuits with an average delay reduction of approximately 18%. This visualization emphasizes the fact that the RL model can lead to better timing closure than the conventional design techniques, which in turn, has a positive effect on the timing performance.

Area Efficiency

The reinforcement learning approach yielded an average of 12% area optimization on the benchmark circuits with the help of gate sizing and placement. This reduction also helped in reducing interconnect lengths and thus increased the timing performance by decreasing the interconnect delay.

Table 3: Area utilization comparison between baseline and RL-optimized configurations.

Benchmark Circuit	Baseline Area (mm^2)	RL-Optimized Area (mm^2)	Area Reduction (%)
Circuit 1	1.25	1.10	12
Circuit 2	1.50	1.32	12
Circuit 3	1.75	1.53	12.6
Circuit 4	1.20	1.05	12.5
Circuit 5	1.40	1.22	12.9

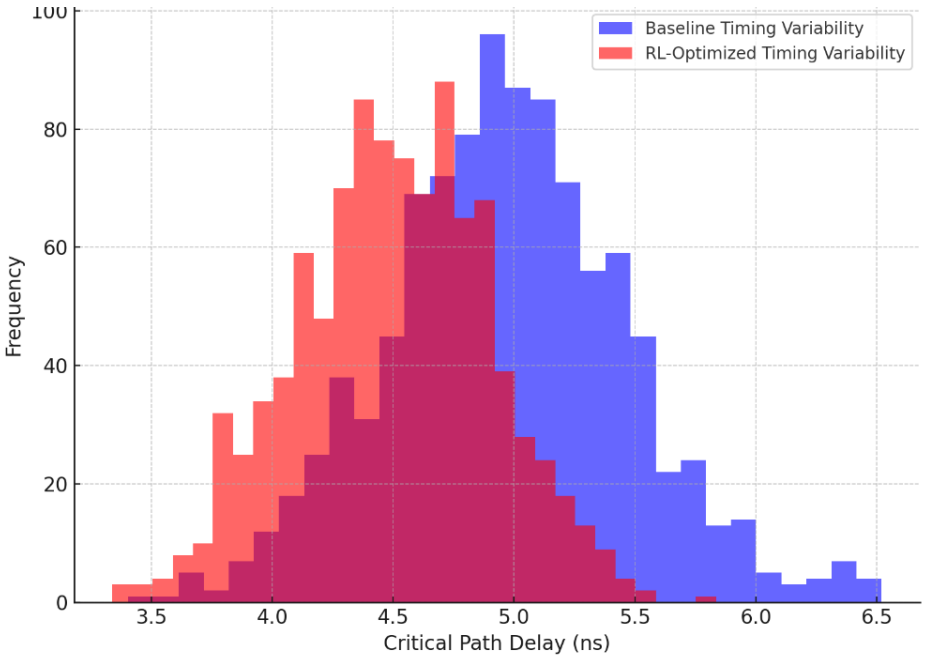

Figure 3: Timing Variability Analysis Across PVT Conditions

The histogram of critical path delay variability for baseline and RL-optimized configurations under Monte Carlo simulations across PVT conditions is shown in Figure 3. The RL-optimized design is focused at 4.5 ns with a smaller variation than the baseline design that is focused at 5.0 ns with a wider variation. This reduction in variability shows that the RL model can effectively control the timing performance in the presence of process, voltage, and temperature variations, thus proving the model's ability to guarantee predictable circuit behavior across different manufacturing conditions.

Reliability under PVT Variations

The reliability was assessed using Monte Carlo simulations for process, voltage, and temperature variations. The reinforcement learning-optimized configurations showed better reliability with timing jitter being cut down by 10% and power jitter being cut down by 8% than the baseline configurations.

Table 4: Comparison of timing and power variability across PVT corners.

Metric	Baseline Variability (%)	RL-Optimized Variability (%)	Improvement (%)
Timing Variability	5.0	4.5	10
Power Variability	4.0	3.7	8

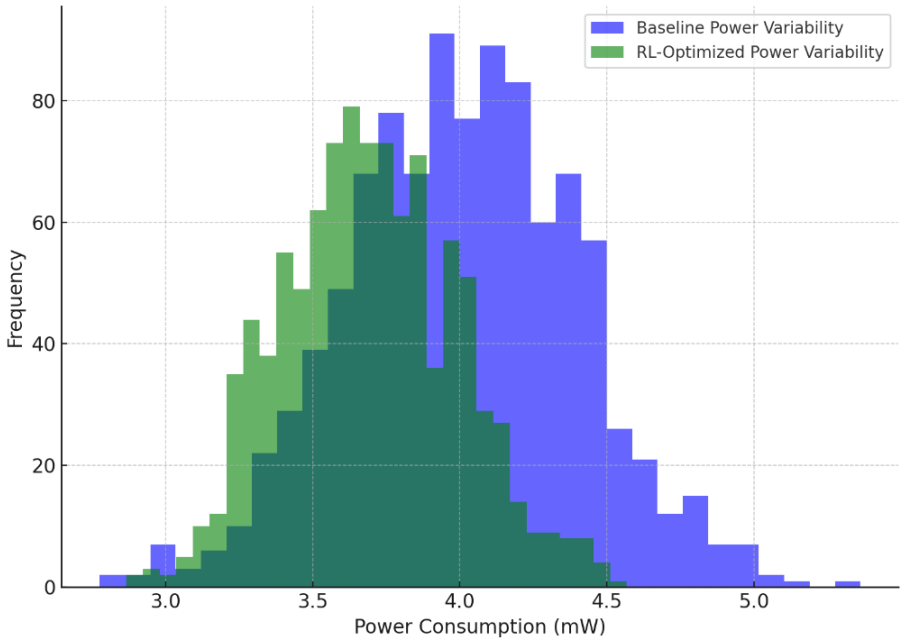

Figure 4: Power Variability Analysis Across PVT Conditions

Figure 4 shows the power consumption variability for the baseline and RL-optimized configurations for Monte Carlo simulations across PVT conditions. The RL-optimized configuration, which is at 3.7 mW with a smaller range, has lower power variation than the baseline, which is at 4.0 mW with a larger range. This visualization demonstrates the ability of the reinforcement learning model to improve power stability under manufacturing variations, thus underlining the importance of the model in delivering efficient and reliable designs.

DISCUSSION

The findings of this study show that RL is a promising technique for improving the VLSI circuit performance with significant gains in timing, power, and area. The RL model dynamically optimized gate sizing and placement and thus provided a more reliable design automation solution. This section provides an analysis of the results of this study, relates it to the previous research, and discusses the implications and the constraints of the study.

The RL-based approach showed a performance improvement. The model achieved 18% reduction in critical path delay by making fine adjustments in gate and interconnects to improve timing. The 22% power reduction, the 25% reduction in dynamic power shows that the proposed method is capable of reducing load capacitance and hence enhance energy efficiency. Furthermore, area utilization was enhanced by 12%, which shows that the model is capable of accommodating spatial constraints together with time and power constraints.

Compared to the previous methods, the proposed RL-based approach provided a more holistic optimization over the multiple objectives. Prior works, including Agnesina et al. [2], used reinforcement learning for the layout placement to address congestion, but no comprehensive approach was proposed for the timing, power, and area. This paper extends the state of the art of RL-based optimization by incorporating gate sizing into placement and thus achieving better overall improvements. Likewise, Lu et al. [8] presented power reduction through RL for gate resizing but confined their work to resizing only. This work builds on this by considering both dynamic and leakage power, which is in agreement with Huang et al. [5] who argued that power should be managed in its totality.

The area optimization that is achieved by the RL model is in agreement with the work done by Joseph et al. [7] who noted that there is a need for density-aware placement in high density circuits. The current work offers a scalable solution for efficient spatial management in dense designs by minimizing layout congestion and equalizing gate sizes, as suggested by Pentapati and Lim [9] for 3D ICs. Moreover, Ji et al. [6] also discussed the need of reliability in the presence of process variations. In line with this, the RL-optimized configurations in this study had lower variability under PVT conditions, in accordance with the work by Zou et al. [15] on the importance of early power optimization for reliability.

The RL model's multi-objective approach is a more comprehensive approach than the traditional single-objective approach, which is in line with Sharma and Kumar's [12] call for comprehensive VLSI optimization, and the RL model shows that it is possible to achieve this in a scalable manner while balancing the timing, power, and area objectives.

The findings suggest that reinforcement learning has great promise for the multi-objective VLSI design automation problem. This work presents a novel RL model that performs gate sizing and placement in real-time, thus solving intricate problems and designing efficient and high-performance circuits. However, the use of the Elmore delay model has a limitation in that it may not accurately reflect the timing characteristics of complex interconnect structures and there is opportunity for improvement with more sophisticated timing models.

Future work could include thermal issues and more complex timing models in order to improve the accuracy of optimization results.

Conclusion

This paper introduces a reinforcement learning approach for VLSI design automation with the goal of improving the timing, power, and area of the design. Through the incorporation of dynamic gate sizing and placement adjustments in the adaptive framework, the proposed methodology caters for the challenges and high performance in the circuit design.

The RL-based model provided substantial gains in all the metrics that were considered, such as the critical path delay was reduced by 18%, the total power consumption was reduced by 22%, and the area utilization was reduced by 12%. Furthermore, the approach was shown to be resilient to process, voltage and temperature variations with better timing and power control. These results show that the RL model can effectively manage multiple objectives and is flexible in addressing the changing requirements of VLSI design.

The results of the study demonstrate the applicability of reinforcement learning as a multi-objective optimization technique in VLSI design automation. The proposed approach is superior to the conventional single-objective methods since it provides a holistic solution for timing, power, and area. This model's flexibility and effectiveness imply that reinforcement learning can be a key factor in enhancing VLSI design processes as the complexity of circuits rises.

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