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An Integrated Multi-Band Low Noise Amplifier with Coverage of 33 GHz in 32 Nm Complementary Metal–Oxide– Semiconductor Silicon Upon Insulator

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Abstract: This work describes a 32-nm CMOS silicon-on-insulator (SOI) multi-band low-noise amplifier (LNA). The three stages of the LNA are centered around the differential cascode amplifier. As the later stages boost the gain, the initial stage is primarily in charge of input matching to guarantee favorable noise characteristics and bandwidth. Additionally, the LNA matches interstage impedance and input/output using baluns. The LNA operates in three bands totaling 17–33 GHz, with the addition of switch capacitances to enable band switching. A gain (S21) of 23.0 dB and a noise figure (NF) of 4.0 dB are achieved by the suggested LNA, according to measurement data

Keywords: Soi; cascode; low-noise amplifier; multi-band; switch capacitance

1. INTRODUCTION

Broadband satellite communication, 5G communication, and millimeter-wave (MMW) car radars are examples of high-frequency broadband applications that are being driven by the need for higher data rates, which is being driven by the rapid advancement of wireless transmission [1]. Transceiver designs have never stopped evolving as the front ends of wireless communication systems. Research and production costs can be greatly decreased by using broad-band transceivers that are appropriate for a variety of applications and providers. This has led to the widespread use of the wideband technique [2]. In order to determine the receiver's bandwidth, linearity, sensitivity, and noise characteristics, low-noise amplifiers (LNA) are necessary. The intended use of an LNA in a multi-band receiver is depicted in Figure 1.

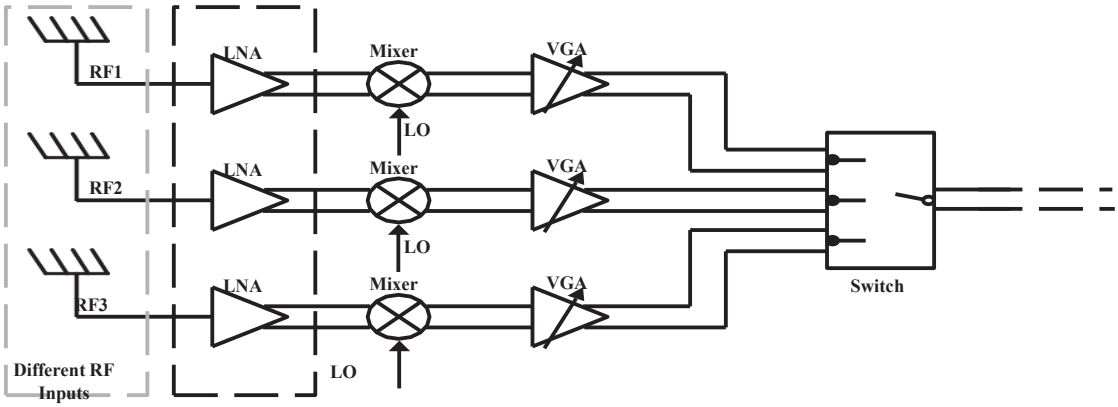

Figure 1. LNA in a system for receiving.

In designs, the common source (CS) amplifier is used for wideband LNA [3-5]. Nonetheless, sophisticated methods are sometimes required to enhance the inadequate input matching for CS-LNA. In order to achieve broadband, source degeneration inductors were employed in [3], and in [4], a bandwidth augmentation method was implemented. Wideband LNA was achieved using the common gate (CG) amplifier in earlier systems [6–12], which can offer better wideband input matching. Nevertheless, excessive power consumption disturbs CG-LNA. In order to solve the above scenario, a gm-boosting method was put forth in [11]. In [10], the current- reuse approach was also a contender. In addition, the poor gain in [10] was a disadvantage that necessitated additional stages. As demonstrated in a number of studies [1,2,13–24], the cascade LNA has favorable high gain, broadband matching, and high reverse isolation when compared to CS and CG structures. This paper proposes a multi-band wideband LNA based on the cascode structure. Since the differential form has a high resistance to power supply and common-mode noise, it is used to make system-on-chip integration easier.

The manuscript reminder is structured as follows: Section 2 presents the LNA's structure, input/output requirements, and interstage matching; Section 3 provides the LNA's measurement findings; and Section 4.

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2. ELECTRICAL SCHEMATIC

Figure 2 displays the proposed LNA's schematic. The LNA is made up of three stages in order to achieve a high gain; the differential cascode amplifier is referenced to understand the basic architecture of each stage. The input/output and interstage impedance matching are crucial for a multi-stage LNA. Baluns are used in this study to achieve advantageous matching. Because it greatly affects NF, bandwidth, and gain, the first stage of the LNA is crucial. The first stage features cross-coupling capacitors and source degeneration inductors in contrast to the later stages. The LNA's input and output ports match to 50 Ω.

1.1. The LNA's Structure and Operation

As illustrated in Figure 3, the input port of a conventional differential cascode amplifier can be comparable in terms of impedance matching to a parallel RC network because of the influence of parasitic capacitances CGS and CGD. The impedance seen from the input port is translated to an equivalent shunt resistance that is about kilo-ohms in value. When a resistance of kilo-ohms is matched to 50 °C, the inductor in balun will be huge, accounting for the great bulk of the chip area. To address the aforementioned issue, Figure 4a illustrates the introduction of a series RC feedback link between the circuit's input and output ports. Equation (1) illustrates how the feedback link can be thought of as being equivalent to the impedance Rmiller at the input port when taking the Miller effect into account. The circuit's open-loop gain, denoted by |Av|, is equal to the feedback resistance, Rf. The real portion of the impedance observed from the input port is reduced by connecting the equivalent network of the input port and the Rmiller in parallel.

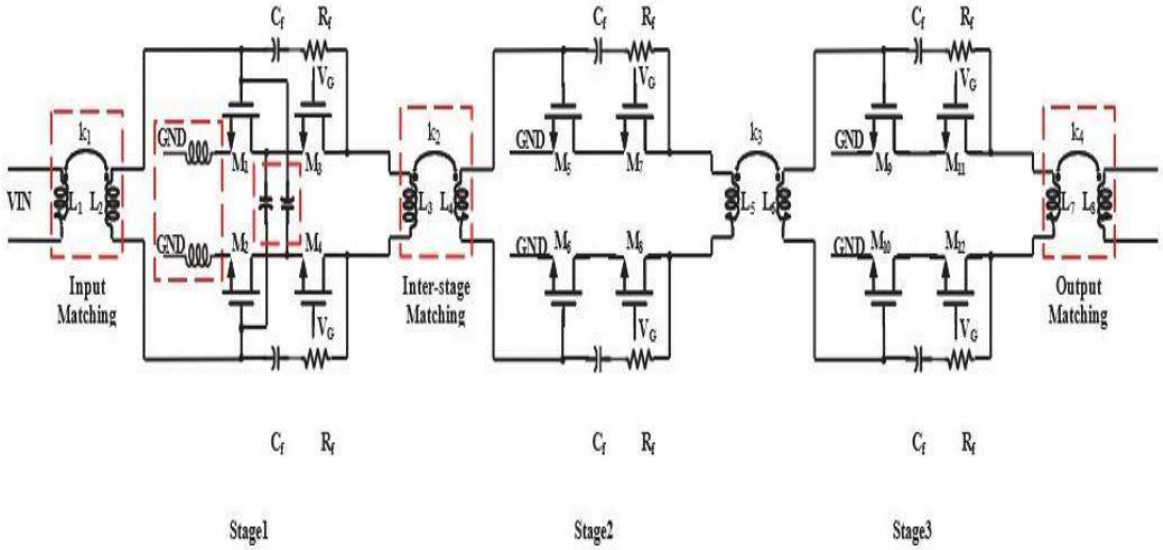


Figure 2: The proposed LNA's schematic

M_1-M_{12}	64 µm/40 nm	L_3	553 pm
k_1	0.6 V/(cm·Oe)	L_4	207 pm
k_2	0.57 V/(cm·Oe)	L_5	553 pm
k_3	0.57 V/(cm·Oe)	L_6	207 pm
k_4	0.57 V/(cm·Oe)	L_7	802 pm
L_1	221 pm	L_8	331 pm
L_2	600 pm	V_{DD}	1.2 V

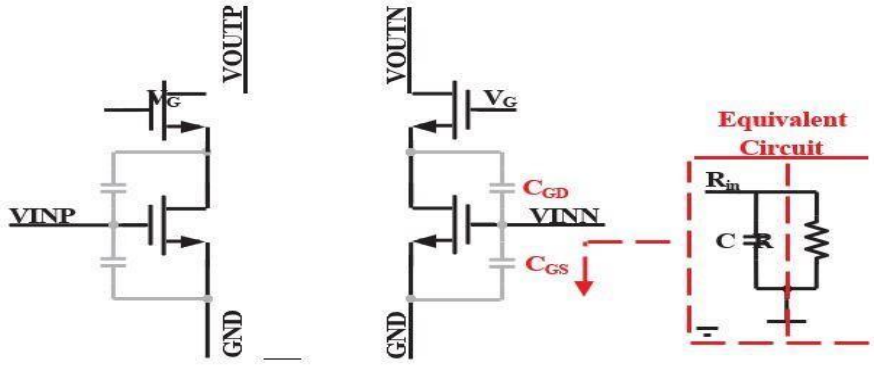


Figure 3. The traditional differential amplifier and the input equivalent circuit.

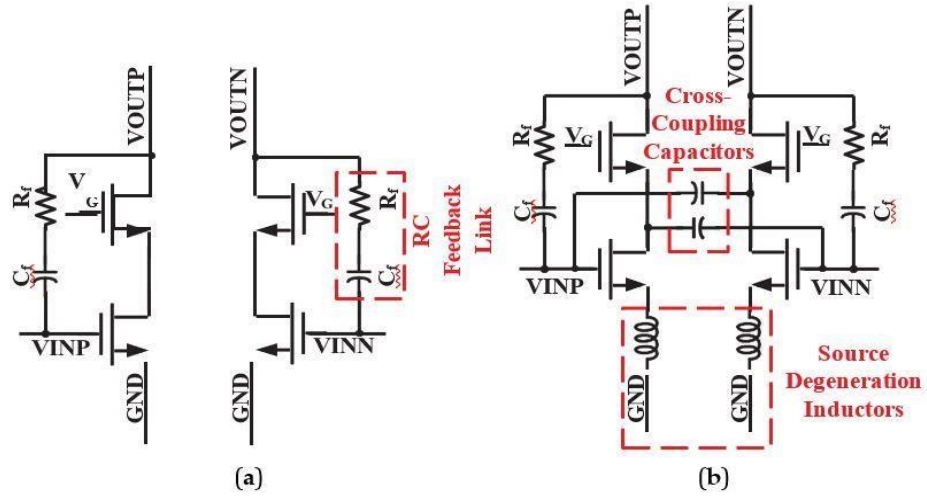


Figure 4. (a) incorporating feedback links that follow the standard differential cascode amplifier design; (b) including more crosscoupling capacitors and a source degeneration inductor

As seen in Figure 4b, the source degenera-tion inductors are added to the first stage in order to lower the input port impedance and improve the noise characteristics, further satisfying the input port's 50 Ω impedance matching. Cross-coupling capacitors are inserted concurrently, which can remove parasitic effects and offer a gmboost. The first stage's S21 and NF simulation results, both with and without cross-coupling capacitors, are displayed in Figure 5. With S-parameter analysis, Cadence Virtuoso Spectre RF simulates gain, input return loss (S11), noise figure, and input impedance.

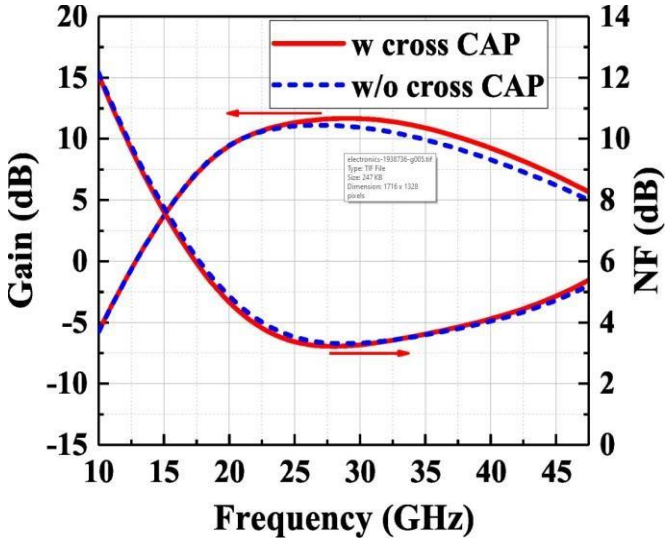


Figure 5. The simulation results for gain and NF of the LNA with and without cross-coupling capacitors.

The transistors (M1–M12) are constructed as 16 fingers with a total channel width of 64
μm, considering the power consumption, input impedance, and gain of the proposed LNA. Figure 6 displays the structures of the suggested LNA, which goes through an equivalent transformation from series to parallel, as well as the simulation results of the impedance of the standard differential cascode amplifier, assuming that the transistors are the same size. The typical cascode amplifier is shown by the black line. The circuits are represented by the blue and red lines, respectively; in one, only the feedback link and the degeneration inductor are added, while in the other, both.
They are both built upon the conventional cascode amplifier.

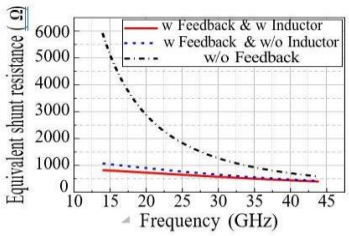
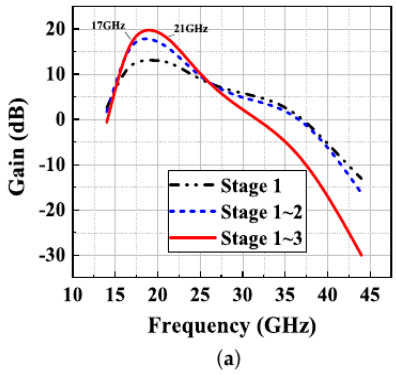


Figure 6: The suggested LNA's architecture and the impedance of the conventional differential cascode amplifier.

Gain is sacrificed in the first stage of the LNA in exchange for excellent input matching
and minimal NF. To increase the gain, two more stages are added. In addition to its high gain, the LNA is controlled by a 2-bit signal and has three operating bands. Figure 7 displays the results of the gain simulation for stepwise circuits in three bands.



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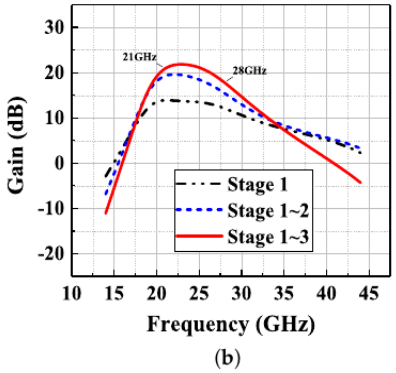

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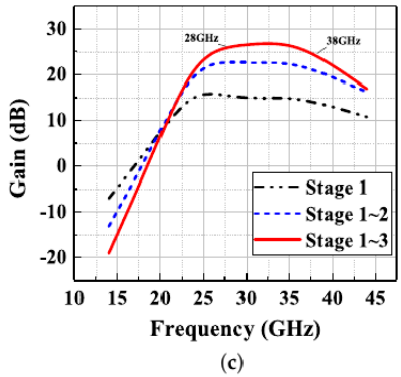


(c)

Figure 7. The gain of all stages simulated in (a) 17–21 GHz, (b) 21–28 GHz and (c) 28–33/38 GHz

1.1. Network for Matching Magnetically Coupled Resonators (MCRs)

The MCR matching network is used for impedance matching in order to get a wide bandwidth [25]. Using input port matching as an example, 50 Ω is translated from the resistance observed through the balun. The input port matching network and the corresponding network on either side of the balun are depicted in Figure 8. The following are the necessary requirements for the matching network, as seen in Figure 8b: Tank 1's R1 is 50 °C, and by translating the available simulation data, tank 2's R2 and C2 may be found. Based on this, L1, L2, and C1 values can be ascertained, provided that the networks' resonance frequencies are distinct. The resonant frequencies of the RLC networks on both sides are adjusted to differing frequencies, f1 and f2, in order to increase the bandwidth. As a result, the S21 image of the balun can produce two peaks, as seen in Figure 9. In the 28–33 GHz range, Figure 10 displays the gain and S11 simulation results of the first stage with various magnetic coupling coefficients k. The LNA's bandwidth expands with an increase in coefficient. K is constrained in balun, though. The interstage matching and output are treated in the same way.

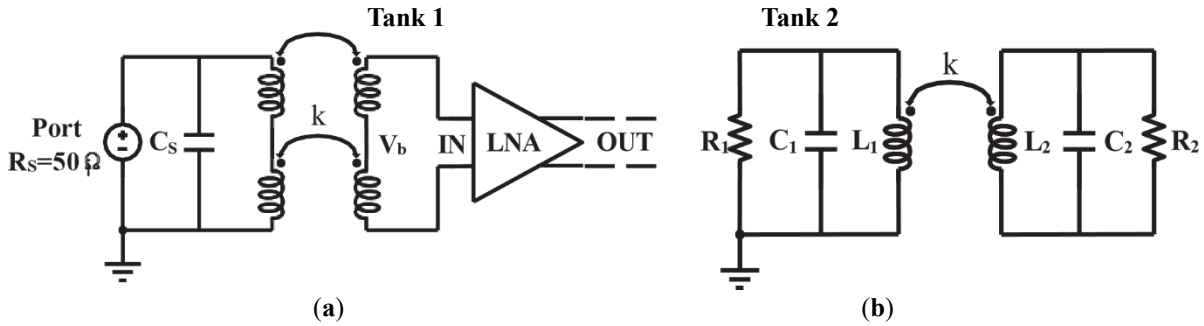


Figure 8. (a) The input port matching network, as well as (b) the balun's corresponding circuit.

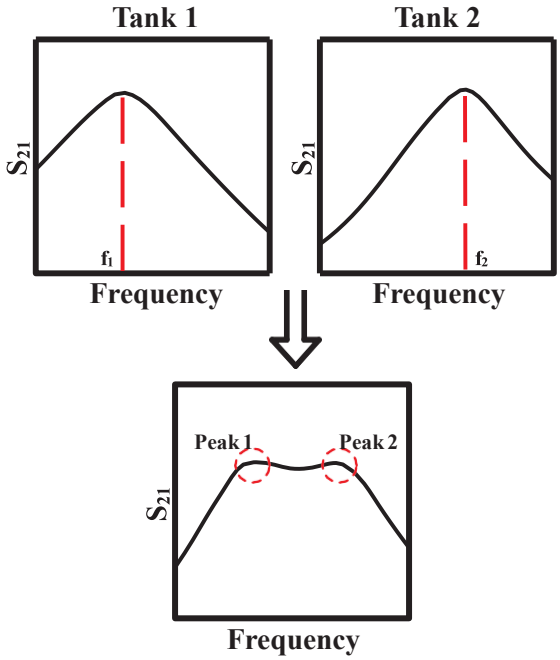


Figure 9. Wideband technology.

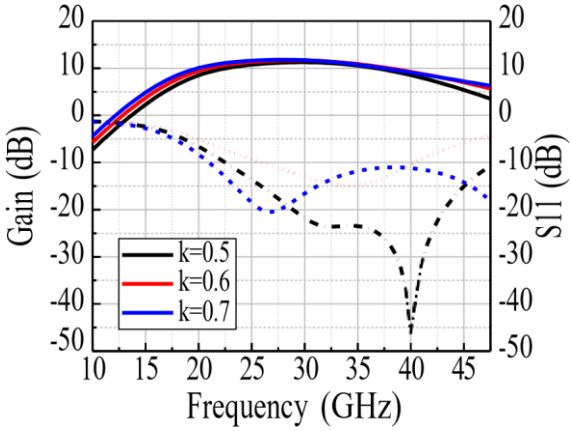


Figure 10. Gain and S11 simulation results of LNA with different magnetic coupling coefficients.

The LNA's three working bands are a result of the trade-off between gain and bandwidth. With the introduction of switch capacitances, three operational bands can be switched using a two-bit control signal. For the switching transistor design, there is a trade-off. Larger switching transistors have better conduction characteristics, but because of their high parasitic capacitance, the matching issue becomes worse. On the other hand, because of its low equivalent shunt resistance, a small switching transistor increases power consumption but has less effect on matching.The switch capacitances built into the LNA are displayed in Figure 11 and are inserted parallel at both the input and output ports of each stage. The S11 simulation results of the are displayed in Figure 12

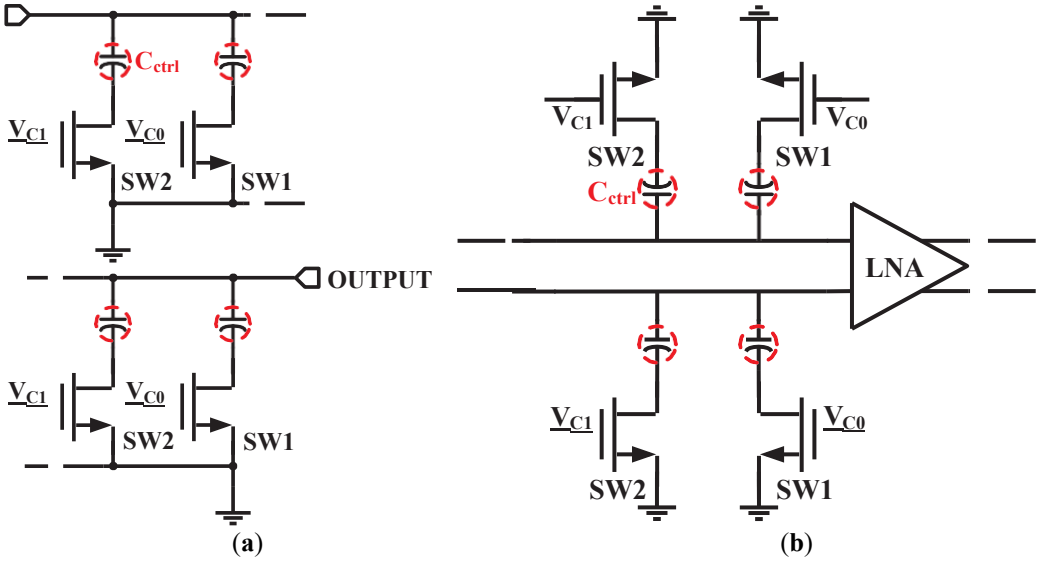


Figure 11. The switch capacitances in LNA (a) for input/output port and (b) for interstage coupling.

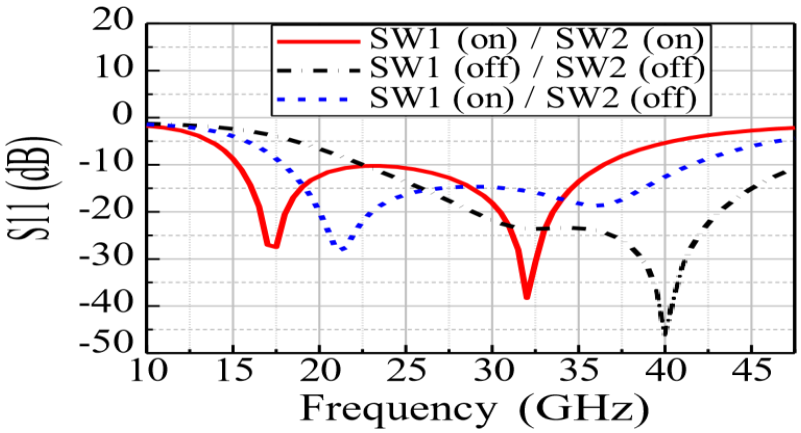


Figure 12. S11 of LNA with switch capacitors in different states.

A shift in capacitance is correlated with a shift in resonance frequency. When the transistor is turned off, the switch capacitance is in the high-impedance state; conversely, when the transistor is turned on, it is appropriately capacitive. In the

latter instance, the input port's capacitance is increased by the CTRL being linked in parallel with the transistor's parasitic capacitance. Based on the assumption that the matching inductance of the balun stays constant, ω = 1/ LC indicates that the resonant frequency will shift to a lower frequency. By applying this approach, both sides of the balun simultaneously expand their resonance frequencies to low frequencies. As a result, the operating frequency band migration can be realized by the LNA.

2. Measurement Outcomes

The 32-nm CMOS SOI technology is used in the design and implementation of the LNA. The die micrograph of the LNA, which takes up 0.94 by 0.34 mm2 of chip space, is displayed in Figure 13. With × a 1-V supply, the power usage is 59 mW. During the measuring process, the chip is tested beneath the probe station. Through GSG RF pads on the chip and Cascade RF probes, the input and output of the LNA are directly connected to the test equipment. Figure 14 displays the block diagram of the measuring setup. A single V power supply is provided via an Agilent E3646A DC source. The S-parameters, gain, and NF are measured using an Agilent N5232A Vector Network Analyzer (VNA). Prior to measurement, the probes and connection cables are calibrated to.

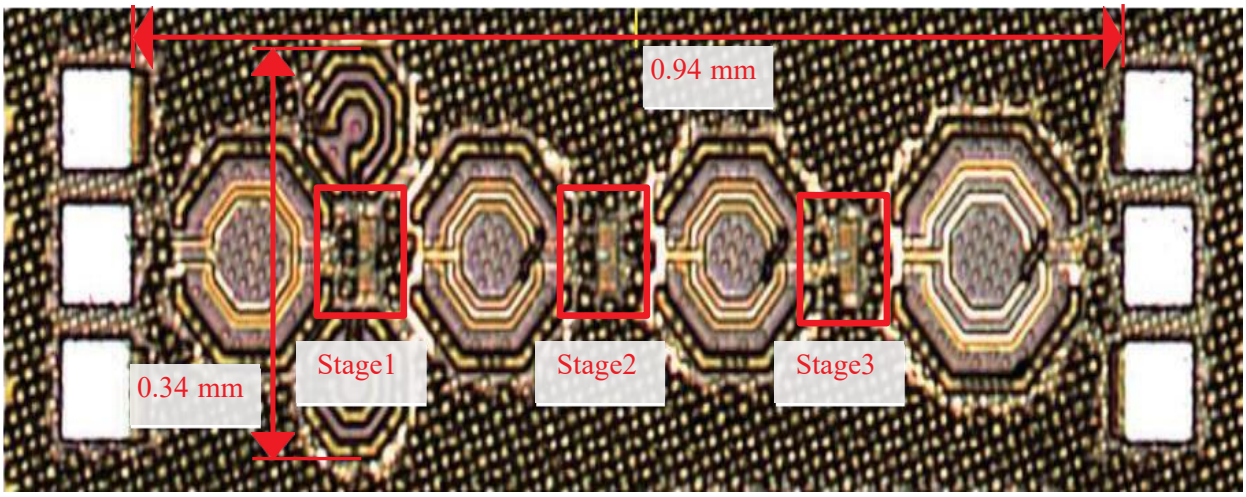


Figure 13. The die micrograph.

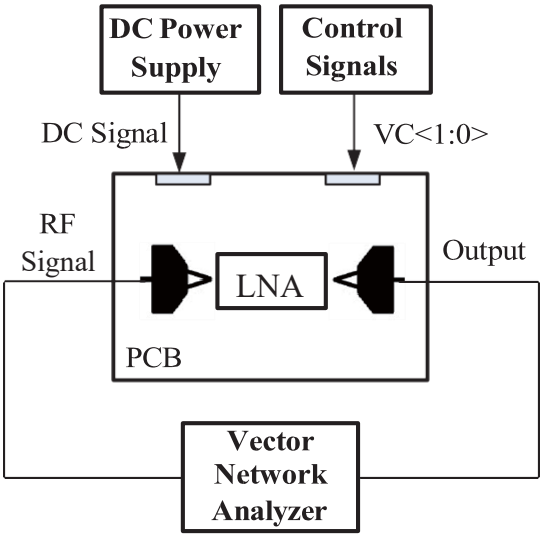
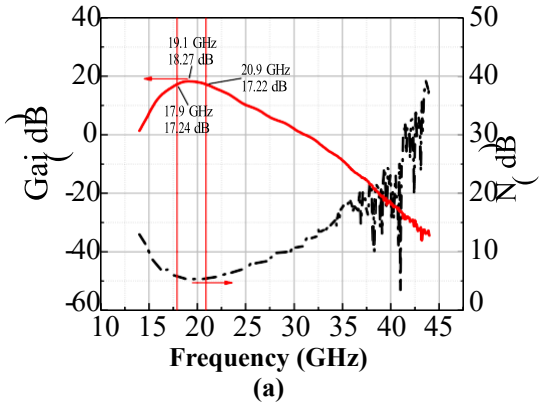
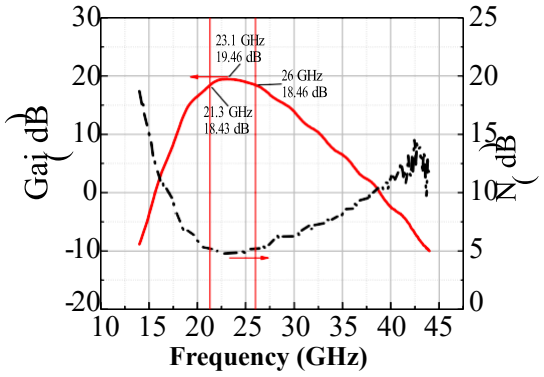


Figure 14: The configuration for measurements.

The measurement findings of the S21 and NF at 17–21 GHz, 21–28 GHz, and 28–33 GHz are displayed in Figure 15. The lowest NF in each band is 5.2 dB, 4.7 dB, and 4.0 dB, although the maximum gain is 18.3 dB, 19.5 dB, and 23.0 dB. In each working range, the measured 1-dB gain bandwidth is 3 GHz, 4.7 GHz, and 5.4 GHz, respectively.
The lowest NF and greatest gain are summarized in Table 1.

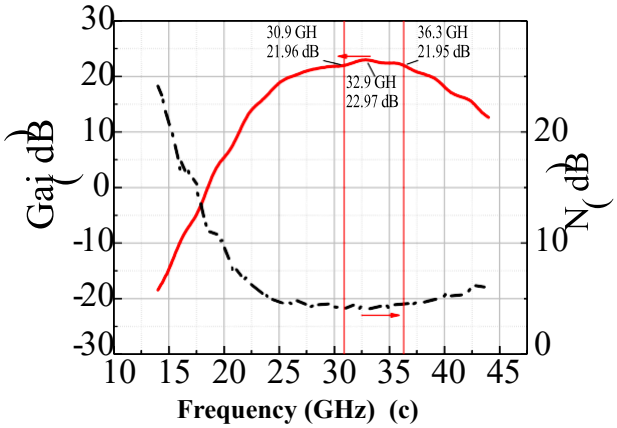


(a)



(b)

Figure 15. ***Cont.***



(c)

Figure 15. The measured gain, and NF at (a) 17–21 GHz, (b) 21–28 GHz and (c) 28–33 GHz.

Table 1. The performance summary.

Frequency Band (GHz)	Maximum Gain (dB)	Minimum NF (dB)
17–21	18.3	5.2
21–28	19.5	4.7
28–33	23.0	4.0

Figure 16 shows the synthesis of gain and NF measurement results in three bands exhibiting that the LNA can provide high gain and low NF across the full frequency band. A figure of merit (FOM) for evaluating the performance of a broadband LNA is defined as Equation (2).

$$FOM[\,] = \frac{GHz\ S^{21}[mag] * BW[GHz]}{mW\ (NF - 1)\ [mag] * PDC\ [mW]} \quad (2)$$

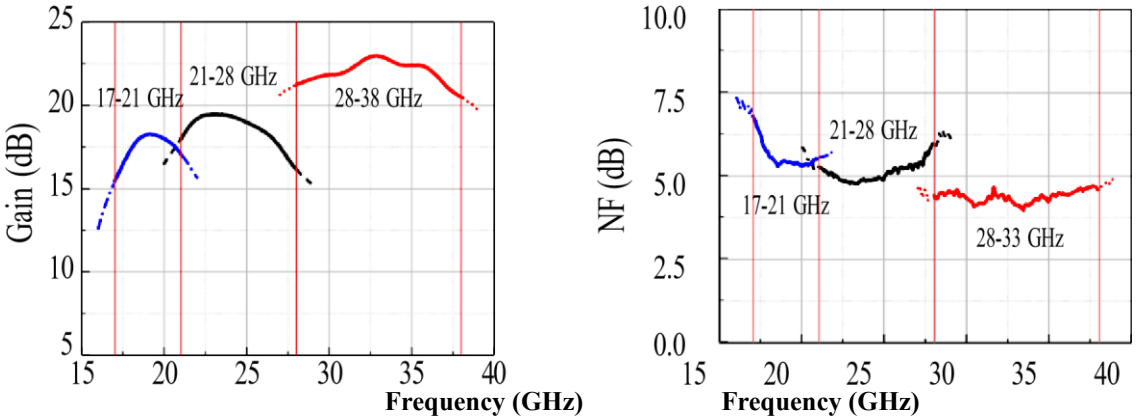


Figure 16. The synthesis of (a) gain and (b) NF measurement results in three bands.

The performance of this design and the most advanced wideband LNAs is contrasted
in Table 2. The LNA in [9] has a narrow band, low gain, and low power consumption even though it can run on two supply voltages. The cascode structure was also utilized by the works [16,17,23, 24]. On the other hand, [16,23] employed low gain, [17] featured narrow bands, and [24] had a worse NF. It is clear that the best FOM of 4.9 GHz/mW is achieved by this effort. The
The suggested LNA has a broad operating spectrum that spans 17–33 GHz and achieves high gain, low NF, and high FOM..

Table 2: The suggested LNA's compiled performance.

Reference	Process	Architecture	Supply Voltage (V)	Bandwidth (GHz)	Gain (dB)	NF (dB)	FOM	Area (mm^2)
[9] [a]	0.13-µm CMOS	CG	0.6 1.2	17.3-29.3 17.3–29.3	15.4 18	5.5–7 4.7–6.2	- -	0.192 [b]
[17]	65-nm CMOS	Cascode	-	30–34.5	20.8	3.71	1.4	0.39
[16]	32-nm CMOS SOI	Cascode	1	24–30	11.2	3.2	0.7	-
[23]	65-nm CMOS	Cascode	-	15.8–30.3	10.2	3.3–5.7	3.3	0.18
[24]	0.18-µm BiCMOS	Cascode	1.8	22–32.5	18.6	4.5–5.5	-	0.46 [b]
This work	32-nm CMOS SOI	Cascode	1	17–21 21–28 28–32	18.3 19.5 23.0	5.2 4.7 4.0	4.9	0.42 [b]

2.CONCLUSIONS:

The differential cascode amplifier, RC feedback link, and source degeneration inductor that make up the multi-band LNA are designed and built in a 32-nm CMOS SOI process in this study. The three-stage LNA uses baluns for input/output and interstage impedance matching in order to achieve high gain, broadband, and low NF. Three operational bands—17– 21 GHz, 21–28 GHz, and 28–33 GHz—can be switched while the proposed LNA is functioning by adding switch capacitances. The measurement's findings indicate that the device occupies a 0.94 x 0.34 mm2 chip area, with a maximum gain of 23.0 dB and a minimum NF of 4.0 dB. For multi-band LNA design, this work has a specific reference value.

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