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Ring Oscillator-Based High-Speed True Random Number Generator with a Minimal Footprint

Abstract: - A fundamental component of every cryptographic system is a True random number generator. TRNG generates the security key with other applications in secure communication. In general, analog components, high-gain amplifiers, and analog-to-digital converters (ADCs) are used in traditional TRNGs. Recently, many TRNGs have been published, but a few may be put into practice using field-programmable gate arrays. This manuscript presents a TRNG using the ring oscillator which can be easily implemented in FPGA, providing high randomness with good statistical results for requirements like area, speed, and power consumption. The proposed TRNG is tested in FPGA families in Vivado version 2018.3 design suite, XC7A100TCSG-1 (Artix 7). The Generated bit stream of TRNG passed all the NIST tests. Moreover, along with the application of a feedback style system, the robustness of a TRNG is explored, and the locking of the ring oscillator is protected. The proposed TRNG achieves 2500 Mbps throughput after a Lineal feedback Shift Register used as a post-processing Unit, which gives a speed 1.8 times faster than presented by other work done on FPGA-based TRNGs.

Keywords: National Institute of Standards and Technology, Metastability, Ring Oscillator, D Flip-flop, Artix-7, True random Number Generator

I.INTRODUCTION

Non-deterministic number generators are useful for creating secure keys [3], encryption generation, and masking of channels [2] - [5]. Previously noise generated within the electronic device is used to produce randomness. Presently FPGAs are used more popularly for used to integrate cryptographic systems on a chip [6] - [9], [20], As a building block of cryptographic systems, all security requirements must be followed by TRNGs [1], [10] - [13], [26-27]. The randomness of TRNG depends on the characteristics of the analog physical source, digitizer, and selected technology [14] - [17].

RNGs must produce unexpected results for cryptographic applications. However, certain physical sources (for example, date/time vectors) are very predictable. By mixing outputs from many sources to use as an RNG's inputs, these issues may be lessened. However, statistical testing may reveal that the RNG's outputs are still insufficient. Furthermore, producing high-quality random numbers may take too long, making it unsuitable for producing huge quantities of random numbers. True random number generators could work better if you need to generate a lot of random numbers [20]. The concept of the non-deterministic number generator and its realization were validated mathematically for testing and certification. The generated sequences were tested with the help of DIEHARDER [42], and NIST SP 800-22 [20]. Various statistical tests may be applied to a sequence to compare and assess it against a random sequence. Since a random sequence's qualities are probably defined and described in the form of probability, randomness is a probabilistic attribute. When mathematical validation is performed to a random sequence, the anticipated outcome is known ahead of time and may be stated probabilistically [41]. There are an unlimited number of alternative mathematical tests, each of which assesses the existence or unavailable of a "pattern" that, if identified, indicates that the sequence is deterministic. A limited set of tests is never considered "complete" since there are countless ways to determine whether a sequence is random or not. Furthermore, the outcomes of to prevent drawing inaccurate conclusions about a particular generator, statistical testing must be evaluated with care and prudence.

The earlier demonstrated RO-based TRNG implemented in FPGA by M. Baudet in the year 2011 used two ROs as the source of randomness number generator [5]. This TRNG requires a relatively smaller footprint at the expense of less speed to provide a sufficient entropy rate with high-security potential. The TRNG has higher power consumption if the frequency of the clock signal is increased [37]-[39].

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A coherent sampling-based True random number generator (COSO TRNG) published in the year 2004 by P. Kohl Brenner uses two oscillators and a positive edge triggered D FF. This TRNG provides a relatively high speed with a very small footprint but has difficulty in designing [6]. [24] presented FPGA using the variable delay generator random jitter of a MOSO ROs as the source of entropy, and achieved 290 Mbps throughput. More than one ROs-based TRNG uses 'm' independent ring oscillators [7]. The TRNG occupies a larger footprint and has the issue of locking rings. In the proposed TRNG we use 16, 24, and 31-ROs, an XOR, and a D FF.

Our objective is to perform on different numbers of ROs to compare area, power consumption, and throughput. So that we can select any of the designs individually as per the required application. They provide a different bit rate with a small area and eliminate the problem of locking rings. This is the work where correlation of Ring oscillators increased random number rates, hence a greater number of ROs. Increase more chance of non-deterministic number stream which is more suitable for security application. So, by using Ring Oscillators proposed work has small resource overhead and achieved high throughput.

Our Contributions: (1) This work has comparison of different entropy source on the base of parameter gain, area, power consumption and throughput. (2) There are issues in stability of randomness, not enough probability and insufficient throughput of random number generator, so proposed design has sufficient oscillations of self-time rings and got exactly by jitter latch structure.

The work is arranged in the immediately following manner. In section 2 the proposed design with structure is presented. In section 3 Vivado 2018.3 Experimental result of the proposed TRNG is discussed. Section 4 consists of NIST test results. In section- 5 conclusions are given.

II.PROPOSED DESIGN

Ring oscillator-based TRNG is presented in Figure. 1. TRNG consists of a 31-ring oscillator (RO0 – RO30), XOR, and rising edge triggered D Flip-Flop. RO is designed by connecting an N+1 of the inverter gate arranged series with the feedback connection from the last inverter gate to the first inverter gate. In the presented TRNG RO0 has five inverter gates in series RO1 has seven inverter gates in series, RO2 has nine inverter gates in series, RO3 has eleven inverter gates in series, RO4 has a thirteen-inverter gate in series, RO5 has a fifteen-inverter gate in the series, RO6 have a seventeen-inverter gate in the series and RO7 have a nineteen-inverter gate in the series likewise N+2 investors are increasing. So, for different numbers of ROs numbers of investors are in increasing in order respectively. By using such an N+1 quantity in several inverters in the queue prevents the locking of ROs.

Meta-stability in the proposed TRNG is designed on the base of delay produced by the series combination of inverters. A different amount of delay is produced depending upon the selection of the RO. The amount of randomness of the output is determined by the time duration of Meta-stability, which again depends on the number of inverters in the series. These all bits coming from each RO are added through the XOR process and the final output is given to the harvester which is to D Flip flop and due to Meta-stability, which is produced by the delay between input and clock signals, randomness is generated. For better results, we have used two D-flip-flops as a harvester. In the proposed design feedback mechanism is adapted to protect the RO from being locked as shown below the Figure 1.

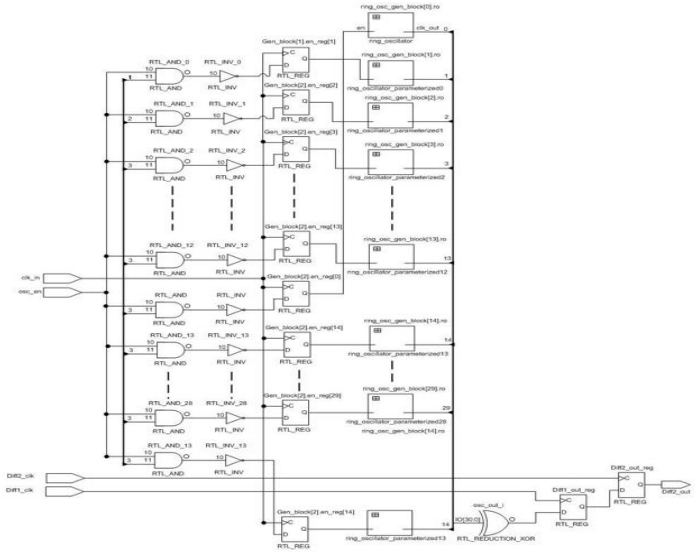

Figure 1. Structure of Proposed TRNG Using ROs.

III.IMPLEMENTATION & EXPERIMENTAL RESULT OF PROPOSED TRNG

The schematic diagram of Vivado in version 2018.3 an implementation of the proposed designed TRNG is presented in Figure. 2 The schematic circuit of a proposed presented True Random Number Generator with PPU is shown in Figure. 4. PPU is designed with a 16-bit linear feedback shift register (LFSR) which gives a final nondeterministic bit stream.

A parameter related to Vivado version 2018.3 implementation is shown in Table 1. The result shows that the area required for different numbers of Ring Oscillators in Vivado 2018.3. We have taken 100ns invertors delay and tried for more than 50 different frequencies to get non-deterministic numbers. For each number of ROs, we get success at different frequency levels. The result also shows that the inclusion of PPU increases the area but does not have any effect on the bit rate. The proposed design of TRNG passed the NIST test with and without PPU is shown below the Figure 3.

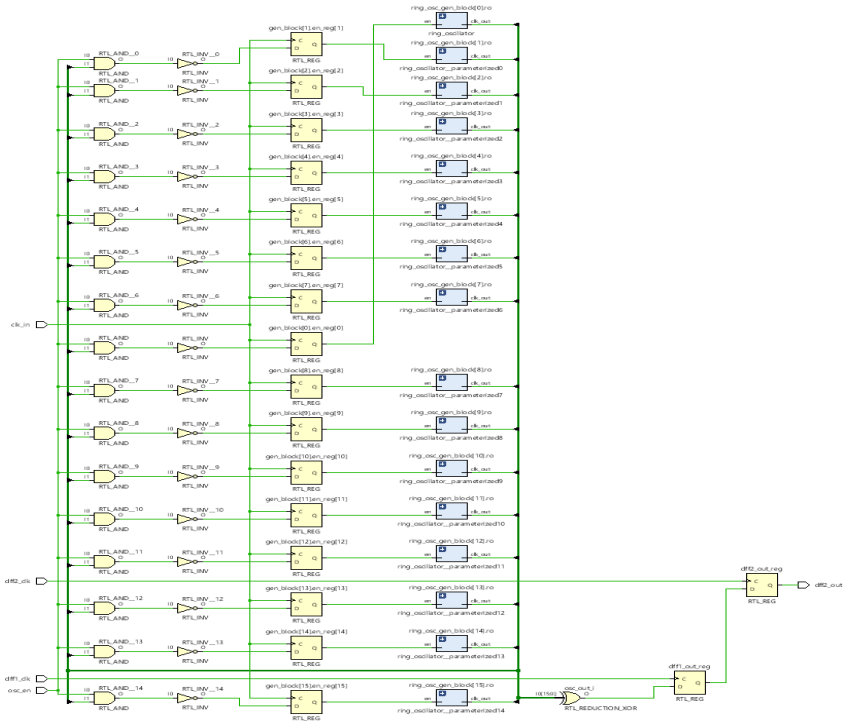

Figure 2. Schematic of Vivado 2018.3 implementation of TRNG

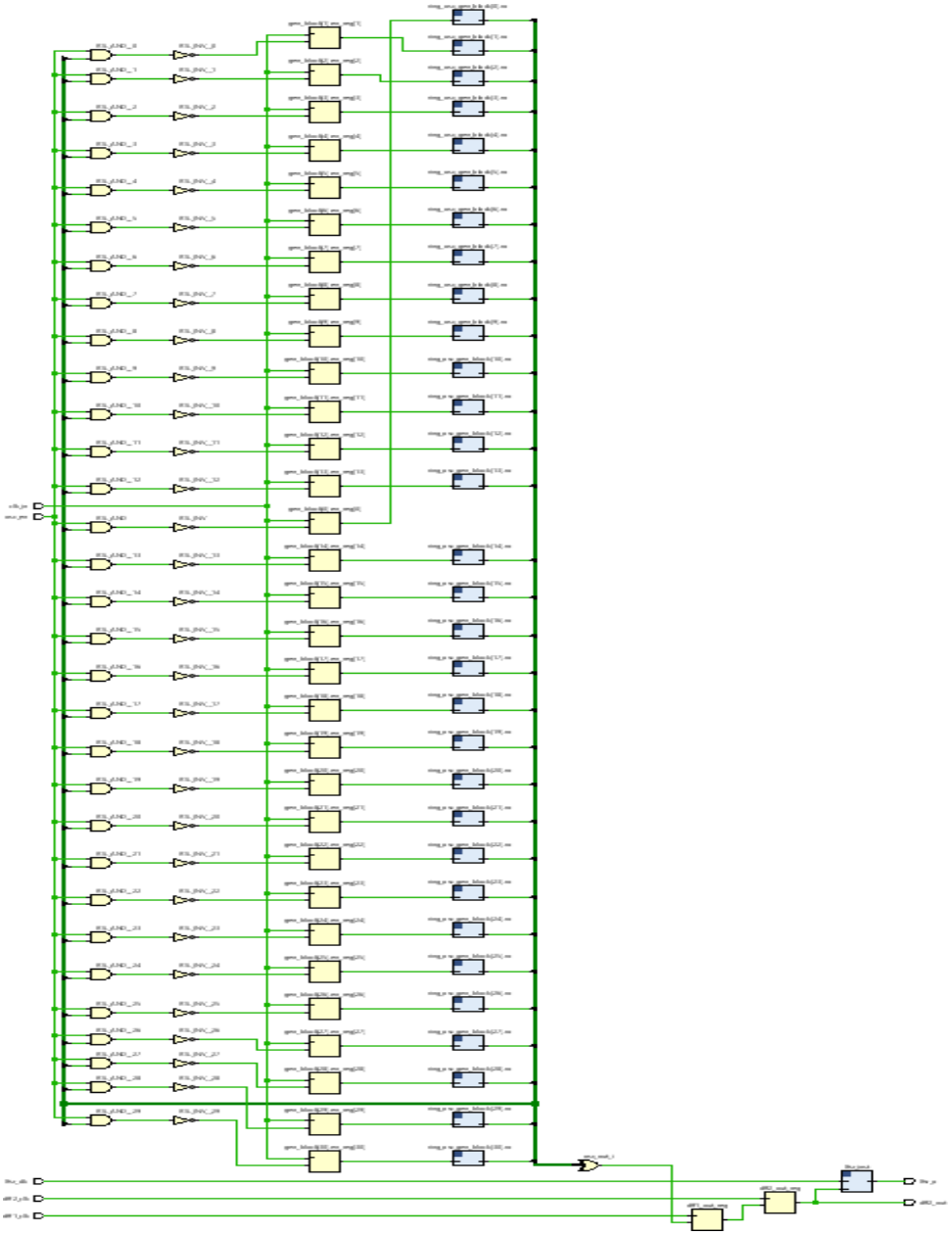

Figure 3. Schematic of proposed TRNG with PPU

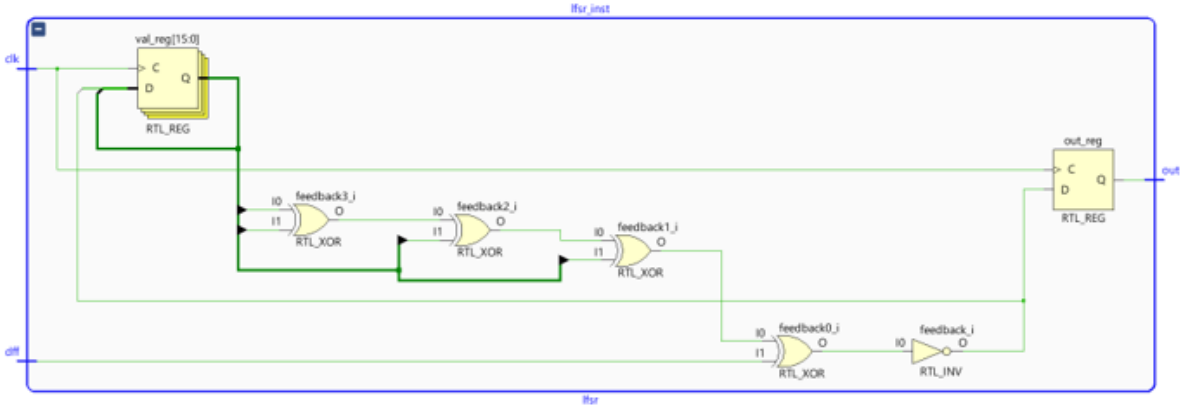

Figure 4. Schematic of 16 bits LFSR

Table 1. Parameter about the VIVADO 2018.3 implementation of planned TRNG

Without Post Processing Unit					With Post Processing Unit			
No. Of ROs.	Area (LUT+FF)	Gain	Power Consumption		Area (LUT+FF)	Gain	Power Consumption	
			Post Synthesis	Post Implementation			Post Synthesis	Post Implementation
16	44	163.836	2.112 W	1.944W	51	489.84	3.108w	2.921W
24	56	240.9	2.53W	2.580W	60	556.777	3.524w	3.487W
32	71	509.168	2.999 W	2.841W	79	726.070	3.991w	3.833w

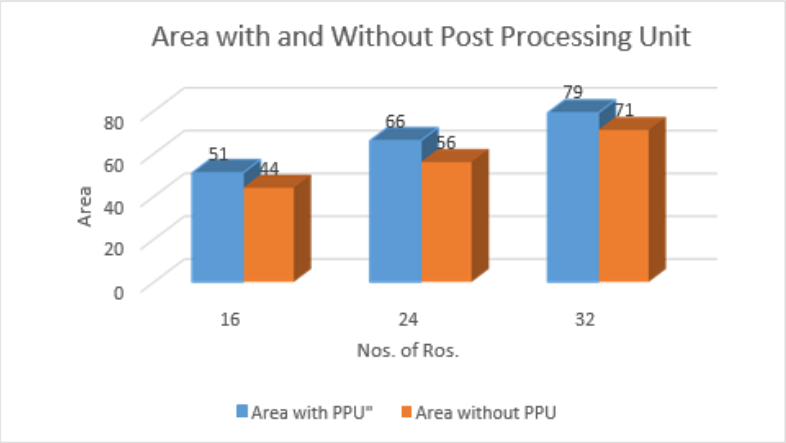

Figure 5. Comparison of Area with and without PPU

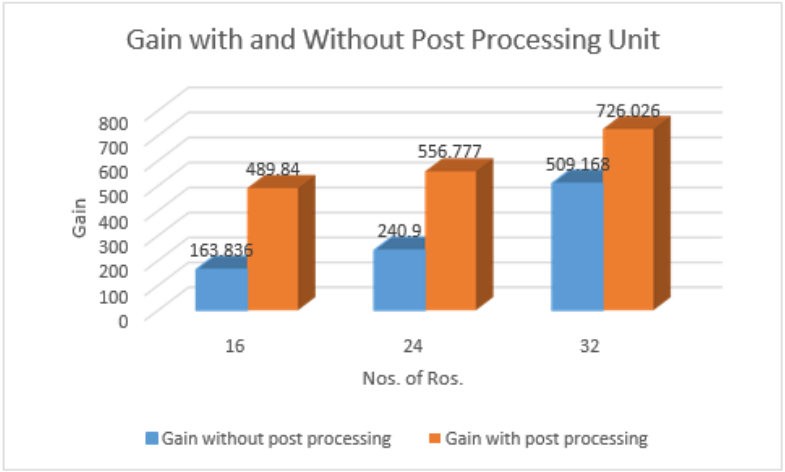

Figure 6. Comparison of Gain with and without PPU

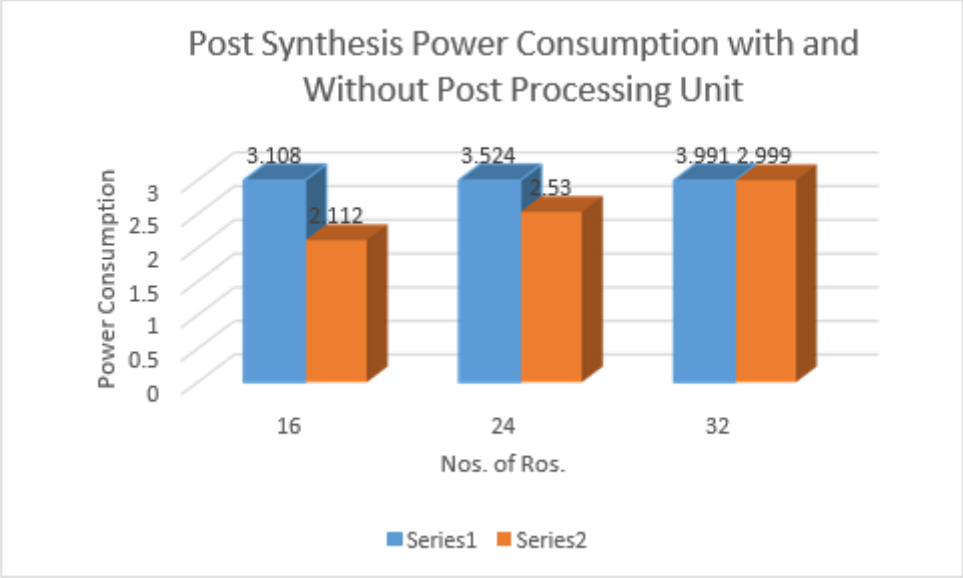

Figure 7. Comparison of Post Synthesis Power Consumption with and without PPU

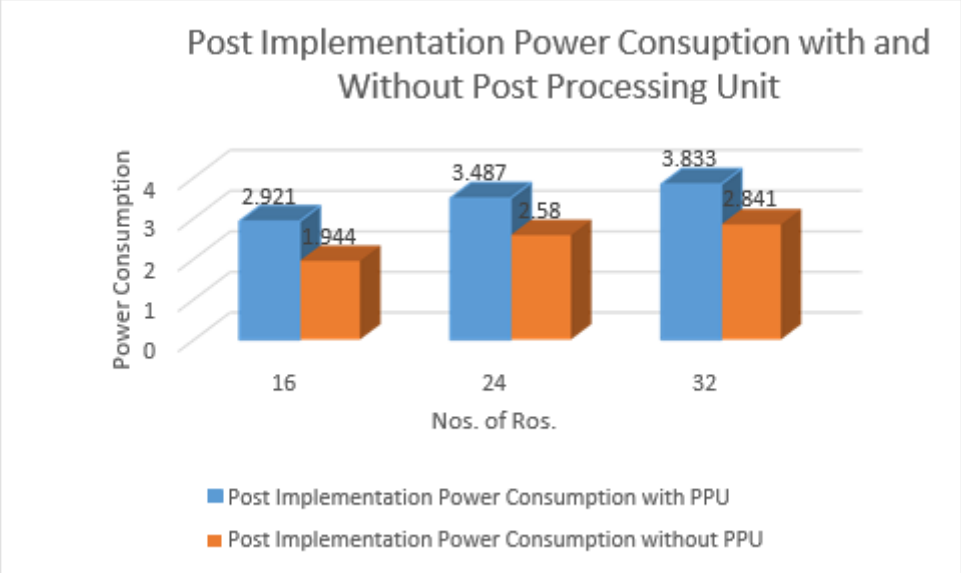

Figure 8. Comparison of Post Implementation Power Consumption with and without PPU

Figures 5,6,7 and 8 area, gain, and power consumption in post-synthesis and post-implementation with and without PPU respectively. As shown in Figures 6 and 7 area and gain are increasing with an increasing number of Ring oscillators. Power consumption is also increasing as the number of increasing ring oscillators is increasing for post-synthesis and post-implementation.

Table 2 shows a comparative analysis of the proposed TRNG with an already published TRNG. Results show that the proposed TRNG required the optimized area i.e. LUT+Reg. 39+40 for the bit rate of 300 Mbps which is comparitvely good than the existing TRNG in Table 2.

Table 2. Parameter available implementation of existing True Random Number Generators

Paper	Device	**Method**	**Area**	**Power Consumption**	**Throughput [Mbps]**

2022[7]	Xilinx Virtex-6 FPGA	MSFRO	26	0.003687	290
2024[11]	Artix-7, Kintex-7	Multiplexer RO	12	0.001	300
2020[14]	Zynq-7000	Three-Edge Ring Oscillator	87	9.514	12.5
2024[18]	Artix-7	Random jitter of GARO	129	*	280
2023[23]	Zynq XC7Z020	DCM hardware primitives to tune the phase shift	159	119	300
2022[24]	Virtex-6	Multi-ring convergence oscillator (MRCO)	17	112	500
2021[30]	65nM CMOS chip design	Ring Oscillator	576	0.26	52
2023[35]	Artix-7	Ring Oscillator	57	4.9	275.8
My Work	Artix-7	8 Ring Oscillator without PPU	44	1.944	115
My Work	Artix-7	8 Ring Oscillator with PPU	51	2.921	120
My Work	Artix-7	16 Ring Oscillator without PPU	56	2.58	125
My Work	Artix-7	16 Ring Oscillator with PPU	60	3.487	179
My Work	Artix-7	32 Ring Oscillator without PPU	71	2.841	300
My Work	Artix-7	32 Ring Oscillator with PPU	79	3.833	300

*Indicates data has not mentioned

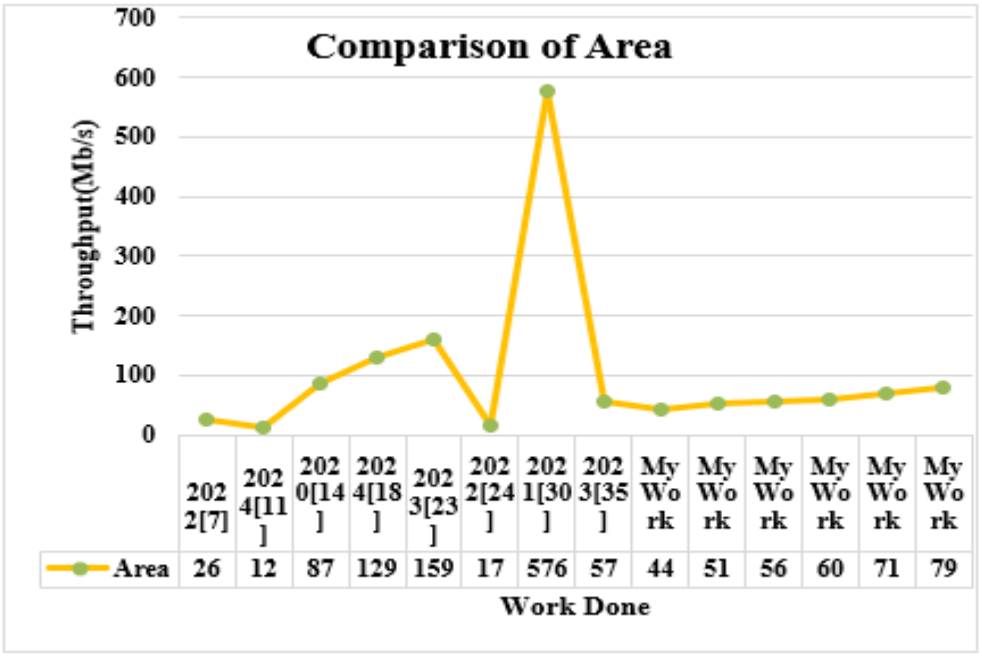

Figure 9. Comparison of Area with existing TRNG design

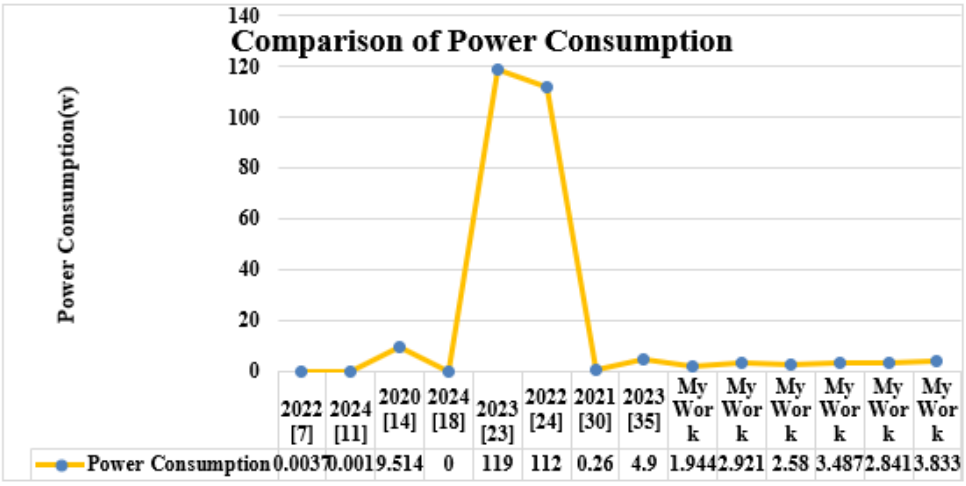

Figure 10. Comparison of Power Consumption with existing TRNG design

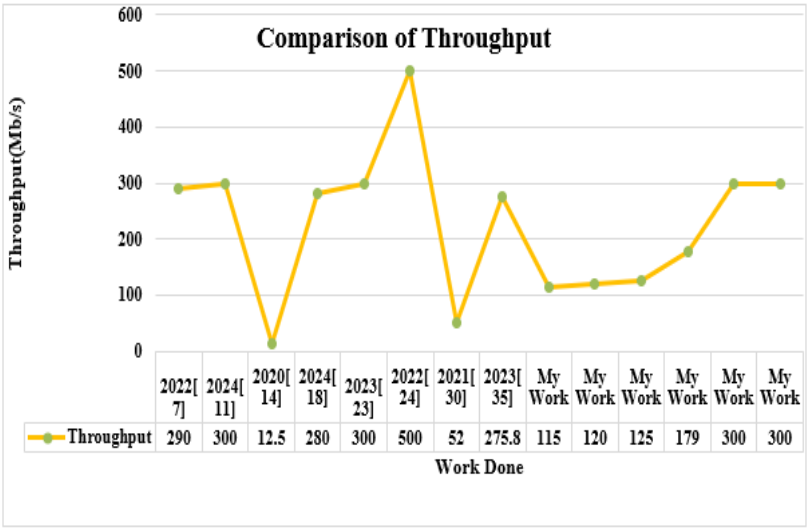

Figure 11. Comparison of throughput with existing TRNG design

The total power consumption after implementation from ISE power analysis, area and throughput is shown in Table 2. This design is also compare with other TRNGs. Based on methods used to get random numbers. As per observation in latest research work speed is compromise in cost of area and power. So, out of all proposed work 32 Ring Oscillators with post processing unit and without post processing unit generates random numbers of throughput 300Mbps in cost of total 79 LUTs and FFs area is shown on above figure 9,10,11.

IV.TEST RESULTS PERFORMED IN NIST

The test performed in NIST and the result of the proposed signed TRNG is presented in Table. 3 which shows that the p-value is always greater than the threshold value of 0.01 for randomness [20]. Hence the proposed system behaves as TRNG.

Table 3. Test performed in NIST and results of TRNGs with and without PPU

NIST tests	Without PPU			With PPU		
	16	24	31	16	24	31
Monobits	0.410	0.774	0.488	0.483	0.443	0.293

Frequency Test within a Block	0.398	0.505	0.678	0.763	0.551	0.136
Cumulative sums	0.234	0.367	0.456	0.679	0.327	0.860
The Runs Test	0.543	0.690	0.780	0.450	0.991	0.234
Longest run	0.141	0.577	0.457	0.983	0.383	0.490
Rank	0.439	0.398	0.867	0.899	0.389	0.460
FFT	0.589	0.789	0.848	0.450	0.680	0.728
The Non- overlapping Template Matching Test	0.998	0.799	0.120	0.450	0.862	0.399
Overlapping template	0.740	0.399	0.270	0.200	0.490	0.894
Universal	0.900	0.298	0.470	0.332	0.670	0.731
Approximate entropy	0.321	0.378	0.347	0.999	0.690	0.780
Random excursion	0.456	0.690	0.580	0.230	0.398	0.723
Random excursion variant	0.554	0.953	0.375	0.376	0.471	0.267
Serial	0.456	0.556	0.715	0.812	0.560	0.178
Linear complexity	0.199	0.788	0.679	0.775	0.390	0.459

> 0.01 value means NIST test pass successfully.

V.CONCLUSIONS

The presented work of RO-based TRNG using multiplexer is implemented in Artix 7 virtual board XC7A100TCSG-1 (Xilinx using Vivado version 2018.3 software design suite. The proposed TRNG clears all NIST tests. The clock timing for the TRNG is taken as 2.719 nanoseconds and resulted speed is 300 Mbps. The implemented and generated outcome represented that the proposed designed and tested TRNG increased 1.8 times and required less area than existing implemented TRNGs done by different authors.

In future work, different algorithms can be used to increase the speed with consumption of less power in post-synthesis and post-implementation by changing several investors, delaying each invertor in each RO, or can take a combination of both. Another future project is to include a TRNG into an IoT (Internet of Things) embedded chip or board to make security a design requirement for IoT-related products. One option, which has fewer implementation restrictions, is to apply TRNGs to the system's gateways. As a result, this work's next challenge may be to distribute random numbers to particular IoT devices for various security purposes.

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