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Design and Analysis of Low Voltage High Mobility OFETs by Using High-K Dielectrics or by Varying Thickness of Dielectric

Abstract: - OFETs (Organic Field-Effect Transistors) are known for its low cost, flexibility, light weight and availability of plenty of organic compounds which makes them a perfect choice for electronic applications. However, stability issues are still a concern in OFETs which limits their efficiency. Also, to be able to employ OFETs for low power consumption devices, their operating voltage should be reduced. To fulfil this requirement, low values of transistor threshold voltage (V_T) and subthreshold swing (SS) are essential. This is a very challenging task as it requires either the gate dielectric thickness to be reduced or by using high-k dielectrics [1]. In this paper, a p-type OFET with DPP (Diketopyrrolopyrrole) as p-type semiconductor [2], SiO_2 as dielectric, Gold as Source and Drain regions is designed and various parameters are extracted like threshold voltage, subthreshold swing, I_{ON}/I_{OFF}, mobility etc. Gate voltage of OFETs is then reduced by varying the thickness of dielectric (SiO_2) and also by varying dielectrics (SiO_2, ZrO_2, TiO_2).

Keywords: BGTC, DPP, high-k dielectric, OFET.

I. INTRODUCTION

Low-voltage devices are lower cost, energy efficient and safe devices. Ideally, to be power efficient, OFETs are operated with gate voltages as low as possible [3]. To design OFETs with low gate voltage, threshold voltage and subthreshold swing need to be reduced. So, either thickness of dielectric needs to be reduced [4] or high k-dielectrics can be used [5].

OFET's drain current equation in saturation region is

$$I_D = \mu \frac{C_i W}{L}(V_G - V_T)V_D - \frac{{V_D}^2}{2} \quad (1)$$

where I_D= drain to source current, μ=field effect mobility, W and L are channel width and channel length respectively, V_G is the gate to source voltage, V_T is the threshold voltage, C_i is the capacitance per unit area of the gate insulator [6].

Ideally, drain to source current, I_D should be maximum while gate to source voltage, V_G should be minimum. But if we reduce V_G then as per eq. (1), I_D will also get reduced which is not desirable. The only parameters that can be changed to compensate for the reduction in I_D are the gate dielectric capacitance (C) and the channel width (W) and length (L). However, W and L depend on the device geometry. Therefore, in order to accumulate the same number of charges within the channel of an OFET and maintain high I_D, it is essential to increase the gate dielectric capacitance (C). The gate dielectric capacitance is given by

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \quad (2)$$

where, ε_0 is the vacuum permittivity (8.854 x 10^{-12} F/m), ε_r is the dielectric permittivity, A is the plate overlap area, and d is the distance between the two plates.

The capacitance varies directly with ε_r and inversely with d. Consequently, in order to increase the capacitance of a parallel plate capacitor, either the dielectric thickness, $d(t_{ox})$ is reduced or dielectric constant, k (ε_r) is increased. So, low voltage OFETs are designed by either reducing the dielectric thickness (t_{ox}) [7] or by increasing the dielectric constant (k).

The manuscript is catalogued as follows, the introduction is covered in section I, the considered device schematic and parameters specifications used for designing is discussed in section II. The results obtained and analyzed with the discussion carried out in section III. A fair conclusion is drawn in section IV with all the enhancements considered.

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II. Device Design Amd Parameters Specifications

A p-type OFET with DPP (Diketopyrrolopyrrole) as p-type organic semiconductor, SiO_2 as dielectric, gold as the source and drain regions is designed. DPP based materials show excellent electronic properties with good thermal and photo-stability [8]. The configuration used here is BGTC (Bottom Gate Top Contact) where gate is at the bottom of the device and source and drain electrodes are kept at the top of the device. As compared to all other configurations such as BGBC (Bottom Gate Bottom Contact), TGTC (Top Gate Top Contact), TGBC (Top Gate Bottom Contact), BGTC (Bottom Gate Top Contact) is preferred due to high drain current and high mobility [9].

Two-dimensional modulated device structure of BGTC configuration is shown below in Fig. 1 and device dimensional parameters are shown in Table 1.

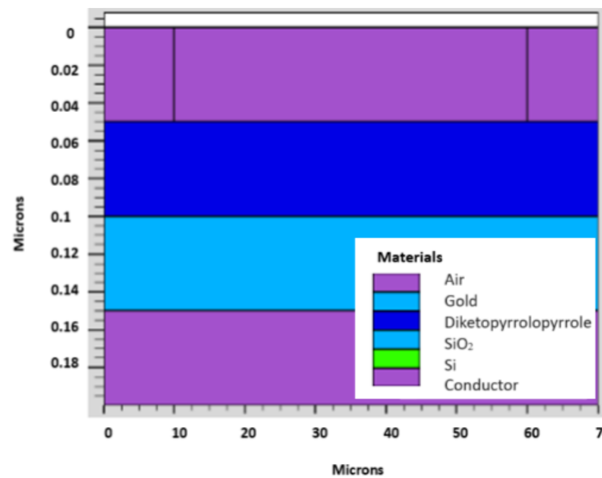

Fig 1 Cross sectional (2D) view of OFET (DPP as p type organic semiconductor), SiO_2=50nm

Table I Device design parameters

Device Dimensional Parameters	Values
Length of the channel, L	50 µm
Width of the channel, W	1000 µm
Thickness of SiO_2, t_{ox}	50 nm

III. Results And Discussions

The simulation results of the above said device are obtained using a 2D Atlas device simulator [10]. The Poole–Frenkel mobility model (pfmob) and Langevin recombination models report the transport and recombination mechanism. These models are used to introduce the effects of mobility and to account for leakage currents. These models have utilized transport and recombination mechanisms within the organic material are accounted for by the Poole–Frenkel mobility model (pfmob) and Langevin recombination models, respectively.

The device shown in Fig. 1 is simulated and transfer characteristics are obtained when thickness of dielectric (SiO_2), t_{ox}=50 nm as shown in Fig. 2. Various parameters are then extracted as shown in the Table 2.

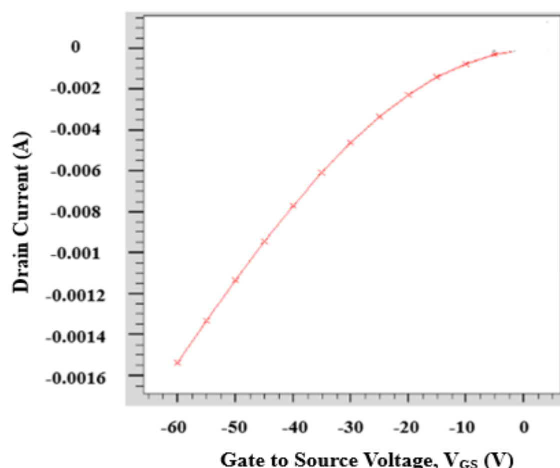

Fig 2 Transfer characteristics with V_{DS} = -60V and V_{GS} = 0 to -60V

Table II Extracted Parameters when t_{ox}=50 nm

Extracted Parameters	Values
Threshold Voltage	-7.383 V
Subthreshold Voltage	6.62 V/dec
Ion /Ioff	2.95 $*10^2$
Capacitance per unit area	$0.6906*10^{-3}$ F/m^2

A. Variation in dielectric thickness

The thickness of dielectric (SiO_2) is reduced (from 50 nm to 10 nm) and transfer characteristics are obtained as shown in Fig. 3 (linear scale) and Fig. 4 (Log scale) [11]. It can be clearly seen in Fig 3 that as the thickness of dielectric, t_{ox} reduces, drain current, I_D increases in negative direction (p type OFET) [12]. As we decrease the oxide thickness, the gate voltage becomes more effective to invert the underlying channel region, which results in an ease of channel formation and hence there is an increase in drain current.

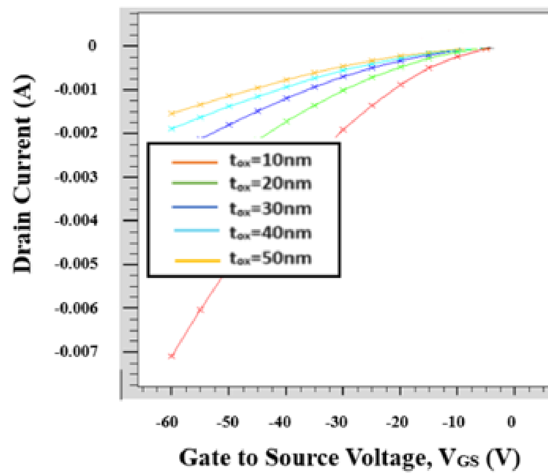

Fig 3 Transfer characteristics (linear scale) with variation in dielectric thickness from 50 nm to 10 nm

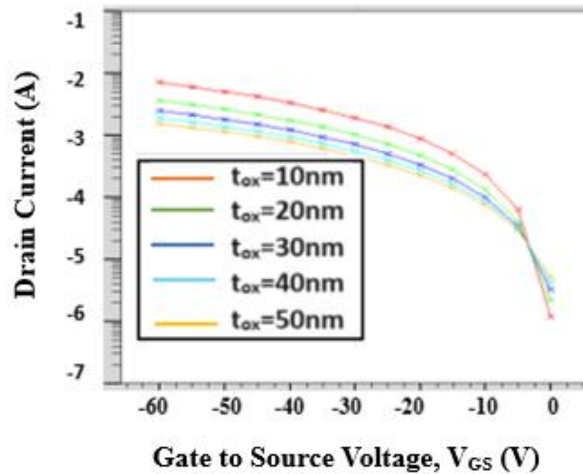

Fig 3 Transfer characteristics (log scale) with variation in dielectric thickness from 50 nm to 10 nm

a) Threshold voltage variation with dielectric thickness

As the dielectric thickness is reduced, less operating gate voltage is required and hence threshold voltage reduces.

$$\boldsymbol{V_G = QC = Q\left(\frac{\varepsilon A}{t_{ox}}\right)} \tag{3}$$

where V_G is the gate voltage, Q is the charge on the plates of capacitor, C is the capacitance per unit area, t_{ox} is the thickness of the dielectric, ε is the permittivity of the material separating the plates and A is the area of the plates of the capacitor.

As t_{ox} reduces, V_G reduces and hence V_t reduces as shown in Fig 5 [13].

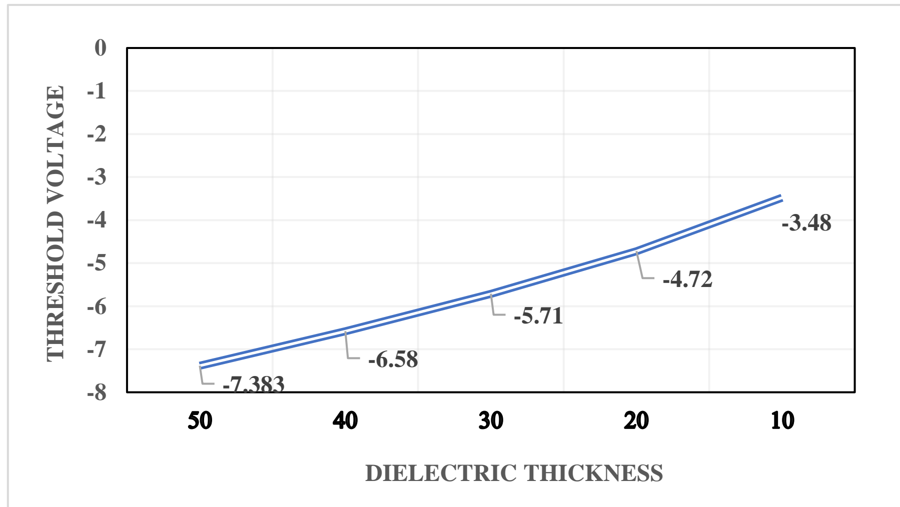

Fig. 5 Threshold voltage variation with dielectric thickness

b) Subthreshold voltage variation with dielectric thickness

As shown in Fig. 6 when dielectric thickness decreases, gate dielectric capacitance increases. So, there is a better control of channel potential and hence tunnelling current through the conduction band is significantly suppressed in the subthreshold regime that improves the subthreshold slope and hence subthreshold voltage reduces [13].

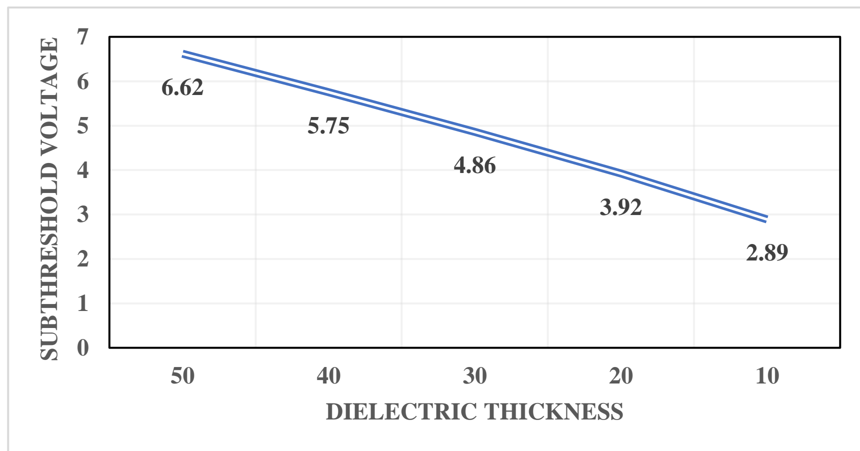

Fig. 6 Subthreshold voltage variation with dielectric thickness

c) ION/IOFF variation with dielectric thickness

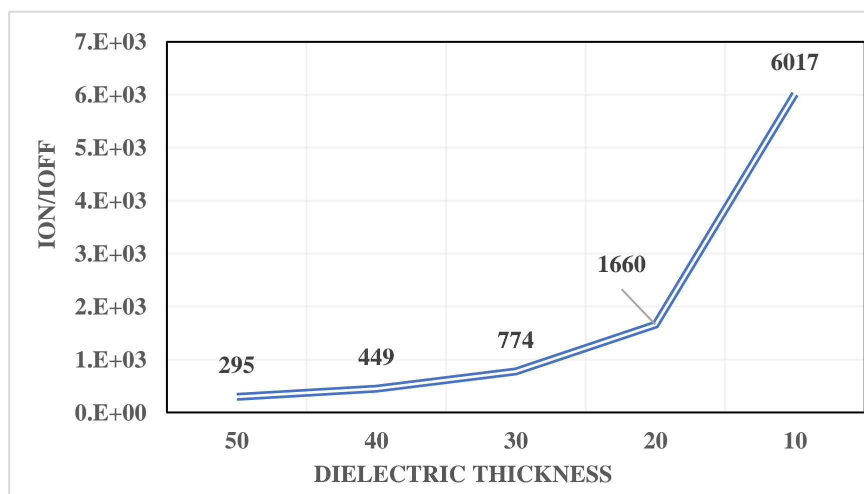

Fig. 7 I_{ON}/I_{OFF} variation with dielectric thickness

As the dielectric thickness reduces, I_{ON}/I_{OFF} improves, which is desirable as shown in Fig. 7.

d) Capacitance per unit area variation with dielectric thickness

The capacitance of a parallel plate capacitor is given as: $C = \varepsilon(A/t_{ox})$, where ε represents the permittivity of the dielectric material being used, t_{ox} is the thickness of the dielectric, A is the area of the plates of the capacitor. As t_{ox} reduces, C increases as shown in Fig. 8

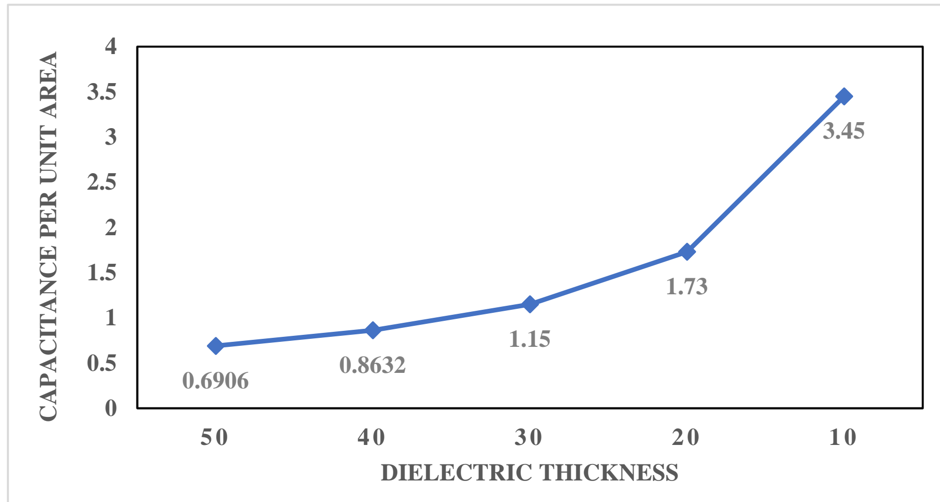

Fig. 8 Capacitance per unit area variation with dielectric thickness

e) Comparison of Mobility vs VG at various dielectric thickness of SiO_2

As the oxide thickness, tox is reduced, electric field increases which results in an increase in drain current. Due to this enhanced slope of transfer characteristics, mobility increases [14], as shown in Fig. 9

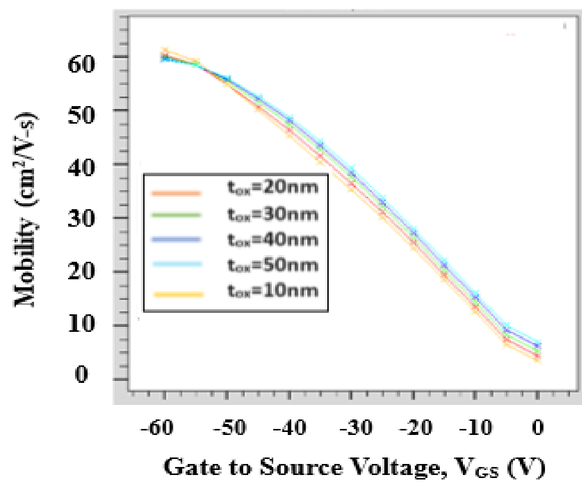

Fig 9(a) Comparison of Mobility vs V_G at various dielectric thickness of SiO_2

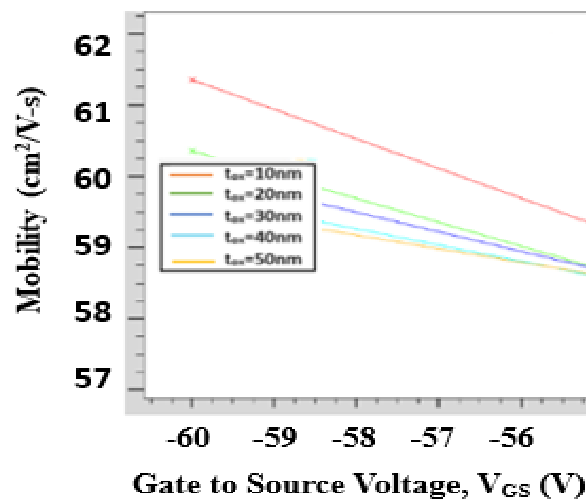

Fig 9(b) Comparison of Mobility vs V_G at various dielectric thickness of SiO2(enlarged)

f) Comparison of transconductance, g_m vs V_G with variation in thickness of dielectric

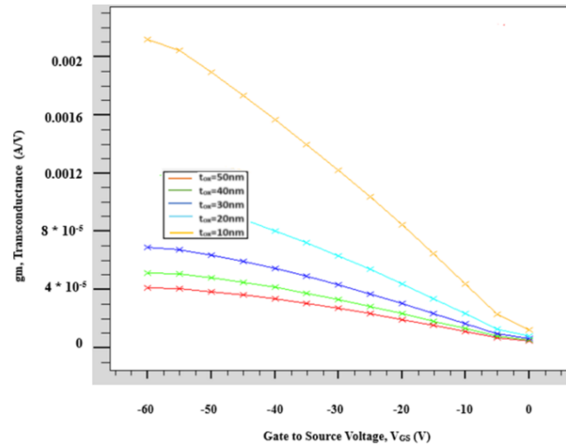

Fig. 10 Comparison of g_m vs V_G with variation in thickness of dielectric

B. Variation of dielectric constant

- *ZrO2 (Zirc onium dioxide) as dielectric*

Here, SiO_2 (dielectric constant=3.9) has been replaced by ZrO_2 (dielectric constant=29).

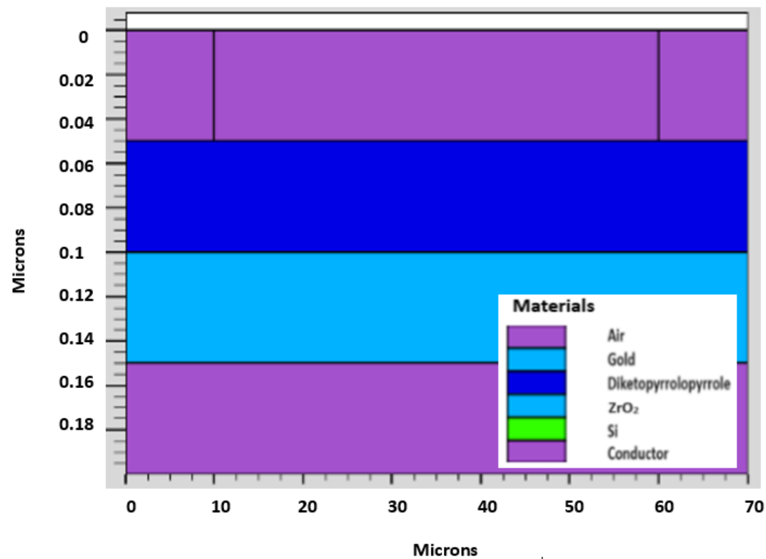

Fig 11 Structure of p-type OFET (ZrO_2 as dielectric t_{ox} = 50 nm

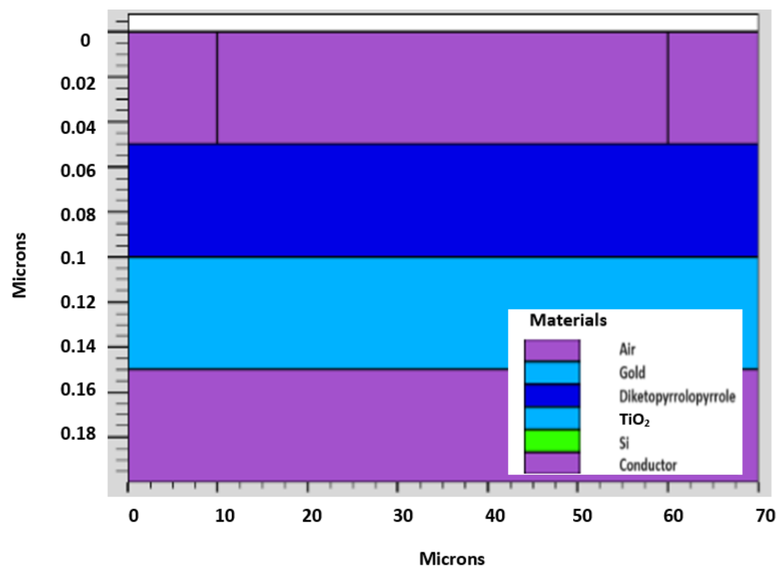

Fig 12 Structure of p-type OFET TiO_2 as dielectric with t_{ox} = 50 nm

a) Comparison in Transfer Characteristics

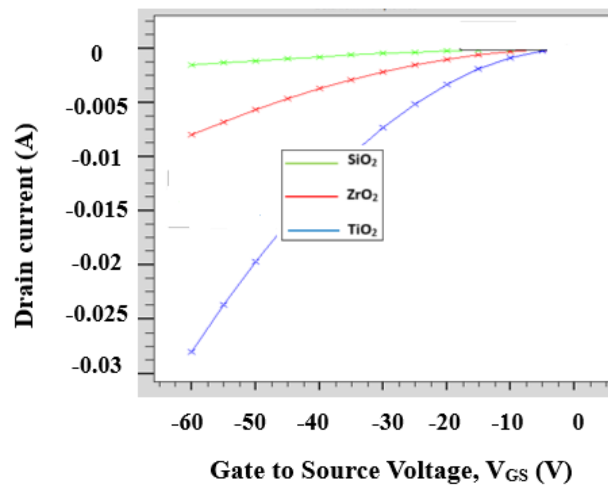

Fig. 13 Transfer characteristics linear scale with different dielectric constants (Dielectric thickness =50 nm)

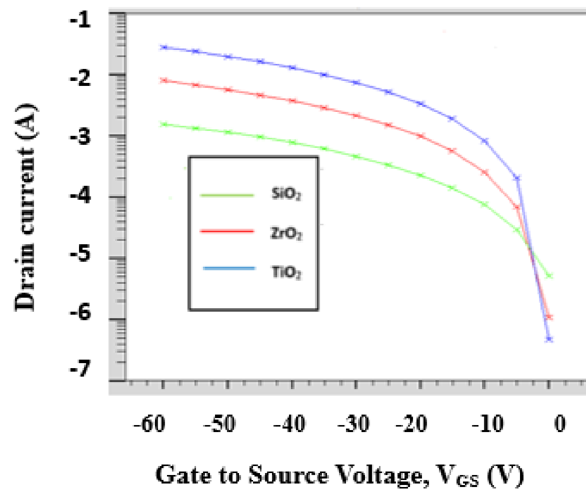

Fig. 13 Transfer characteristics (log scale) with different dielectric constants (Dielectric thickness =50 nm)

As shown in Fig. 12 and Fig.13, drain current, I_D increases with increase in dielectric constant (ε_r).

b) Variation of transconductance, gm with dielectric constant

As dielectric constant increases, gate voltage decreases and hence transconductance increases as shown in Fig. 14.

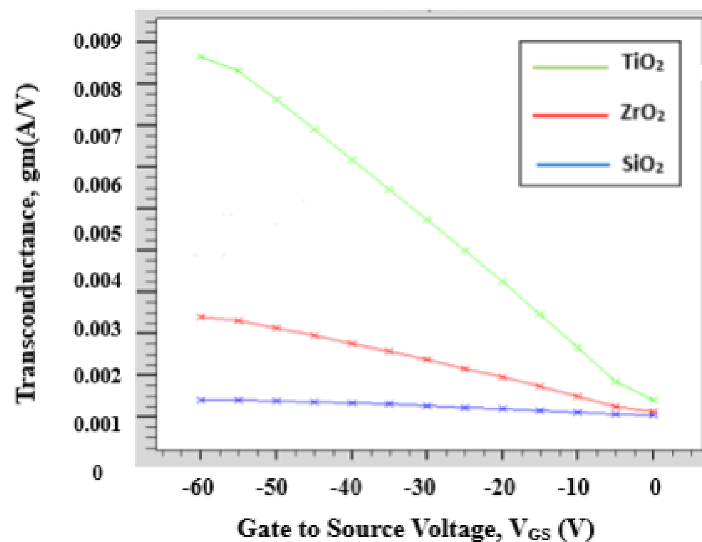

Fig. 14 Variation of g_m with dielectric constants

c) Comparison of Mobility vs VG for different dielectrics at tox = 50nm

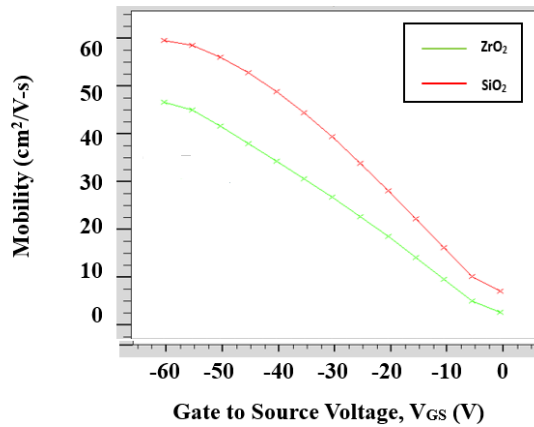

Fig. 15 Comparison of Mobility vs V_G for different dielectrics at $t_{ox} = 50$ nm

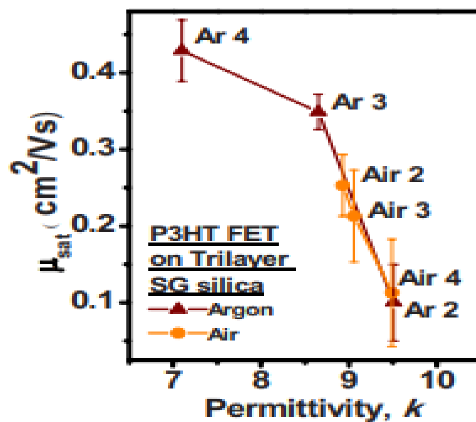

Fig. 16 Carrier saturation mobility of P3HT FETs decrease with increasing permittivity of Tri layer SG silica with different plasma treatment Ref: Article in Applied Physics Letters · July 2009 [2]

As seen in the reference above (Fig. 16), the mobility decreases with increase in the dielectric constant. Same are the results obtained in Fig. 15 when dielectric constant varies from SiO_2 (3.9) to ZrO_2 (29). This is due to the effect that the dipole field present in the higher k insulators may enhance the formation of local states in the active layer, which induces carrier localization and reduces charge carrier mobility [15].

d) Comparison tables with variation in thickness of dielectric and dielectric constant

Table III Comparison table of various parameters (with variation in thickness of dielectric (SiO_2))

BGTC	SiO_2 (50nm) K=3.9	ZrO_2 (40nm) K=29	TiO_2 (30nm) K=95
Threshold Voltage (V)	-7.383	-3.32	-2.362
Subthreshold Voltage (V/Dec)	6.62	2.76	1.895
I_{on}/I_{off}	$2.95*10^2$	$7.46*10^3$	$5.95*10^4$
Mobility (cm^2/V-s	59.55	46.58	51.4
m (A/V)	$4*10^{-5}$	0.00024	0.0009

Table IV Comparison table of various parameters (with variation in dielectric constants)

BGTC	t_{ox} (50 nm)	t_{ox} (40 nm)	t_{ox} (30 nm)	t_{ox} (20 nm)	t_{ox} (10 nm)
Threshold Voltage (V)	-7.38	-6.58	-5.71	-4.72	-3.48
Subthreshold Voltage (V/Dec)	6.62	5.75	4.86	3.92	2.89
I_{on}/I_{off}	$2.3*10^2$	$4.5*10^2$	$7.7*10^2$	$1.7*10^3$	$6*10^3$
Mobility (cm^2/V-s)	59.55	59.725	60.05	60.36	61.36
gm(A/V)	$4*10^{-5}$	$5*10^{-5}$	$7*10^{-5}$	0.0001	0.0002

IV. Conclusion

A p-type (DPP as organic semiconductor) low voltage high mobility OFET is designed by varying the thickness of dielectric (SiO_2) from 50 nm to 10 nm and by varying dielectric constant (SiO_2 (k = 3.9), ZrO_2 (k = 29), TiO_2 (k = 95)). As per the results obtained, threshold voltage is reduced from -7.383 V (t_{ox} = 50nm) to -3.48 (t_{ox} = 10nm) and subthreshold swing is reduced from 6.62 (t_{ox} = 50 nm) to 2.89 (t_{ox} = 10nm) when thickness of dielectric varies. Further, the threshold voltage is reduced from -7.383 (SiO_2) to -2.362 (TiO_2) and subthreshold swing is reduced from 6.62 (SiO_2) to 1.895 (TiO_2) when dielectric constant increases. Due to this, gate voltage of OFET is reduced. Thus, the observed mobility is increased from 59.5 (t_{ox} = 50 nm) to 61.3 (10 nm) when thickness of dielectric reduces. These low voltage high mobility OFETs have a wide application in medical sensors, radio frequency identification (RFID), wearable and stretchable technologies, etc. Now-a-days flexible OFETs are in high demand. Many flexible OFETs are being designed for displays, sensors and label technologies. Also, in future technologies dual gates or gate all around are preferred instead of single gates because of better controllability of gate over channel and also they produce more I_{ON} that leads to high mobility in OFET.

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