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Design of High-Speed Area Efficient 16-Bit KSA Implemented By Novel 6T-Hybrid XOR-Cell for ALU-Processors

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Abstract: This paper outlines the development of a 16-bit Kogge-Stone Adder (KSA) that is both rapid and effective in terms of space use. The architecture incorporates a unique 6T-Hybrid XOR-cell specifically designed for ALU processors. The study highlights the growing need for quicker arithmetic logic units (ALUs) in contemporary processors, which requires the creation of efficient adder designs. According to literature analysis, the KSA is considered a highly promising option because it outperforms ordinary addition algorithms in terms of both speed and ar ea. The methodology centers on the utilization of the KSA through the cutting-edge 6T-Hybrid XOR-cell, which improves both velocity and space effectiveness. This study presents a new 16-bit KSA that utilizes an innovative 6T-Hybrid XOR-cell. The suggested design offers superior performance in terms of rapid operation and decreases the number of transistors by 50% opposed to the standard XOR-cell. Thereby, the amount of power consumption and area get minimized compared to the existing PPA (Brent Kung, Sklansky adder, and Ladner-Fischer) designs. Typically, KSA consists of low fan-out compared to other designs, calculated by $\log_2^N$. The Performance parameters for XOR-cellpower, 16-bit KSA are **0.967**(uW), **24.512**(uW) and delay of 0.0278 **(ns)**, **30.154** (ns),which inference that the power and delay of the proposed designs improved by 50% compared to the conventional PPA- designs. The simulation results were collected from the Cadence virtuoso tool of45nm technology with a supply voltage of (Vdd) 0.8V at a frequency of 1GHz. Hence, the proposed 16-bit KSA implemented by 6T-Hybrid XOR-Cell can be effectively utilized for high-speed battery operation and edge-device manufacturing, which is used for IoT applications.

Keywords: Parallel Prefix Adder (PPA), Kogge-Stone Adder (KSA), Carry-generate (Gi), Carry-propagate(Pi), Pull down Network(PDN), Pull up Network(PUN),6T- Hybrid XOR-cell, CMOS-Logic.

I.INTRODUCTION

Digital Signal Processors (DSP) and application-specific integrated circuits (ASICs) rely on the efficient implementation of the arithmetic unit (AU) [1-3]. Adder is the major core and fundamental building block to perform any operations such as addition, multiplication, subtraction, and division. Based on the power consumption, area, transistor count, and interconnections, adder structures can be classified into two approaches (i) the Classical design approach, and (ii) the Hybrid design approach [1], [4], [5]. In the first approach, the adder circuit is designed based on the principle of Pull up Network (PUN), and Pull down Network (PDN). Typically, referred to as complementary metal oxide semiconductor logic (CMOS) [6], [8], [9-10]. Addition is a vital mathematical function performed in digital circuitry. ALU, or Arithmetic Logic Unit, is a component found in different kinds of electronics such as cell phones, laptops, and tablet PCs. These gadgets have chips with processors [23]. As a component of ALU, additional circuits play a crucial role in computations for floating point calculations, generating memory addresses, doing index activities, and similar tasks in the "Digital Signal Processor" (DSP). The DSP is liable for processing large amounts of visual and audio information at extremely high speeds. Therefore, these necessitate intricate adder logic.

In CMOS-Logic, all P-MOS transistors were connected to the supply voltage (Vdd) which encourages pulling the output voltage equal to the supply voltage, and all NMOS transistors are connected to GND-potential which encourages pulling the output voltage to zero-volts [4][6-7]. It has a feature of robustness against voltage scaling and produces full swing voltage [8]. The large transistor count (28T) and interconnections between nodes power consumption, and area-occupied in the chip are more, which causes to enhancing the parasitic capacitance, and short-circuit power [15], [17]. The bottleneck in this design is to reduce the lifetime of the chip. On the other hand, Hybrid full-adder design has the best feature in terms of transistor count (16T) and interconnections [15-17]. Thus, improves the full swing voltage and driving capability. The term 'Hybrid' refers to the implementation of more than one logic to produce full swing with low latency compared to counterpart adder structures [13]. Hybrid adder design has the advantage of low power consumption, high speed, less transistor counts and low-area [14]. Hence, these are highly preferred for high-speed portable devices such as cellular phones, gadgets, and IoT-based based on the long battery life [13-16], [18]. A digitized circuit's adder cells symbolize the extra value of a single bit. There are actually two different types of modifications: the combination performed by 2 bits is referred to as a half addition, while the adding that involves all three bits is called a complete adder. The last bit represents the carrying signal that is transmitted to the subsequent step of a complete adder. The complete adder is chosen as a typical cell to run complex adder architectures in this study. Our primary emphasis was on the static style due to its appealing efficiency compared to other logic types, characterized by low variable electrical consumption and high distortion margin [24, 25]. The chosen adders in the KSA are of particular significance due to their 16-bit phrase capacity. NIST [26, 27, 28] states that an encryption key of at least 110 bits is necessary to withstand violent assaults.

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Cryptography and by the KSA [29, 30]. As a consequence, these functions are meticulously chosen and merged to generate robust encrypted text [31, 32]. The secret key employs the KSA to produce round keys that are necessary to perform the decryption procedure in the symmetrical block cipher. The round keys are applied using a direct XOR operation with the encryption state, which serves to obscure the starting point and output of a certain round.

Based on the speed and area, adder designs have been classified into two type's i.e. serial adder and parallel adder. In serial adders (RCA, carry skip adder, carry save adder, and array multipliers) [4-6], [9]. Thus, the worst-case delay and power consumption in the chip cause to increase in the glitches [10-12]. On the other hand, parallel adders (KSA, Brent-Kung, Sklansky, Han-Carlson) have an excellent feature high-speed and low fan-out [1-3],[6],[9]. Whicharedevelopedbasedonthefundamentalprincipleofthecarry-look-aheadadder (CLA)[3],[7],[9-10]. In parallel prefix adder (PPA), the computation of the final explored, pre-processing stage, computation stage, and post- processing stage [4] [6].In the first stage of the PPA, carry-generate(Gi)and carry-propagate (Pi) are outputs which were produced based on the 'AND' gate logic and 'XOR'-gate logic respectively,referredas'RED-cell'[6- 8],[10],[12]. In the second stage of the PPA, calculating the carry signal in parallelly and transferring it to the next stage, which consists of two'AND'gates and 'OR' gate logic, referred to as 'Gray- cell' or Black cell [7],[9],[10].

In the last stage of the PPA process, the major function is to evaluate the total sum by 'XOR'- logic. Thus, this state is called the post-processing stage [6], [8], [10]. The function of buffer cells in PPA is to balance the intermediate nodes for impedance matching. As a result, minimizes the power glitches in the circuit and maintains high speed [4],[11],[12].

This study enhances the discipline of electronic circuit design by presenting a high-speed and space-efficient KSA that is executed utilizing a unique 6T-Hybrid XOR-cell. The suggested XOR-cell surpasses existing designs by obtaining the smallest delayed energy use and PDP. These enhancements enable quicker calculations and lower energy consumption, rendering the architecture ideal for inclusion into ALU-Processors, hence improving its overall performance as well as efficiency.

Dinesh Kumar et al., (2019)[33] created numerous designs to enhance processing in areas such as signal processing, information channel interactions, control, and surveillance applications. This design minimizes power consumption, reduces area requirements, and minimizes propagation delay. The study showed a 43% reduction in energy use, a 20.9% decrease in power delay product, and a 46% decrease in delay in propagation compared to the current way of studying. **Maddula et al., (2014)** [34] executed multiple architectures of sixteen-bit adders, including the "Kogge Stone Adder" (KSA), in 65nm CMOS semiconductors. The efficiency of these addition algorithms was studied in terms of authority, working rate, and acceleration at close to threshold functioning regions. **Shirol et al.,(2020**) [35]proposed ALU design incorporated dual reversible and irreversible logic gates to minimize dissolution, switching strength, and latency. The suggested design was described as a Hybrid ALU design. Adder designs were used to sum up the partial results in Vedic multipliers, resulting in a reduced delay when digital multiplication was employed.

Manchala et al., (2022) [36] incorporated the concept of a 6T-XOR-cell and a "1-bit Hybrid Full adder" (HFA) in a "Parallel Prefix Adder" (PPA) to enable fast speed computation. The power was enhanced by 53%, while the PDP (aj) experienced a 28% improvement, resulting in a value of 41.08. **Garima Thakur et al., (2020) [37]** discussed many types of adders, including "Ripple-carry (RC)" and KSA. The adder design supported bit-lengths of 16, 32, and 64, and exhibited delays of 9.248ns, 10.231ns, and 7.258ns, accordingly. **Shrinidhi et al., (2022)** [38] developed the 16-bit linear convolution structure by introducing a series of 4-bit "reversible Vedic multipliers" (RVMs) architecture, along with 8-bit reversible KSAs. The investigation resulted in a roughly 50% decrease in the quantity of "clock cycles" (CCs) and "constant inputs" (CIs).

Katreepalli et al., (2017) [39] introduced a novel CSA architecture that incorporated the "Manchester carry chain" (MCC) in a multioutput dominoes CMOS logic design. The architectural layout of the CSA utilized a unique hierarchical method that incorporated MCC blocks. The validity of the suggested layout was confirmed through the execution of 16 and 32-bit addition circuits using a typical 45nm CMOS manufacturing technology. The outcomes of simulations demonstrated that the suggested architecture offered dual benefits in terms of PDP and mechanical expense. **Shylashreee et al., (2019**) [40] presented a high-speed 8-bit ALU that utilized 18 nm Fin FET technologies. The ALU consisted of high-speed computational units, including the KSA and Dada multiplier, along with fundamental logic gates. The suggested design had a transistor amount of 5297, a power usage of 218 µW, and an ultimate delay of 166.9 ps. **Sridhar et al., (2014) and** Thakur**et al., (2018)**[41,42]The concept that was suggested involved a 16-bit sparsely tree "Rapid Single Flux Quantum" (RSFQ) architecture. The KSA and CLA methodologies were combined. In the past, N-bit adders like "Ripple Carry Adders" (RCA) were commonly used. The research used the combined results to analyze performance metrics, including the number of "Look-Up Tables" (LUTs) and delay. All of these adders were

assessed based on their size and latency values.

The following paper organizes, section-II, for the working principle of various types of PPA designs and their need for high-speed devices. Section-III- describes the methodology of 16-bit KSA implemented by 6T- Hybrid XOR-cell and its advantage, and necessity for low-power battery-operated edge devices. Section IV explores the result with Tables. Section V explains of conclusion with validation by existing literature its importance for the design of high-speed operated portable devices such as cellular phones, gadgets, and battery devices.

II Existing16-bitKSA-PPAdesign

Parallel prefix-adder (PPA) designs were classified into four types based on performance parameters such as speed, area, fan-out, and driving capability. Among all PPA's, KSA has a high-speed and low-fan out though the chip area is high. Thus KSA is highly preferred for the manufacturing of high-speed computational device applications [1-2].

2.1 16-bitKSA-design

KSA is the fastest among all PPA structures which have low fan-out, a limit of 2 at each stage, and functions based on the "recursive doubling technique" which means the "divide and conquer principle"[5-7],[9]. Whereas, in terms of speed and working process it has been divided into two equal composite sub section s whose estimation can be performed concurrently with stage of N [5],[7],[11].The disadvantage encountered in this design is high number of interconnections in computation state compared to other PPAs [6],[9],[8].

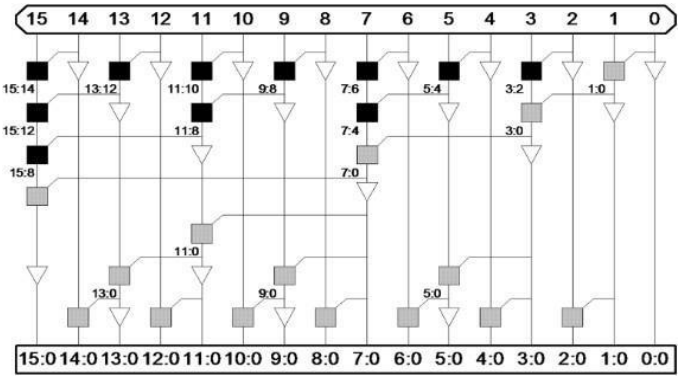


Fig.1:16-bitKSA-design [5]

2.2 16-bit Brent-King Adder

BKAisdevelopedbyBrent-Kungin1982.Which has an attribute of fewer computational nodes, maximal data path, and less wiring congestion compared to KSA [5], [8], [10].Thus BKA occupies less space intermesh of area and utilization of cell- structures during the delay calculation process, intermediate carrier process is introduced in between the computational stages which cause to increase the latency [5]. The delay of the BKA can be calculated by[(2) (n)-2-log n] and the number of computational nodes can be measured by 2[2(n)-2-log n] shown in fig.2. To improve the performance and overcome thebottlenecks associated in BKA, Sklansky has been introduced [5].

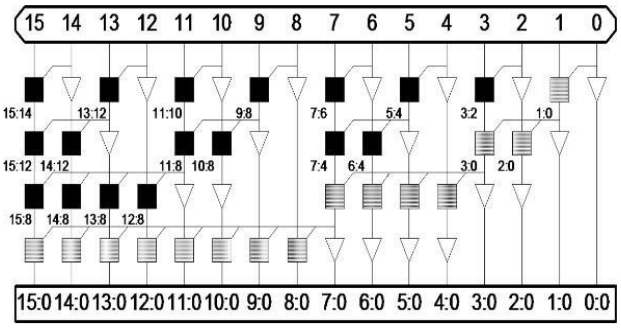


Fig.2:16-bit BKA-design [6]

2.3 16 bit Sklansky Adder

Whereas, in terms of speed and working process it has been divided into two equal composite sub section s whose estimation can be performed concurrently with a stage of $\log N$.[5],[7],[11].The disadvantage encountered in this design is high number of interconnections in computation state compared to other PPAs [6],[9][8]. The fig.3 shows the schematic of the16-bitsklansky adder which also works based on the principle of "dividend conquer" and was developed by Sklansky in 1960 [5], [12]. It divides the PPA-structure into two equal sub- sections which segregates overall bits into even-bits and odd-bits respectively [5], [9]. Later, it recombines

and develops the final carry in the post-processing stage. The fan-out of the Sklansky adder increases significantly from the input to the output along the critical path which may cause degradation of the performance when connected in a large number of bits. So, in terms of the latency and driving-capability of the Sklansky adder has been modified and introduced HCA design [5], [10],[12].

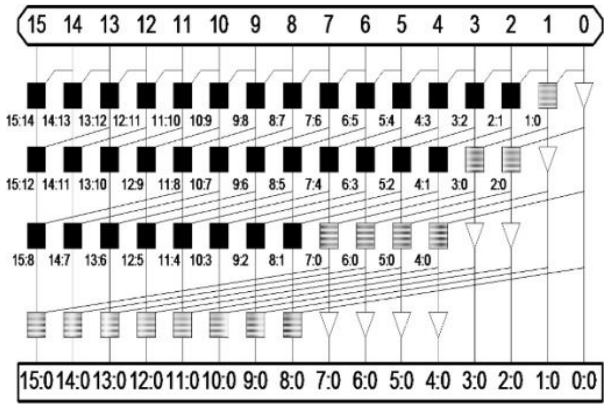


Fig.3:16-bit Skalansky-design [9]

2.4 16-bit Han-Carlson

Developed Carlson's works based on the combinations of KSA and BKA-structures which implies BKA-tree is implemented in first-stage and the KSA-tree is implemented lateral stage respectively [5],[6],[7]. HCA design divides the carry-merge computation into even bits to produce Group-Generate/Group- propagates that are used for the calculation of the final carry [8], [9]. Later, both even bits and add-bits are recombined to produce final-carry bits. Thereby, HCA has a total of $N + 1$stages to generate the final carry. The advantage of HCA is fewer inter connection nodes and less area-complexity. Thus, the performance parameters interms of power consumption, regardless. The bottle neck encountered is due to hybrid structure (i.e KSA & BKA) impedance mismatching arises, which causes the intermediate nodes. As a result, increases the latency [5], [10], [12].

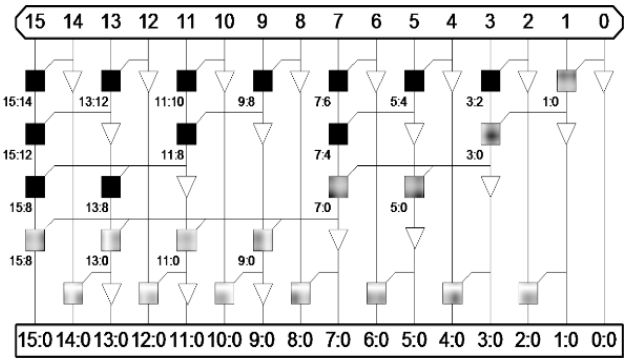


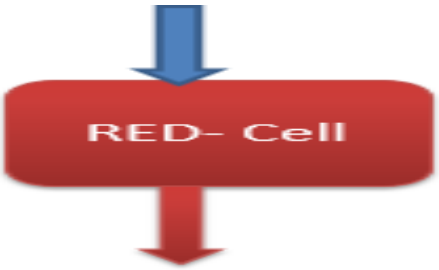
Fig 4:16-bit Hancarlson design [9]

III METHODOLOGY

The development methodology for the speeds, area-efficient 16-bit KSA incorporates the novel 6T-Hybrid XOR-cell, which plays a crucial role in improving efficiency. The 6T-Hybrid XOR-cell utilizes six transistors in order to effectively minimize both latency and electrical consumption. The KSA design consists of three main cell types: the yellow cell, the red cell, and the buffer cell. The cell in red is accountable for producing a portion of the outputs; the yellow cell manages the transmission of carry messages, and the buffering cell guarantees signal integrity and time coordination. The utilization of the 6T-Hybrid XOR-cell in this well-organized and effective design technique leads to a highly tuned KSA that is well-suited for ALU-Processors. This improved KSA achieves exceptional rapidity and effectiveness in terms of area utilization.

3.1 Operation of 6THybridXOR-cell design: The proposed 6T Hybrid XOR-cell has been developed based on the principle of CMOS-Inverter, CMOS-PTL-logic, and CMOS-level-restorer logic, which generates the full swing at the output node and also functioned at high-frequencies. Particularly, in terms of transistor count reduces by 50% compared to the conventional XOR-gate. Thus, the area occupied by the chip gets miniaturized. The major advantage is due to the absence of cross-coupled connections at the critical path, parasitic capacitance and short- circuit's power generated by the chip is less. The literature survey in Table.1 explores the performance parameters in terms of Power, delay, and PDP

3.2 RED-cell: In the PPA-KSA-structure, the function of RED-cell is to produce the generate (Gi), and propagate (Pi) based on the 'AND-Gate' and proposed 6T-XOR-gate logics respectively. The advantage of the proposed 16-bit KSA i s less transistor count and low-area. Hence, the power consumption is minimized. The transistor-level schematic of the 6T-Hybrid-XOR-cell is shown in Fig. 5. Due to absence of cross-coupled connections, the amount of leakage current gets



(a)

Fig.5: (a) Red-cell, (b) 6T-Hybrid XOR-cell schematic, (c) Gate-level

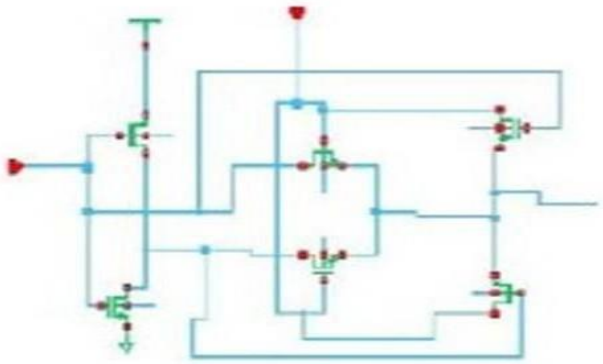


Fig.5: (a) Red-cell, (b) 6T-Hybrid XOR-cell schematic, (c) Gate-level

3.3 Yellow-cell: The function of Black or Yellow-cell is to carry -forwarding the propagate (pi) and generate (Gi) to the next stages. The gate level schematic of Black-cell as shown in fig.6 consists of two-AND gates and OR-gate-logics.

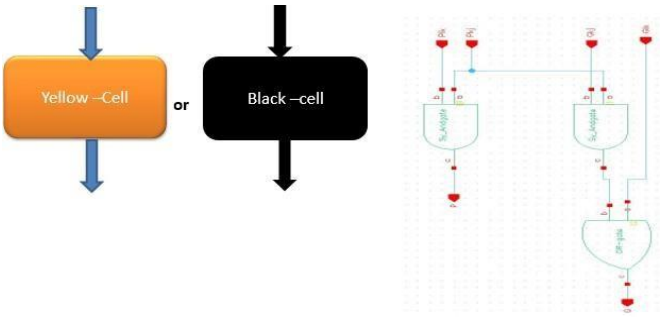


Fig.6: Yellow-cell, Gate-level-schematic

3.4 Buffer-cell: The function of the buffer cell for PPA-structure is to balance the impedance which arises due to the implementation of hybrid designs (i.e. KSA and BKA). The Fig. the transistor levels schematic depicts in 7. It has two inverters connected by cascade

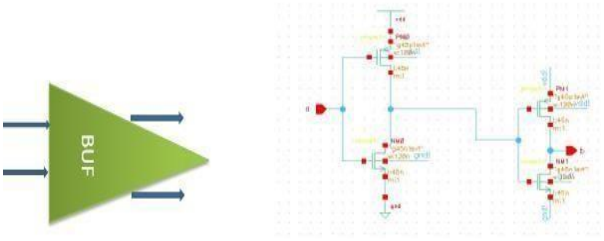


Fig 7: Buffer-cell, Transistor level schematic

IV RESULTS

4.1 Dynamic Power consumption

The study focuses on minimizing variable electrical usage by optimizing changing activity and reducing the impedance of the transistors. The revised cell design guarantees that the power consumed during signal transitions is considerably reduced, hence enhancing the overall energy efficiency of the ALU-Processors. Static CMOS adders usually require power when they charge their internal capacitance, which encompasses wire capacitance and gate capacitance resulting from supply and drainage. The total power over one cycle is given by the product of the capacitance (C), the VDD and it is transferred from the VDD to the earth. The mean power level was determined using the following equation

$$P_{avg} = {}^{C_{total} \times VDD^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots \textbf{(1)}$$

Power Delay Product (PDP): PDP refers to the amount of energy consumed during each switching operation. The term refers to the result of multiplying the amount of power used with the time it takes for a signal to travel from the input to the output. In this study, the interruption refers to the amount of time required for each adder's critical route. It has been utilized as an Indicator that is associated with the energy consumption of logic gates [43].

A comparative examination of different XOR circuits, assessing their efficacy in terms of power, delay, and PDP. The evaluated circuits comprise designs by Goel, Chang, Aguirre, Valshani, Naseri, and a recently suggested XOR circuit. The suggested XOR circuit exhibits superior performance compared to the other circuits, with the lowest latency of 0.0278 ns, minimal power usage of 0.967 µW, with the smallest PDP of 18.09 atto-joules. The findings emphasize the improved economy and reliability of the suggested design, which makes it extremely appropriate for applications that need high speed and power sensitivity.

Table.1: The comparison of the proposed 6T-Hybrid-XOR-cell with existing literature intermsof power (µw), Delay (ns), and PDP (joules).

XOR CIRCUITS	Delay (ns)	Power (µW)	PDP (10-18) Joules
	XOR		
Goel	0.0381	1.894	71.44
Chang	0.0328	1.518	48.92
Valshani	0.0657	2.187	142.6
Aguirre	0.0945	1.782	159.7
Naseri	0.0367	1.058	37.9
Proposed-XOR	0.0278	0.967	18.09

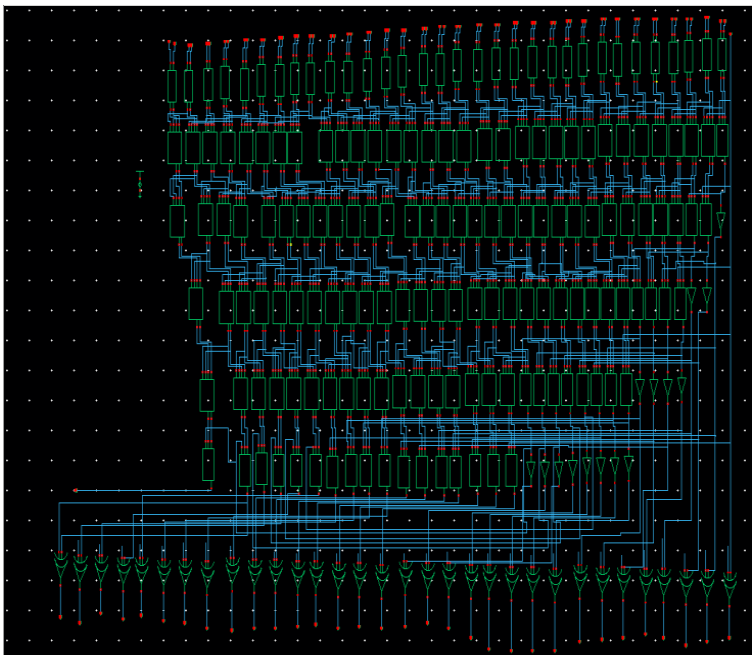


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Fig.8: 16-bit Proposed KSA

The 16-bit KSA design was implemented in a cadence-virtuoso tool of 45nm with 0.8V as the supply voltage (Vdd). This structure is explained by three processing steps with individual cell structures as shown Fig 8 depicts the arrangement of the 16-bit Proposed KSA that includes the innovative 6T-Hybrid XOR-cell. This schematic highlights the intricate connections and positioning of components in the KSA circuit, highlighting a small and effective design. The recommended KSA's organized architecture is designed to maximize performance and area efficiency, making it highly suitable for insertion into ALUs within CPUs. The utilization of the 6T-Hybrid XOR-cell in the KSA design demonstrates that the suggested system has a reduced transistor count, resulting in fast calculation and efficient use of space. This addresses important performance measures for contemporary ALU-Processors.

The following timing diagrams show the output collected at the different stages and is noted as shown in Fig. 9

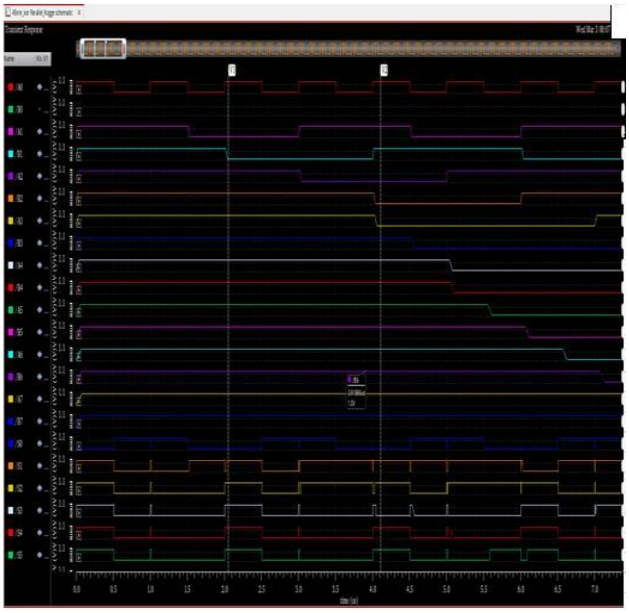

Fig. 9(a):16- bit KSA-Timing diagram

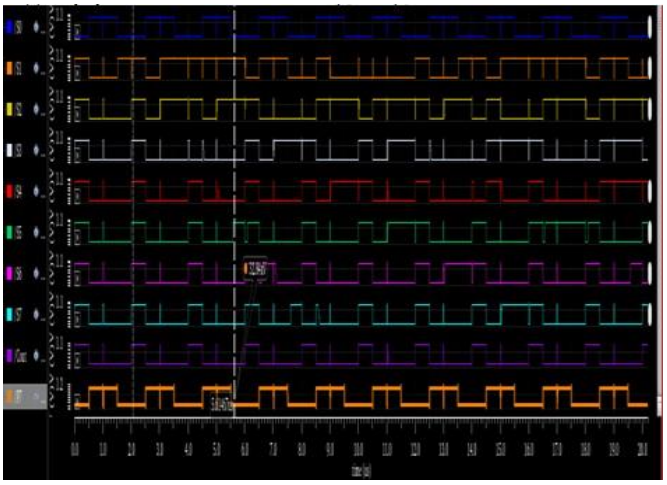

Fig.9 (b):16-bitKSA-Timing diagram

The timing diagrams of the 16-bit KSA constructed with the innovative 6T-Hybrid XOR-cell are shown in Figures 9(a) and 9(b). The graphs depict the signal's changeover and delayed propagation of several inputs and outputs across time. Each colored line represents a unique signal. The constant and smooth changes provide evidence of the KSA's high-speed reliability and effectiveness. The timing diagrams, when compared to Figure 8 which illustrates the physical arrangement of the 16-bit Proposed KSA, confirm the effectiveness of the design by showcasing its capability to sustain consistent voltage levels and perform precise logical operations shown in table.2. This further strengthens the advantages of the design. The Proposed-XOR circuit demonstrates exceptional efficiency and performance, characterized by its low latency, power use, and PDP) in comparison to alternative designs. This makes it extremely ideal for ALU processors.

Table 2: performance parameters of Power (uW) and delay (ns)

SL. NO	Types	Delay (ns)	Power (u W)
1	Sklansky Adder	56.785	34.165
2	Brent-Kung Adder	40.782	33.781
3	Ladner-Fischer Adder	36.244	37.142
4	Proposed Kogge-Stone	24.512	30.154

Table 2: describes the performance parameters of Power (uW) and delay (ns) with existing PPA designs, which rely on the proposed design have low power consumption, and improve the delay which were plotted and shown in Fig. 10

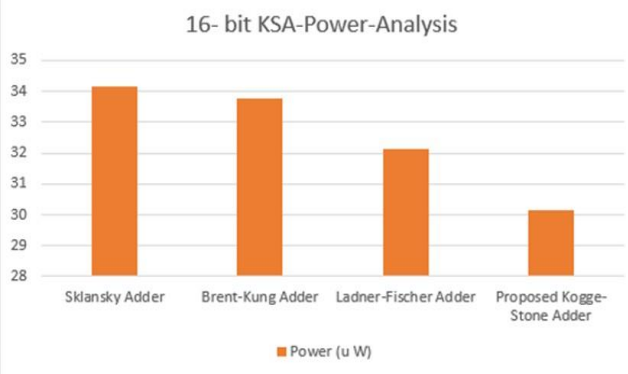

Fig. 10 (a): Power Plot

Figure 10 (a) illustrates a comparison of energy consumption between four distinct adder architectures and the developed KSA. The measurement of power usage is expressed in µW. The chart demonstrates that the KSA utilizes

considerably fewer resources or power (about 28 µW) in comparison to the other adders. The "Sklansky Adder" and "Brent-Kung Adder" both consume around 33 µW, while the "Ladner-Fischer Adder" consumes about 31 µW. This demonstrates the exceptional thermal performance of the suggested KSA, resulting in a more efficient solution for ALU-Processors in terms of power consumption.

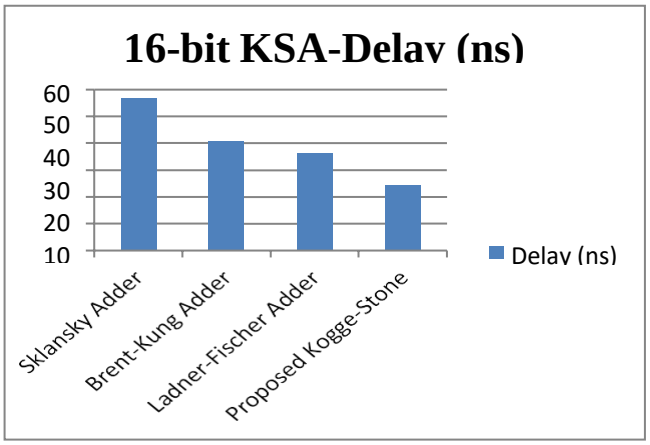

Fig. 10 (b): Delay Plot

Figure 10 (b) depicts the delay and presents a comparison of several adders using a 16-bit K.S.A. delay plot. The duration is quantified in ns. The chart demonstrates that the recommended KSA has a much lower delay (about 24 ns) in comparison to the other adders. Both figures 10 (a) and (b) demonstrate that KSA utilizes a 16-bit design, resulting in a reduction in the number of transistors and a 50% decrease in power intake, while also achieving the shortest delay relative to other adders.

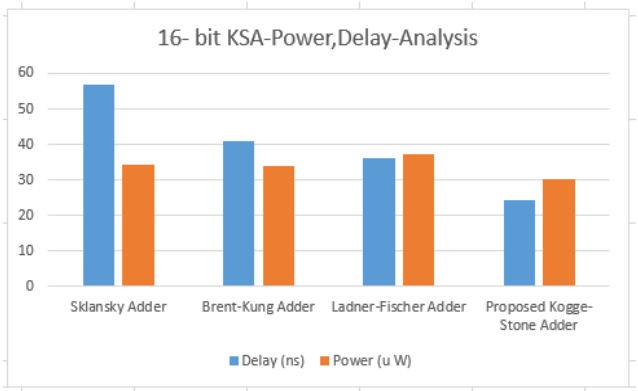

Fig.10(c):16-bitKSA Power, Delay Analysis plot

Figure 10 (c) is a bar graph illustrating the mean power delayed comparison of four distinct adders. The x-axis of the chart is labeled "Adder" and represents the four distinct types of adders. The y-axis, denoted as "Delay (ns)", represents the standard power delay. The graph illustrates that KSA exhibits the lowest delay in comparison to the other three adders. Ultimately, the graph indicates that the KSA exhibits the highest level of efficiency among all four adders when considering the mean power delay. The result shows that this design incorporates a small 6T-Hybrid XOR-cell to minimize the additional space required, while still achieving a rapid speed. The KSA effectively produces a 16-bit sequence of keys, which is essential for cryptography-related tasks, guaranteeing the best possible efficiency on microprocessors based on ALUs with just a small amount of hardware required.

V DISCUSSION AND CONCLUSION

The study presents various notable benefits compared to prior studies. The inclusion of the 6T-Hybrid XOR-cell greatly improves the performance and area utilization of the adder when compared to conventional XOR constructions. This innovative cell optimizes the number of transistors and areas while improving performance, making it especially appropriate for integration within ALU processors wherever economy and performance are crucial considerations. In addition, the KSA structure naturally decreases critical path delays by utilizing its parallel-prefix order, hence improving speeds. The KSA with the 6T-Hybrid XOR-cell outperforms traditional adders such as RCA or CLA in

terms of power-delay ratio metrics, showcasing its excellence in high-performance computing applications. Moreover, the design's scalability enables effortless incorporation into larger adders with greater bit-widths, guaranteeing interoperability with advancing microprocessor architectures. In summary, this work highlights the significance of creative cell design and choice of architecture in enhancing the abilities of ALU processors, providing a convincing solution for upcoming computing needs.

In this paper, various types of 16-bit PPA- structures i.e. KSA, Brent-King, Han-Carlson, and Sklansky were validated with proposed 16-bit KSA implemented by novel 6T-Hybrid XOR-cell. The proposed KSA is simulated in the Cadence Virtuoso tool with a frequency of 1-GHz with a supply voltage of (Vdd) at 0.8V. The inference in terms of power is 24.512 (uW) delay 30.154 (ns), which improves by 50% in terms of transistor count compared to conventional PPA structures and XOR-cell designs, which produce full swing with tremendous speed. Hence, the area of integrated chip size gets reduced. Due absence of cross-coupled connections, the amount of parasitic capacitance and short-circuit power developed by the chip gets minimized. Hence it concludes that the proposed 16-bit KSA using a 6T-Hybrid XOR-cell structure is best suited for low-power high-speed edge devices controlled by a battery. Thus, the circuit is best suited for high-speed battery-operated smart chip in IoT applications.

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