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Design and Simulation of Fault Tolerant 3- Φ Multilevel Inverter Topologies with Reduced Components: A Review

Abstract: - Three-phase multiphase inverters are widely used in power distribution, motor, photovoltaic systems and other industries. In this article, STM32F407 will be used to control the multistage inverter. Compared with the digital signal processor F28335 (DSP), STM32F407 can be expanded to 56 ePWM and arithmetic operations. Thinking in other context, the number of ePWMs and the computational logic capacity of the DSP are inadequate. Also, the STM32F407 is cheaper than the DSP while retaining inverter features. Therefore, this new concept aims to pave the way for many applications and business opportunities. To prove this, the test results of STM32F407 control and DSP control card were compared.

Keywords: Power Distribution, Digital Signal Processing, Photovoltaic System, Multilevel Inverters, Simulation Results, Control Method, Processing Speed, Fuel Cell, Load Current, Dc-link Voltage, Voltage Polarity, Hybrid Electric Vehicles.

I. INTRODUCTION

while one of the most outstanding and inexpensive solutions for converting DC into AC power in various power ranges – including low, medium and high power, multilevel inverters have experienced widespread use for a range of applications. These systems are remarkably versatile, with applications including a wide array of tasks such as; power quality improvement, grid power management, adjustable speed drive, induction heating, photovoltaic power system integration, reactive power compensation, high-power AC motor drive, uninterruptable power supplies, and both high-voltage DC transmission (HVDC) and flexible AC transmissions system (FACTS), to static var compensator, and more recently, active filtering is used in powering the electrical and hybrid electric vehicles (EHVs). AS the modernization in technology of control increases, particularly the emergence of the high-power semiconductor devices, have propelled multilevel inverter technology forward significantly. Traditionally, the multilevel inverter was finally realized after a combination of power electronics/components technology and control theory had reached a point where it could be implemented. This inventive solution borrows heavily from both concepts of equalizing/donut insertions and dc-link capacitors to create resonance fatality. Of particular note is its use in a unique hybrid series/parallel transformer strategy.

Competently we are witnessing the fast development in technology; mainly advent of new high-power semiconductor devices has opened the door for the development of MLIs. Traditionally, MLIs are developed using semiconductor devices and diodes to provide controlled ac power. However, use of high number of power

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semiconductor devices, gate drivers and diodes increases sophistication of the MLI topologies so that the probability of the occurrence of faults in MLI topologies is significant.

II. LITERATURE REVIEW

The author in this paper proposes a novel three-phase four-leg-based split4 source inverter (SSI) topology with reduced instantaneous common-mode (CM) voltage is proposed. The proposed topology employs a single Boolean logic gate for its fourth leg based on imaginary switching times (ISTs) utilizing discontinuous pulse width modulation (DPWM) strategy.

The researcher proposed the use of STM32F407 to manage the multilevel inverter. Compared to Digital Signal Processors F28335 (DSP), the STM32F407 can extend up to 56 ePWM as well as compute logic function [2].

The multilevel inverters (MLIs) are able to present a high resolution voltage waveform as output by integrating the ac output waveform from plentiful dc input sources. This high-resolution waveform can only be achieved by enforcing suitable switching pulse pattern. The superiority of voltage waveform of the load is directly influenced by the number of voltage levels as provided by the output voltage levels used. With the increased number of steps, the waveform generated at the output approaches more like a sinusoidal shape and its harmonic profile improves.

Several traditional MLIs serving diverse range of voltage and power levels can be found in the literature [4], [5]. The converter 6 of Figure 1 does not possess the line-frequency voltage components on the capacitor voltages, unlike conventional structures [6]. It provides low voltage stress on the power switching devices than the peak value of the output 1 voltage, small amount of Total Harmonic Distortion (THD), improved electromagnetic compatibility (EMC), little dv/dt stress on the load and hence minor electromagnetic interference (EMI) and reduced switching losses with higher converter efficiency. A variety of MLIs is being into existence and the extensively used and commercialized ones are: neutral point clamped (NPC), flying capacitor (FC), cascaded H-bridge (CHB) [3].

The author's give a methodology that is useful for finding Fault tolerance which is gaining increasing importance in applications such as power generation in photovoltaic cell, electric drives, electric cars etc. In MLIs the fault tolerance is achieved by including manyfold switching states for getting the output voltage that is fed by same source. The switching states are popularly known as 'redundant states'. Obviously, the availability of redundant states is due to more number of switching devices. As the number of switches is reduced to obtain RSC-MLIs, the redundant states are more likely to decrease. In fact, for some MLIs consisting of asymmetrical source configurations, the redundant states are fully eliminated [4].

The researcher observed in the proposed model that MLIs suffers from the limitations of more number of dc link capacitors and flying capacitors. This extremely degrades the reliability of the converter system [5].

The author proposed model anticipated that in order to impart fault tolerance to flying capacitors MLI, a solution is presented by connecting an SCR in parallel with each of the main IGBTs [6].

The author identifies the MLI topology that is capable to create both positive and negative levels and broadly reduces the fraction count but it does not bear at all open switch failure [7].

The suggested model of the author is that 'classical' or 'conventional' topologies are more suitable for getting a feel that they are productive at the task in hand [1]. For a better quality of multilevel waveform we have to increase the number of levels which in turn leads to increased number of switching elements. [2] In those 'conventional' topologies. If we increase the number of level to two it will increase the lifespan of one converter. This increase in levels will be in a position to inculcate low voltage across the switches and will also lower the frequency which results in lowered dv/dt stress [3]. Among others challenges, one major challenge is the increase in the number of semiconductor devices [8].

Fault tolerance typically means "maintain a system's function in the event of a failure" [4]. This concept is gaining importance by the day, if not hour, due to applications including, say, generation of power using the principle of Photovoltaic, electric drives, electric cars and what have you. Fault tolerance in 13 MLIs is supported by the fact that they provide multiple switching 1 states for an overall state i.e. 1 state.

The researcher proposed model MLIs have a superior offer in terms of likelihood of fault-tolerant (FT) procedure [9].

Our main aim is minimizing the element count for advanced amount of levels. This class of MLIs is referred to as 'reduced switch count multilevel inverters' (RSC-MLIs) [10]. A revise reproduction of faults has been projected in this paper of them. The most important faults for switching devices are: open circuit faults and short circuit faults. Short circuit 6 faults occur due to the consequence of an overvoltage, a very high temperature, a 2 inaccurate gate voltage, an avalanche stress or a 3 abnormal strain. This type of fault that occur is very disastrous and dangerous.

Hence, an abnormal IGBT over 1 current flow produces rigorous damage to a lot of sectors of the structure and hence a total shutdown of the system is generally recommended. The main reason behind the open circuits fault is when gating signal is lost, thermal feedback cycling, and fault in the driving circuits of the gate. Due to open circuits fault the overall effect is that the performance of the system is decreased. However if the whole system is programmed to be fault tolerant complete shutdown can be avoided [11].

The author's consider the dependability of semiconductor power and solder joint failures. 34% of the breakdown of the converter system is caused due to this attribute of the system [12]. The author's propose that "Cascaded topologies have been analyzed suppressing Total Count of Switches (TCS). Since these structures have modular structure, most of them have no FT feature for any switch failure. Therefore, most of RSC-MLIs are not fault tolerant for open switch faults." [13]

Referenced papers proposed MLI consider the symmetric and asymmetric configurations [14], with both said to offer superior performance to conventional MLIs, while considerably reducing the component count, but limited in their ability to function in the occasion failure due to open switch faults.

The authors presented a model cross-connected sources based MLI (CCS-MLI) which has lower number of switch counts [15] albeit with very partial fault tolerance ability. In the literature, the researcher proposed model have been surveyed that the MLI topologies can be devised that consist of post fault-tolerant operation, As per the need of application the control mechanism and reliability can be tailored. This research work focuses on the expansion of decorating fault tolerance feature to proposed 3-Φ RSC-MLIs so that in the event of open circuits faults in different power devices the dc-ac converter system work efficiently[16].

III. METHODOLOGY

The proposed model work has been illustrated through some of the RSC-MLI topologies examples for fault tolerant feature added MLIs. In meantime, two new 3-Φ FT RSC-MLIs has been introduced. Proposed FT MLIs all operation and performance is discussed in different chapters. A comprehensive examination of combinations of switching is being studied to deal with the failure of switch that occurs in individual manners. While OSF case and its effect on the stepped waveform which was the output has been focussed on the work that is conducted in the ongoing work.

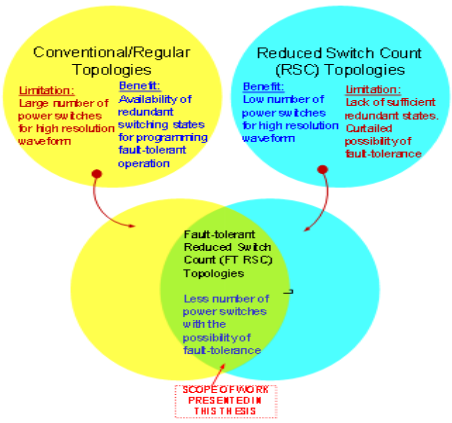

Fig.I Design pertaining to the research gap recognized for the work

The analysis made using OSF in RSC-MLIs reveals that preferred fault tolerant action can be achieved by making precise changes on these topologies, and this is based on the combination of the required voltage levels. Here, the designed voltage level is made by adding the minimum number of additional switches into the RSC-MLIs. It must be emphasized that fault recognition and troubleshooting issues are not examined in this proposed work. Fig.II displays a flow chart of the operation of the fault tolerant of the proposed 3-Φ MLIs in the occurrence of an OSF.

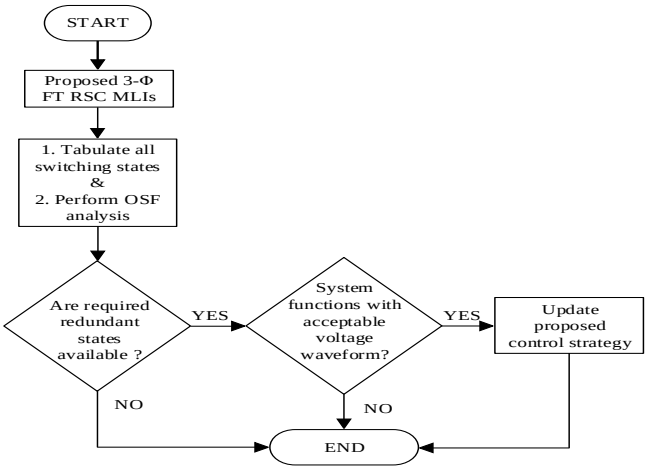

Fig. II Flowchart illustrating fault tolerant action of proposed 3-Φ FT RSC MLIs

Various control techniques are proposed in literature to modulate multilevel inverters. These control strategies are based on switching frequency which is low (space vector control, selective harmonic elimination and adjacent level control) and high switching frequency (space vector pulse width modulation (SVPWM) and multicarrier PWM). The use of this control scheme varies for different multilevel inverters. Henceforth, control methodology used for testing of proposed 3-Φ FT RSC-MLI topologies is developed for any given voltage-level with satisfactory performance. A schematic diagram of the control methodology is shown in Fig. 3.

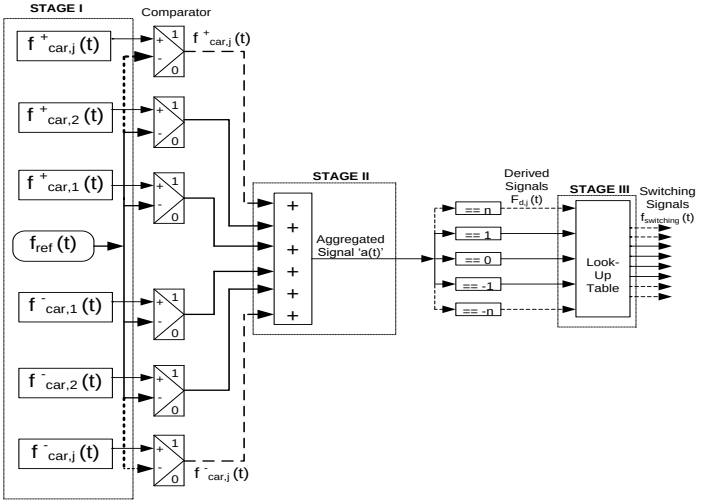

Fig. III Schematic diagram of control methodology

MATLAB software is used to imitate the proposed 3-Φ FT RSC-MLIs and the obtained results are verified. The circuit parameters taken for simulation and real time studies for proposed FT topologies are listed in Table 1.

TABLE I. PARAMETERS USED IN SIMULATION AND REAL TIME STUDIES

Parameter	**Data**
DC supply	24V
Reference frequency	f_m=50Hz
Carrier frequency	f_c=3000Hz

Modulation Index	m_a= 0.85
Inductive load	R = 20Ω, L=10mH

To validate the simulated results, real time simulation studies are carried out for the proposed 3-Φ FT RSC-MLIs. A OPAL-RT OP5600 real time digital simulator is used for validation of the obtained simulation results. The real time simulator setup consists of several types of equipment such as host-PC with MATLAB toolbox, connecting probes, digital storage oscilloscope.

IV. CONCLUSION AND FUTURE WORK

The primary idea of this proposed work is to examine 3-Φ fault tolerant reduced switch count multilevel inverters (RSC-MLIs) for open circuit fault occurred in single or multi power switches. However, most of the RSC-MLIs have some compromises in characteristics of MLIs such as reduce redundancy, fault tolerant capability, reliability, increases voltage rating of switches, cost and control complexity. In spite of these compromises, there exists significant potential on configuration of MLIs with the chances to impart fault tolerance characteristics on them. Thereby, the work offered in this paper aims at arriving at topological solutions by modifications in the proposed 3-Φ RSC-MLIs with imparting proposed fault tolerance feature to overcome or minimize the aforementioned limitations. The simulation results obtained are validated in real time simulator (OPAL-RT). It is observed that all the proposed FT topologies have been shown improved performance with proposed FT control technique. Results and comparative assessment reports demonstrate the efficacy and robustness of the proposed technique.

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