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Design and Performance Efficiency Analysis of a Low Power 4-bit Arithmetic Logic Unit

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Abstract: - In this paper, a novel low-power and low-transistor-count 4-bit ALU using Gate Diffusion Input technique, which reduces dynamic power consumption. We present a comprehensive analysis and simulation of the 4-bit ALU, comparing its performance in terms of power consumption, area, and delay with CMOS and GDI techniques. The GDI technique demonstrated superior performance characteristics, particularly in power dissipation, area, and propagation delay. This study focuses on the 4-bit ALU designed with both 45nm and 32nm technology for optimal low power and minimal area. The outcome reveals that the GDI technique significantly outperforms CMOS, with a reduced transistor count by half, leading to lower delay, reduced power consumption, and increased speed. These findings suggest that the 4-bit ALU using GDI techniques is a highly viable option for low-power digital design.

Keywords: CMOS, ALU, Leakage power, Low power analysis.

1. INTRODUCTION

A central processing unit (CPU), memory, and input/output units are the fundamental components of a computing device. The CPU functions similarly to the human brain, comprising all registers, the control unit, and the ALU. The ALU is considered the most powerful digital computer subsystem. It is a digital circuit which would performs arithmetic, logical, and bit-shifting operations on n-bit digital words. Functionally, the ALU can be divided into three circuits: the arithmetic circuit, the logical circuit, and the shift circuit.

The core of a microprocessor is the ALU, capable of executing a variety of arithmetic and logical operations. Most operations, such as addition, require two binary inputs (A and B) to produce a binary output, while some operations, like increment or decrement, require only one input. Thus, an ALU typically has two binary inputs and one binary output for data processing, along with a binary input for selecting the appropriate operation. A simple ALU can be created from a 4-bit adder by adding a control line to facilitate both addition and subtraction.

The ALU consists of two main functional components: the logic block and the arithmetic block. The arithmetic block is responsible for performing arithmetic operations such as addition, subtraction, and comparison, with an adder being the central element of this unit. The logic block handles basic logical operations, including AND, OR, and XOR.

2. RELATED WORK

Circuit design is crucial for the development of digital circuits, such as multipliers. To ensure the multiplier operates at the desired clock rate, the designer must understand the delay of the critical path and determine the timing for inserting pipeline stages. To minimize the multiplier's area, different adder architectures are explored. Circuit analysis verifies the functions and performance of these adders. The adder's architecture must be established first, followed by determining the number of pipeline stages based on the adder's speed. The multiplier should be as compact as possible while meeting all requirements. Fast arithmetic necessitates fast circuits, which in turn require a small size to reduce wire delay effects. A small size allows for single-chip implementation, reducing wire delays and enabling integration into larger single-chip systems to minimize I/O delays. The rising demand for low-power VLSI emphasizes the need for power-efficient logic styles. Performance criteria for logic styles include circuit speed, size, power dissipation, wiring complexity, ease of use, and generality of gates in cell-based design techniques. Dynamic logic styles are often chosen for high-speed circuits but are less suitable for low-power implementations due to high node activity and large clock loads.

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In VLSI, especially in DSPs and microprocessors, logic gates and arithmetic circuits are extensively utilized. Common operations within these circuits include AND, OR, addition, subtraction, and multiplication. Logic gates and full adder cells are fundamental components in arithmetic circuits, and their efficiency is crucial. The demand for low-power systems has surged in mobile communication and computation due to rapid technological advancements. As devices scale down to the nanometer regime, arithmetic and logic circuits must be designed to minimize power consumption, size, and propagation delay.

A processor is a critical part of any digital system, and the ALU (Arithmetic Logic Unit) is a primary component of a microprocessor. The ALU performs arithmetic and logical operations on pairs of n-bit operands and must be designed to be compact, power-efficient, and fast. CMOS technology, which uses both PMOS and NMOS transistors, traditionally results in high power dissipation and delay. However, the Gate Diffusion Input (GDI) technique can reduce power consumption, area, and improve speed compared to CMOS.

The GDI technique allows for the implementation of complex logic functions using only two transistors, making it suitable for fast, low-power circuit design. This method enhances power characteristics and simplifies design using a small cell library based on Shannon's theorem. This work aims to explore and compare the GDI technique with CMOS, particularly in designing an ALU. The GDI-based ALU design demonstrates the efficiency of this technique.

Vaijayanti Panse et al. proposed minimizing transistor count for a 2:1 MUX using the GDI technique, showing its advantage over conventional CMOS in 90nm process technology. Biswarup Mukherjee et al. introduced a low-power, high-speed full adder using GDI-based multiplexers, achieving superior performance compared to standard CMOS designs. Amanpreet Kaur conducted a comparative analysis of GDI-based D flip-flop circuits in 90nm and 180nm technologies, further highlighting the benefits of GDI in low-power VLSI design.

3. METHODOLOGY

In digital electronics, an Arithmetic Logic Unit (ALU) is a digital circuit that performs arithmetic and bitwise logical operations on integer binary numbers. It is a critical component of the central processing unit (CPU) in many computers. The ALU designed in this study carries out operations such as addition, subtraction, comparison, and various logic functions. Figure 4 presents the block diagram of the proposed ALU. In this diagram, the full adder/subtractor requires three inputs: A, B, and Cin, while all other operations require only two inputs. A multiplexer, controlled by select lines, determines the operation, and the output is then generated.

The ALU is a vital component of a microprocessor, utilizing fast dynamic logic circuits and carefully optimized structures. It significantly contributes to the overall power consumption of the data path. The ALU is also one of the highest power-density regions within the processor, as it operates at maximum speed and is frequently active, leading to thermal hotspots and sharp temperature gradients within the core. Power dissipation, which generates heat and requires careful management, is a critical factor affecting the device's performance. Electrical and electronic devices have limitations on the current they can safely handle, not due to electronic constraints, but due to physical ones. For example, while a transistor can handle a certain current, it's wise to set a lower threshold to avoid overheating the die. Dissipation, measured in watts, is calculated using Ohm's law. In most Very Large Scale Integration (VLSI) applications, the full adder circuit is a fundamental building block and a key element in complex arithmetic circuits such as microprocessors, digital signal processors, and other ALUs. Nearly all complex computational circuits require full adder circuitry, and the power consumption of the entire computational block can be reduced by applying low-power techniques to the full adder circuitry. Numerous studies have proposed various full adder circuits based on different low-power techniques. In this work, we designed the ALU using GDI cells to implement the multiplexers and the full adder circuit.

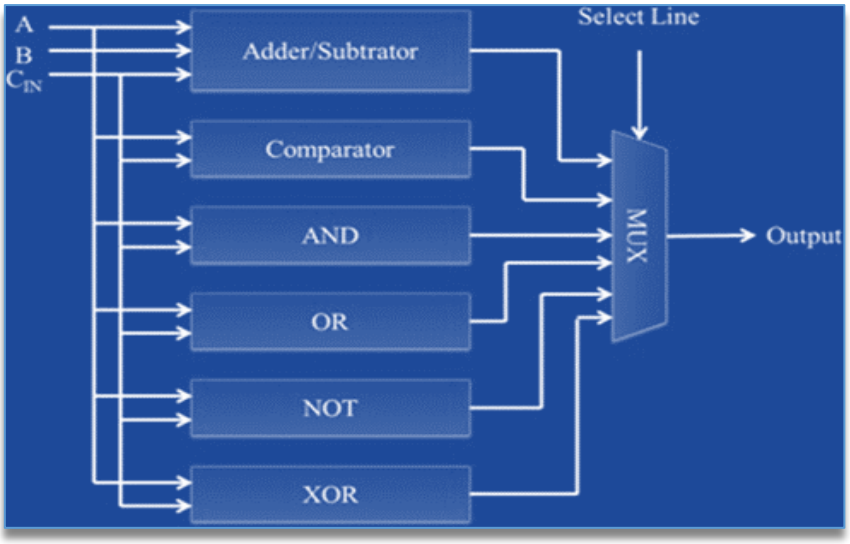

Fig 1 Block diagram of the ALU Circuit

Arithmetic, the oldest and most fundamental branch of mathematics, focuses on the study of numbers and basic operations such as addition, subtraction, multiplication, and division. It is a crucial component of number theory, which, along with algebra, geometry, and analysis, constitutes one of the core divisions of modern mathematics. The arithmetic logic unit (ALU) designed in this study performs arithmetic operations, including addition, subtraction, and comparison. The comparator within the ALU is responsible for determining whether values are less than, greater than, or equal to one another.

A digital logic gate is an electronic device that makes logical decisions based on different combinations of digital signals at its inputs. Although digital logic gates can have multiple inputs, they typically produce a single digital output. These gates can be interconnected to create combinational or sequential circuits, allowing for more complex logic functions. The ALU circuit proposed in this study performs several logic operations, including AND, OR, NOT, and XOR.

4. SIMULATIONS AND RESULTS

The simulation results of cadence for 45nm technology is shown below which illustrates that the ALU operation is working properly.

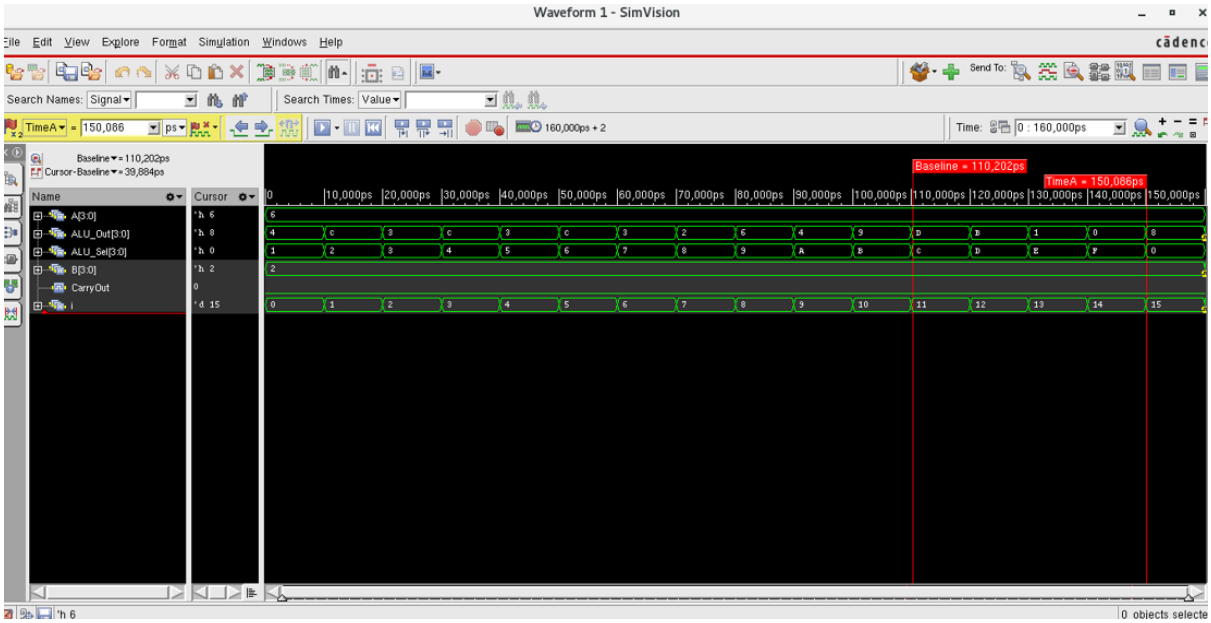

Fig 2: The simulation result of the ALU using 45nm technology

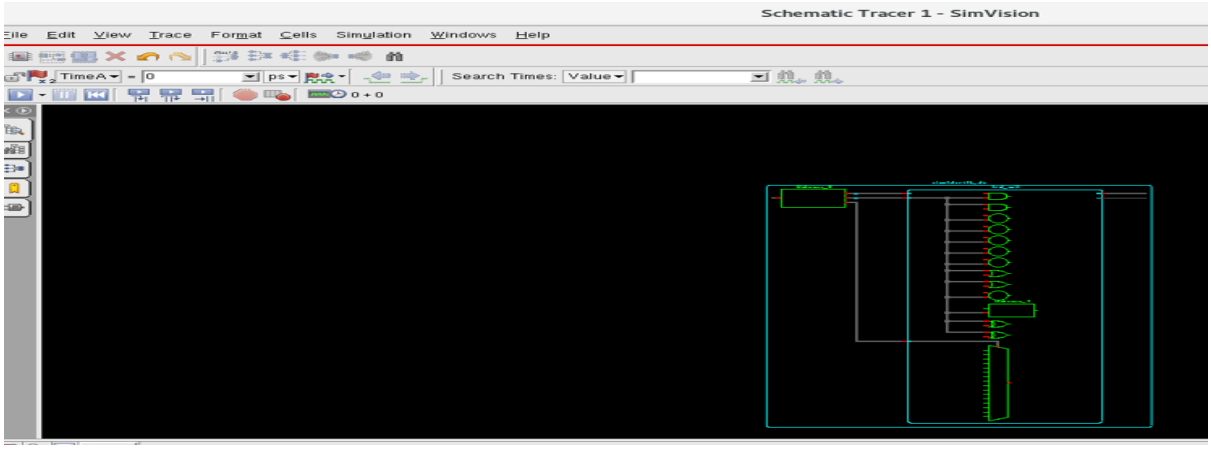

Fig 3: The schematic view of ALU using 45nm technology

The netlist for 4 bit ALU is shown below

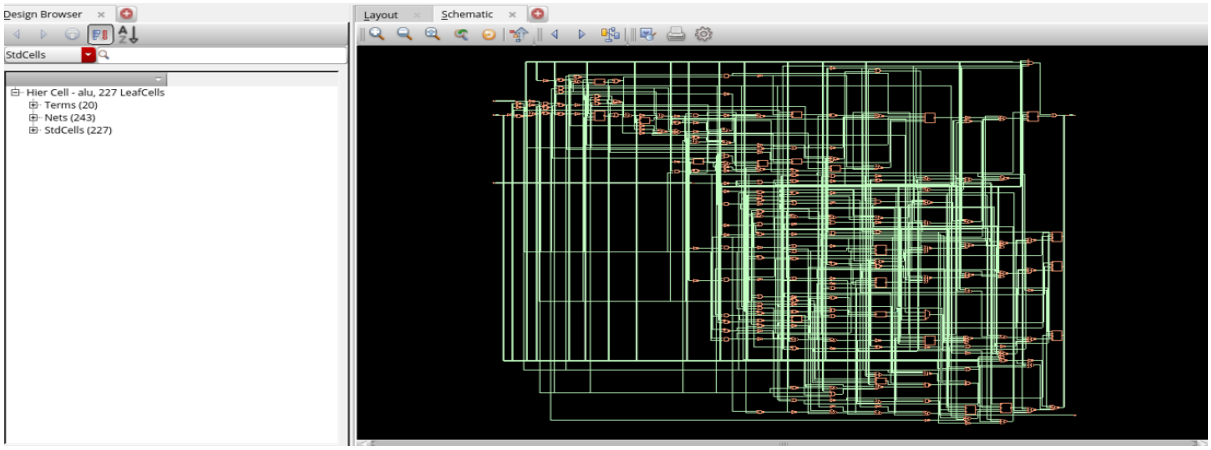

Fig 4: The netlist schematic for 4 bit ALU for 45nm technology

The netlist schematic for the 4 bit ALU is shown in Fig 3 and Fig 4 for 45nm technology.

Instance Module	Cell Count	Cell Area	Net Area	Total Area	Wireload
alu	227	0.000	0.000	0.000	<none> (D)

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	2.49648e-08	1.71138e-05	6.78683e-06	2.39255e-05	100.00%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	2.49648e-08	1.71138e-05	6.78683e-06	2.39255e-05	100.00%
Percentage	0.10%	71.53%	28.37%	100.00%	100.00%

Fig 5 Cell count and the power dissipation in 4 bit ALU for 45nm Technology

The simulation results of synopsys for 32 nm technology is shown Fig 6.

The simulation results of synopsys for 32 nm technology is shown below

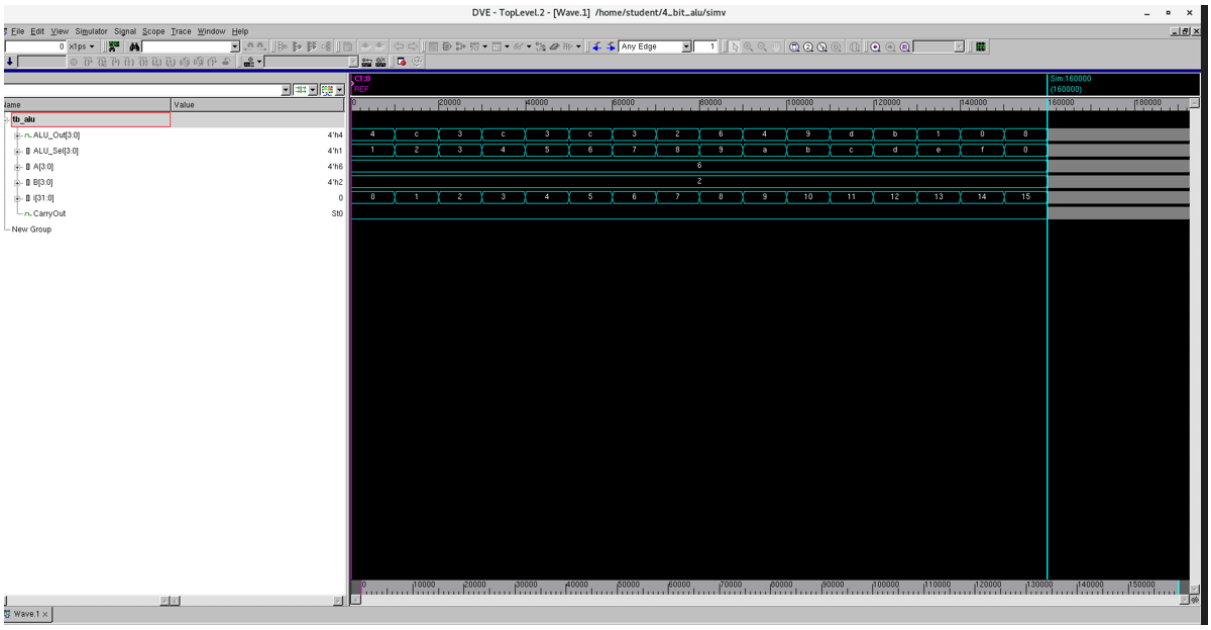

Fig 6: simulation results of synopsys for 32 nm technology

The schematic view of the 4 bit ALU is shown below

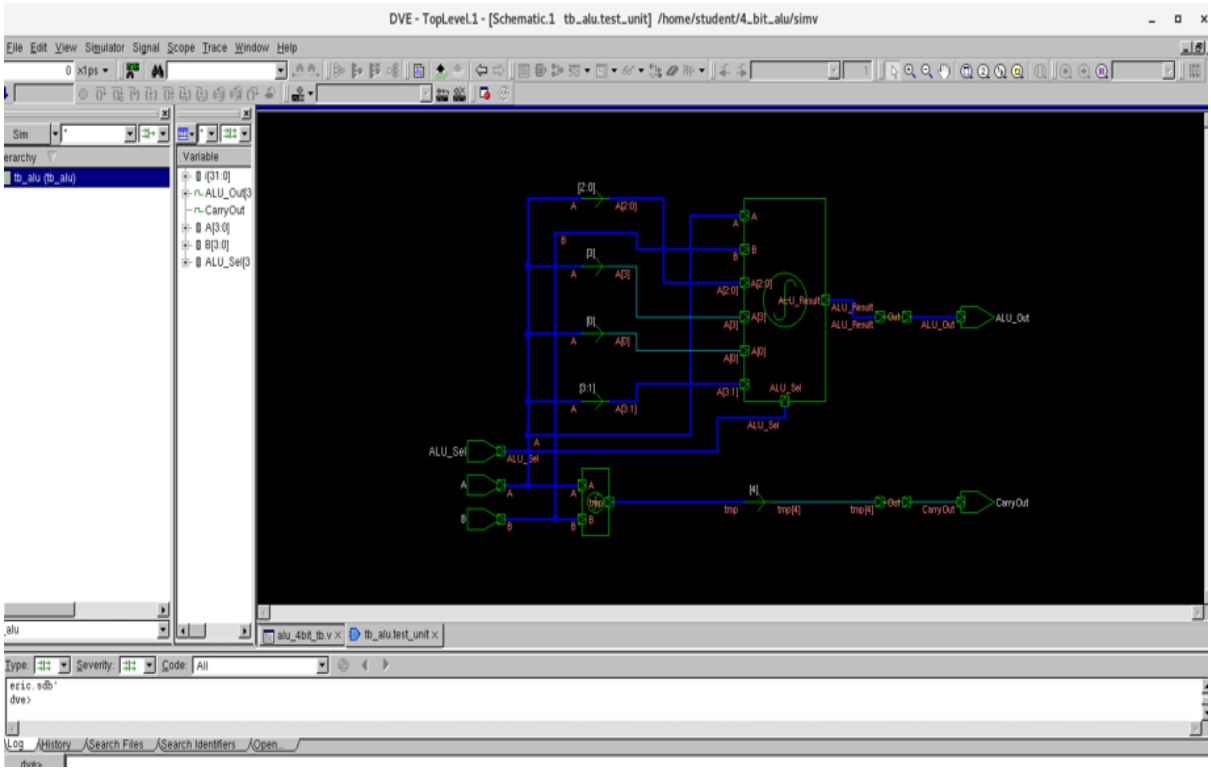

Fig 7: The schematic view of the 4 bit ALU for 32nm Technology

The gate level netlist for 4 bit ALU is shown below

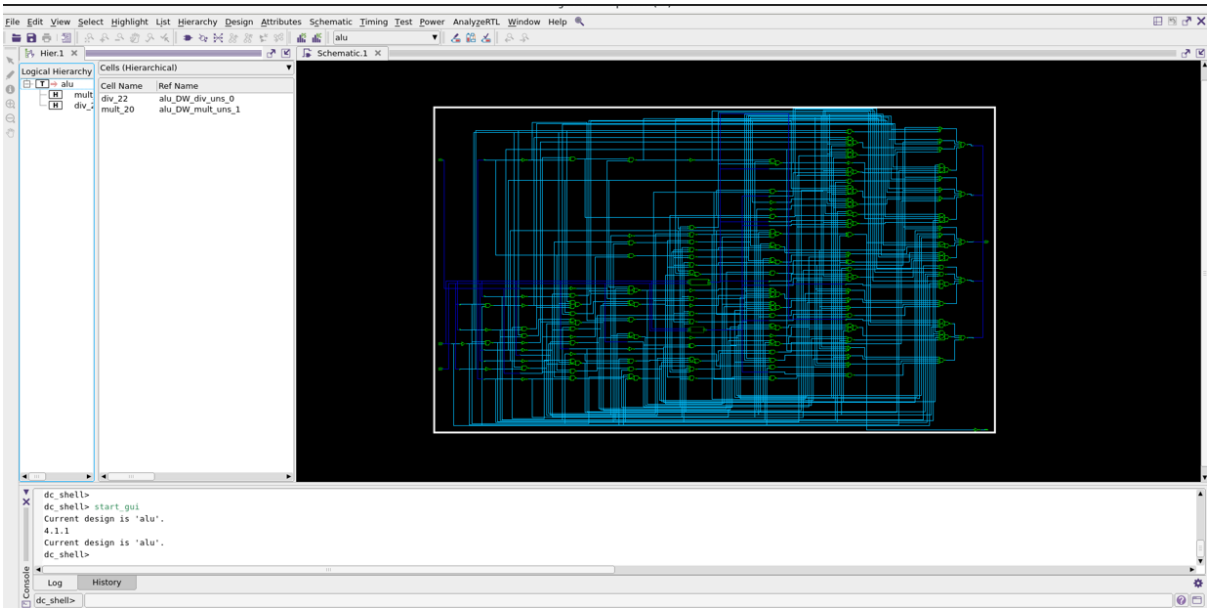

Fig 8: The gate level netlist for 4 bit ALU is shown below

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Number of ports:                          61
Number of nets:                          292
Number of cells:                         244
Number of combinational cells:           242
Number of sequential cells:                0
Number of macros/black boxes:              0
Number of buf/inv:                        49
Number of references:                     19

Combinational area:                562.166532
Buf/Inv area:                       62.265280
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:              89.641920

Total cell area:                   562.166532
Total area:                        651.808453
```

```
                 Internal         Switching           Leakage             Total
Power Group      Power            Power               Power               Power   (   %    )
--------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000              0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000              0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000              0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000              0.0000  (   0.00%)
register           0.0000           0.0000              0.0000              0.0000  (   0.00%)
sequential         0.0000           0.0000              0.0000              0.0000  (   0.00%)
combinational     41.3311          19.2422          2.1346e+07             81.9197  ( 100.00%)
--------------------------------------------------------------------------------------------
Total             41.3311 uW       19.2422 uW       2.1346e+07 pW          81.9197 uW
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Fig 9 : Cell count and power dissipation in 32nm Technology.

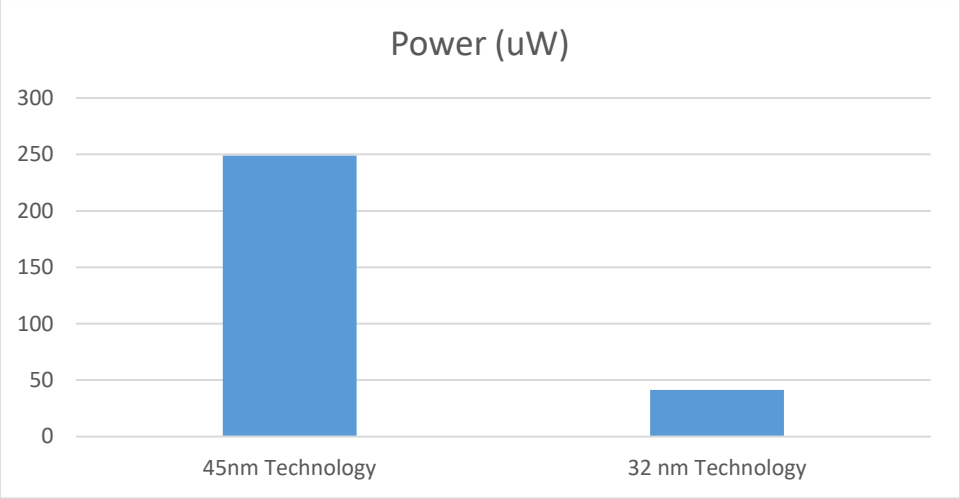

Fig 10: count versus technology for 45nm and 32nm technology

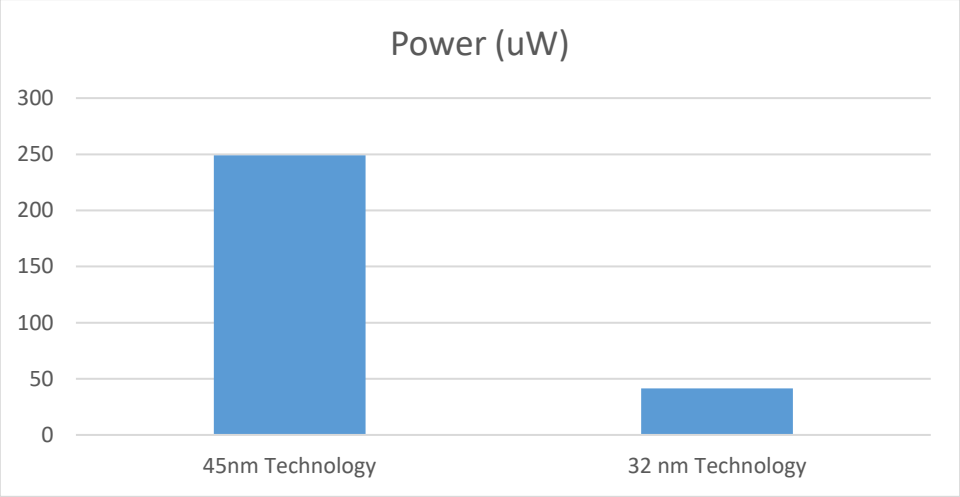

Fig 11: Power versus technology for 45nm and 32nm technology.

Fig 10 shows the cell count of 4 bit ALU for 45nm and 32nm technology and is observed that the cell count is more in 45nm technology than 32nm technology. Fig 11 shows the power dissipation versus technology is shown. It is observed that 32nm technology dissipates less power than the 45nm technology.

CONCLUSION

The GDI implementation reduces the number of power supply-to-ground connections, thereby lowering dynamic power consumption. This paper introduces an innovative low-power, low-transistor-count 4-bit ALU, and evaluates its performance in terms of power consumption, area, and delay. We conducted analysis and simulations on the 4-bit ALU using the GDI technique, comparing its power dissipation, propagation delay, and transistor count with those of CMOS-based designs. The results showed that the GDI technique outperformed all other design methods. The 4-bit ALU was developed using both 45nm and 32nm technology for optimized low power and minimal area. The GDI technique proved to be superior to CMOS in terms of power dissipation, area efficiency, and propagation delay. The combination of low power consumption and a reduced transistor count makes the 4-bit ALU using GDI techniques an excellent choice for low-power designs. The transistor count in GDI is halved compared to CMOS, leading to reduced delay, lower power consumption, and increased speed.

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