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Modelling, Analysis and Control of Multiphase Synchronous Buck Converters

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Step-down multiphase dc-dc converters enable very low voltages and high currents through parallel operation. Additionally, high redundancy, fault tolerance and very fast output voltage dynamics can be obtained by using synchronous switching and interleaving. The current balance in the various converters can be achieved by different methods: average current control, peak current control, etc. This paper analyzes and compares the steady-state and dynamic performance of two current control methods from simulations and experimental results when using three paralleled converters. It is concluded that similar performance is achieved by the two methods.

Keywords: Dc-dc Buck converters, Interleaving control, Multiphase converters, Parallel operation.

1. Introduction

FA large part of the electrical energy conversion is done using dc-dc topologies based on electronic power converters. There are a large set of dc-dc conversion topologies: isolated and non-isolated, unidirectional or bidirectional in power, with powers below 1 Watt and in the range above megawatt. In particular, and in a wide range of applications, step down dc-dc converters are critical, as in automotive industry, [1], microprocessor power supplies, [2], photovoltaic applications, [3, 4], or unmanned aerial vehicles (UAVs), [5]. On the other hand, when the power handled by the converter is associated with very low voltages and high currents, there are advantages or even the need to configure the converter for some kind of parallel operation to reduce the current in the simple elements of the converter. Parallel operation minimizes losses and increases reliability, and adds modularity and fault tolerance to the converter, either in dc systems, [2], and in ac systems, [6].

This parallel operation of dc-dc converters can be performed in different ways: by semiconductors, or by elementary converters with common input and output, [7]. In the latter case, in addition to distributing the total load current across the various branches and semiconductors, it is possible to obtain additional advantages such as: equivalent frequency increase, reduced current ripple in the input and output stages, better dynamic performance, [4], [8]. To obtain these advantages it is necessary to operate the converter with an appropriate control method, in particular based on the concept of interleaving, [9, 10]. As a consequence, the first two advantages reduce the size and cost of passive components. On the other hand, with the availability of various types of integrated semiconductor modules, it is possible to replace a diode with a transistor and thereby use synchronized switching, [11, 12]. This allows optimizing the drive's dynamic operating range over a wide range of load power as there is no operating zone with discontinuous current, thus increasing the converter linearity.

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However, like any mode of parallel operation, it is necessary to ensure the balance and distribution of currents in the various branches in parallel. Among the various possible alternatives, as presented in [13, 14, 15], the most commonly used methods for current equalization are the control of the maximum (or minimum) value of the current in the inductor and the control of the average value, [7, 16], with special focus on digital control [17] and computer aided design tools, [18, 19]. Sliding mode techniques are also capable of guaranteeing robustness, stability and improved efficiency, [15, 20]. Additionally, to overcome the poor light load efficiency in multiphase converters, several phase shedding approaches are used to improve it, [21, 22]. In order to fully understand the interleaved operation, either in steady-state and in transient conditions, different modelling approaches have been used, in time domain, [14], and in frequency domain, [23], and a unified approach presented in [24].

This paper evaluates and compares the performance of these two control methods through simulation and experimental testing using an interleaved converter with three phases and synchronized switching.

2. Multiphase DC-DC Converter

This section discusses the main aspects of interleaving approaches and current sharing methods, passive component sizing as well as controller design. The simplified power structure of the multiphase synchronous step-down converter is shown in Figure 1. Switches S_k and S_{kc} have complementary command signals and, ideally, have the same voltage drop and switching characteristics. In the same view, the output inductances have equal parameters, L_k and r_k.

As can be easily deduced from Fig. 1 and also well known, the main features/advantages of the multiphase converter are: high modularity and reliability, fault tolerance capability, load current sharing, reduction of current ripple in the input source and output capacitor, small output voltage ripple, high dynamics. Additionally, the converter can achieve high efficiency levels in all load range, namely using phase blocking/shedding, [21, 22].

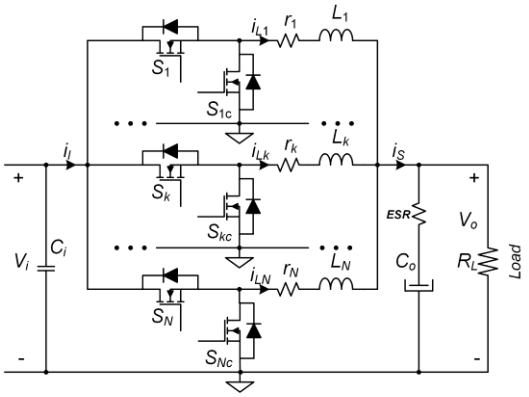

Figure 1. Multiphase synchronous step-down converter with *N* phases.

Heavy loads require all phases in operation and thus nominal and optimized operation (e.g. the efficiency). However, for lighter loads the witching losses will become dominant over the conduction ones and the efficiency deteriorates. In order to achieve high efficiency

in all load conditions, the multiphase buck converter can block non-required phases thus reducing the losses but with a cost; the voltage ripple will also increase.

2.1. Interleaving Approaches

The presence of more than one converter guarantees higher redundancy in case of failure and gives the opportunity to interleave them in order to reduce the harmonic content and ripple in both the source current and output current. The same optimization is also verified in the output voltage. Interleaved switching options are represented in Figure 2.

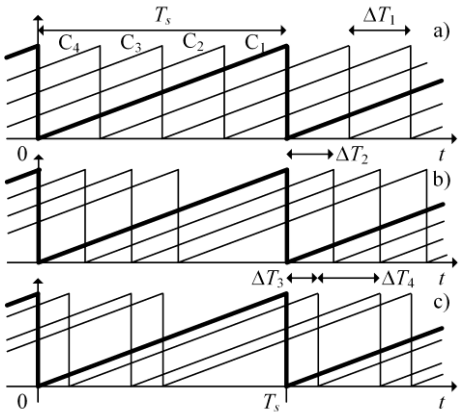

Figure 2. Interleaved switching options in a 4-phase step-down converter: a) symmetrical interleaving; b) asymmetrical interleaving I; c) asymmetrical interleaving II.

The conventional (symmetric) interleaving method (Fig. 2 a)) implies the carrier time delay to be equal to T_S / N of a switching cycle (with frequency F_S) when N converters are connected in parallel. It can be concluded from the Fourier analysis of the global output current that symmetric interleaving, under ideal conditions, cancels all voltage and current harmonics multiples of the carrier frequency, only remaining components starting at NF_S, [25]. This perfect harmonic cancellation only occurs if all the following conditions are simultaneously fulfilled:

- The converter parameters are equal;
- The delay angle of the PWM switching is symmetrical for all converters;
- The interleaved PWM converter has equal load sharing.

By converter parameters it is meant the voltage drop across the electronic switches, the inductance values and their equivalent loss resistance, [26]. The symmetrical delay angle is assured by some synchronization method between the converters and can be accomplished by several methods, with centralized and decentralized operation, [10, 27].

In different applications it could be desirable to selectively reduce harmonics in specified frequency ranges. For example, the size of an Electro-Magnetic Interference (EMI) filter is usually determined by the attenuation required at a particular frequency, or range of frequencies. This can be achieved using a different approach to interleaving, in which the carrier time shift is not confined to $\Delta T_1 = T_S / N$ as in Fig. 2a), but can vary from one pair of converters to another. Methods in Fig. 2b) and c) do not provide flat harmonic cancellation until NF_S, and could be used in such conditions.

2.2. Current Sharing Methods

Current sharing methods fall into two categories from the point of view of the current sharing operation mechanism, namely passive droop methods, [28], and active current sharing methods, [7].

In a droop method the converter output voltage slightly decreases as the current increases. Its operating mechanism is to shape the equivalent output impedance to achieve current sharing between the various converters. This family of control methods does not require wired interconnections between the control circuits of the various paralleled converters, and is therefore in fact an open loop technique that individually defines the output impedance of each converter.

Active current sharing methods are a combination of specific control methods and current sharing error processing methods, including self-balancing and sensorless methods, [27, 29, 30, 31]. Among active current sharing methods it should be highlighted the internal loop regulation, the outer loop regulation and external controller methods, [7]. Their main merits and possible drawbacks are described in the following paragraphs.

In the internal loop regulation method the reference voltage, the voltage feedback and the compensator block are common. The internal loop regulation has stable current sharing, precise output voltage regulation and fast dynamics. Its disadvantages are: it degrades system modularity and has poor fault tolerance.

The outer loop regulation approach uses a current-programming error to adjust the reference of the outer voltage loop until equal load current sharing is achieved. The method has good modularity, and has flexibility in system configuration, making it easy to expand or maintain the global system; has excellent fault tolerance. Disadvantages, however, are the possibility of transient instability and limited feedback voltage gain.

The external controller approach has good current sharing and output voltage regulation; it is easy to implement fault monitoring. The associated disadvantages come from the need of more interconnections between modules and the external controller. Then, a decreased degree of modularity and decreased reliability due to more interconnections and more complex control is associated with it.

In this work it was selected for analysis and implementation the internal loop regulation method; the control block diagram is shown in Figure 3. The control architecture is based on an external (common) voltage regulation loop and a current sharing loop.

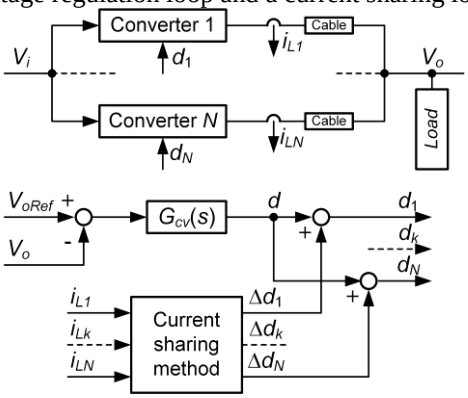

Figure 3. Block diagram of the proposed controller: internal current loop regulation method and output voltage regulation.

2.3. Passive Components Sizing

Assuming continuous conduction (the only mode in this converter due to synchronous switching), the inductor current ripple in a generic branch of the multiphase converter in Fig. 1 is given by:

$$\Delta I_L = \frac{V_o}{LF_s}(1-D) \tag{1}$$

where V_o is the output voltage, L is the inductance value of the inductor, F_s is the switching frequency and D is the duty-cycle. As known, when neglecting losses, $V_o = DV_i$.

In a multiphase Buck converter operating under ideal conditions, the ripple of the summed output currents (flowing into the capacitor), ΔI_s, results lower than that of each phase, [16], and is given by:

$$\Delta I_s(D,N) = \frac{V_o}{LF_s}\left(1-\frac{m}{DN}\right)(1+m-ND) \tag{2}$$

where D is the nominal duty-cycle, N is the number of phases and $m = floor(D \cdot N)$, where $floor()$ is the largest integer less than $D \cdot N$. The expression can be used to size L from ΔI_s's knowledge or specification. For example, if $D < 1/N$ then $m = 0$ and (2) simplifies to (3):

$$\Delta I_s = \frac{V_o}{LF_s}(1-ND) \tag{3}$$

The result in (2) for ΔI_s is smaller than the inductor ripple current given by (1) due to current harmonics cancellation of the interleaved Buck converters, and could be used for sizing L. Alternatively, knowing that in steady-state, the output voltage ripple is mainly given by $\Delta V_o = ESR \cdot \Delta I_s$, then L can be obtained from:

$$L = ESR\frac{1}{\Delta V_o}\frac{V_o}{LF_s}\left(1-\frac{m}{DN}\right)(1+m-ND) \tag{4}$$

where ESR is the equivalent series resistor of the bulk output capacitor. As the main function of the output capacitor during steady-state is to limit the output voltage ripple, ΔV_o, within a specified level, the minimum filter capacitance $C_o(D,N)$ can be calculated for multiphase converters by:

$$C_o(D,N) = \frac{\Delta I_s(D,N)}{8NF_s\Delta V_o} \tag{5}$$

The last two equations provide design guidelines for L and C_o according to imposed specifications and available degrees of freedom, [32].

2.4. Controller Design

To design the two controllers inside the converter, it is needed to know the dynamic response of the two variables (inductor current and output voltage) as a function of the control variable, the duty-cycle d. Each phase current and the output voltage are described by:

$$\begin{cases} L_k \dfrac{di_{Lk}}{dt} = -r_k i_{Lk} - v_o + V_i d_k, \qquad k = 1,...,N \\ C_o \dfrac{dv_o}{dt} = \sum\limits_{k=1}^{N} i_{Lk} - \dfrac{v_o}{R_L} \end{cases} \tag{6}$$

where R_L is the equivalent load. As it is a switched electronic converter (with $d_k \in \{0,1\}$ and being $d_j(t) \neq d_k(t)$) with several interacting variables, it is necessary to analyse its frequency response using a linearized AC model, [33, 34].

From the AC model, it can be obtained the transfer function of the inductor current in one-phase in relation to the duty-cycle of the same phase, $I_{Lk}(s)/D_k(s)$, as in (7) for an ideal lossless converter with equal L in the N phases:

$$\frac{I_k(s)}{D_k(s)} = \frac{V_i}{sL} \cdot \frac{s^2 + 1/(R_L C_o)s + (N-1)/(LC_o)}{s^2 + 1/(R_L C_o)s + N/(LC_o)} \tag{7}$$

It is concluded that the denominator is the same as in a single Buck converter (with normalized L) but the numerator is quite different, with two zeros and an integrator. Alternatively, the frequency response can be obtained by directly simulating the global power structure around a working point and introducing AC disturbances.

Differently, the frequency response of the output voltage in relation to the duty-cycle of one phase is quite similar to the single Buck converter, as shown in (8), if a normalized L is considered:

$$\frac{V_o(s)}{D_k(s)} = \frac{V_i}{LC_o} \cdot \frac{1}{s^2 + 1/(R_L C_o)s + N/(LC_o)} \tag{8}$$

In the more complex models behind the two last expressions, it is immediate to include several parasitic terms, e.g., voltage drop in the switches, losses in inductors and capacitors, which facilitates, when using software tools, the knowledge of different gains and the correct identification of poles and zeros in the frequency response diagram.

2.5 Frequency Response Analysis

In order to show the frequency response characteristics corresponding to (7) and (8) with the addition of the main parasitic elements, the general specifications and resulting passive components for the conversion system are presented in Table 1 for the proposed system. It is also given the parasitic elements and the switch model, $r_{DS(on)}$.

Table 1: Main requirements and parameters.

Parameter	Name	Value
Input voltage	V_i	48 V
Output voltage	V_o	24 V
Nominal power	P_n	120 W
Nº of phases	N	3
Nominal inductance	L	430 µH
L parasitic	ESR_L	0.8 Ohm
Nominal capacitance	C	100 µF
C parasitic	ESR_C	0.06 Ohm
Switching frequency	F_s	10 kHz
Ripple voltage	ΔV_o	40 mV
Ripple current	ΔI_o	2.8 A
Switch model	r_{DS}	0.12 Ohm

The high value of the ripple current was selected to impose a negative current in the inductor in a large range of loads and make use of the synchronous switching. Regarding inductance values, a large tolerance was also considered, i.e. more than ±15%, in order to better analyse the behaviour of the two current sharing methods.

From the average AC model, two analyses are performed to identify the $I_{Lk}(s)/D_k(s)$ and $V_o(s)/D_k(s)$ transfer functions, both for continuous conduction mode (CCM) and including the parasitic elements indicated in Table 1. It is shown in Fig. 4 the frequency response of $I_{L1}(s)/D_1(s)$ and Fig. 5 shows the frequency response of $V_o(s)/D_1(s)$, both for $N=1,...,4$, interleaved converters. In the last case it was assumed that no inner current controller exists.

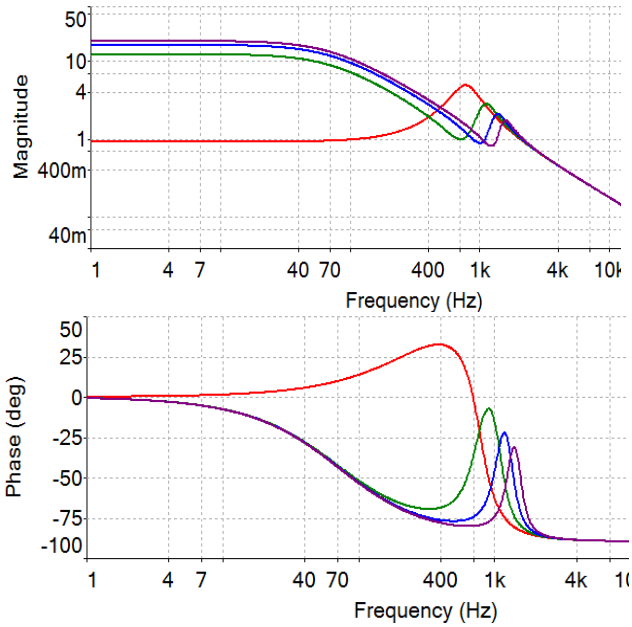

Figure 4. Frequency response of $I_{L1}(s)/D_1(s)$ for paralleled Buck converters in CCM and including losses (N=1, 2, 3, 4).

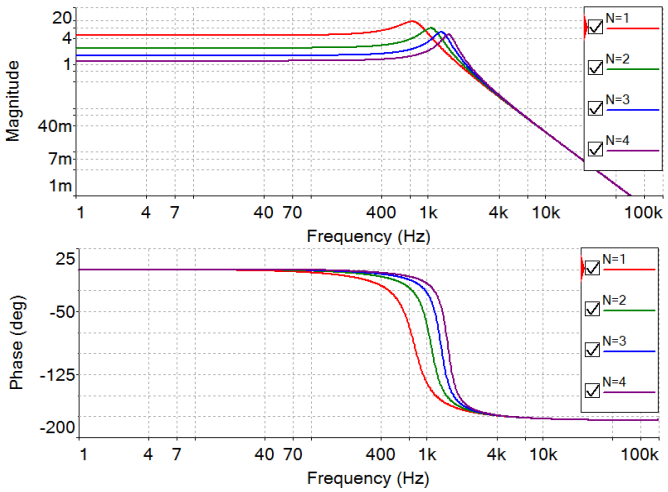

Figure 5. Frequency response of $V_o(s)/D_1(s)$ for paralleled Buck converters in CCM and including losses (N=1, 2, 3, 4).

For any N higher than 1, it can noticed the integrator effect in the low frequency region and the difference in the resonance frequency. The difference can be attributed to the dumping effect on each power stage from the other stages in parallel.

Regarding the frequency response of $V_o(s)$, it is noted a reduced gain in steady-state, according to the number of single converters as shown in eq. (7).

As can be concluded from the Bode diagrams plots, the dynamic response is somewhat faster as the number of single converters increases. Therefore, an appropriate and more precise small-signal model becomes significantly important to an adequate control loop design, e.g. when using CAD tools. In terms of current sharing method the frequency response characteristics applies to both.

In this work, and according to Fig. 3, two decoupled control loops were designed: an inner PI controller for current sharing, thus defining the duty-cycle correction to be applied to the common one, and an outer and slower controller to stabilize the output voltage, also a PI one.

3. Simulation Results

3.1. Steady-State Operation

For the steady-state some simulation results are presented, having been used both methods of current sharing: average current control (ACC) and peak current control (PCC). In ideal conditions, as referred in Section 2.1, with parameters given in Table 1, both methods perform similarly. In Fig. 6 are shown the steady-state waveforms for the three I_{Lk} currents, the equivalent output current and the output voltage. It is noticed that the equivalent (I_s) output current has a ripple frequency of three times the switching frequency, with a ripple magnitude of nearly one third of each converter current. The output voltage ($V_o = 24$ V, which means $m = 1$), has similar properties: the ripple frequency occurs at three times the switching frequency and satisfies the initial requirement of being less than 40 mV.

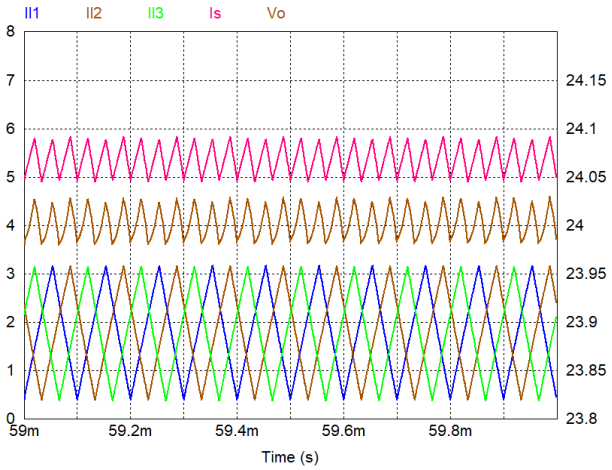

Figure 6. Ideal and nominal steady-state operation with the ACC or PCC methods: V_i=48 V, V_o=24 V, P_o=P_n. [Left vertical scale for currents: right vertical scale for the voltage].

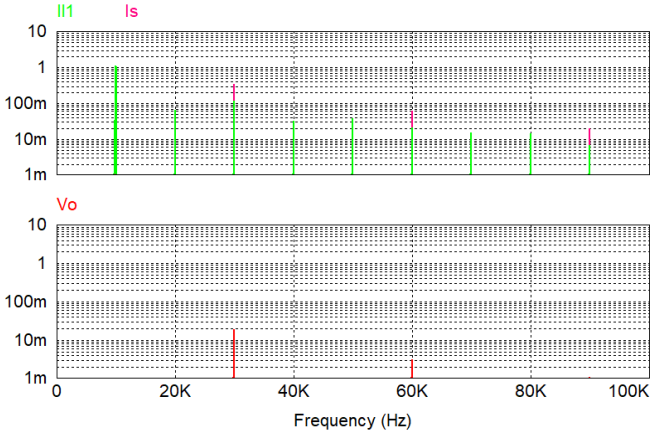

Figure 7. Harmonic spectrum of one converter current (IL1), total output current (Is) and output voltage (Vo), in ideal and nominal steady-state operation: Vi=48 V, Vo=24 V, Po=Pn, Fs=10 kHz.

Regarding the ideal condition, Fig. 7 confirms one of the main advantages of the interleaving methods, the reduction of the harmonic components either of the equivalent output current and the output voltage. For $F_s = 10\ \text{kHz}$, the harmonic spectrum only exhibits components at 30 kHz and multiples both for the equivalent output current and for the output voltage.

However, ideal conditions hardly occur in practical implementations. For the next analyses, and to highlight the characteristics of both methods, the following inductance values per phase (and respective losses) were used $L_1 = 430\ \mu\text{H}$, $r = 0.9\ \Omega$; $L_2 = 440\ \mu\text{H}$, $r = 0.9\ \Omega$; $L_3 = 630\ \mu\text{H}$, $r = 1.2\ \Omega$.

Figures 8 and 9 show the currents per phase, the current flowing into the output node (I_s) and the output voltage with $P_o = P_n$, for the ACC and the PCC methods, respectively.

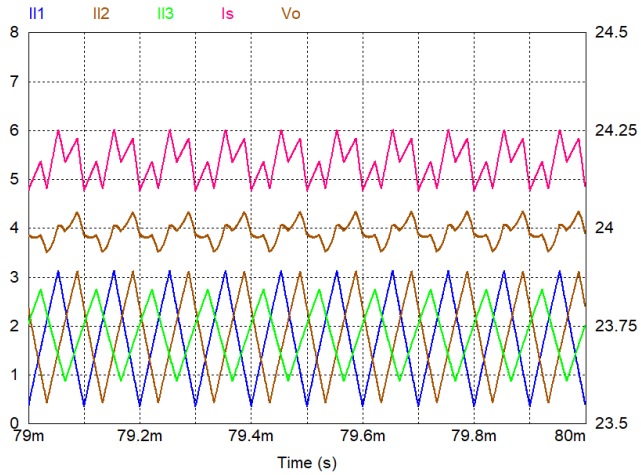

Figure 8. Steady-state operation with the ACC method: V_i=48 V, V_o=24 V, P_o=P_n. [Left vertical scale for currents: right vertical scale for the voltage].

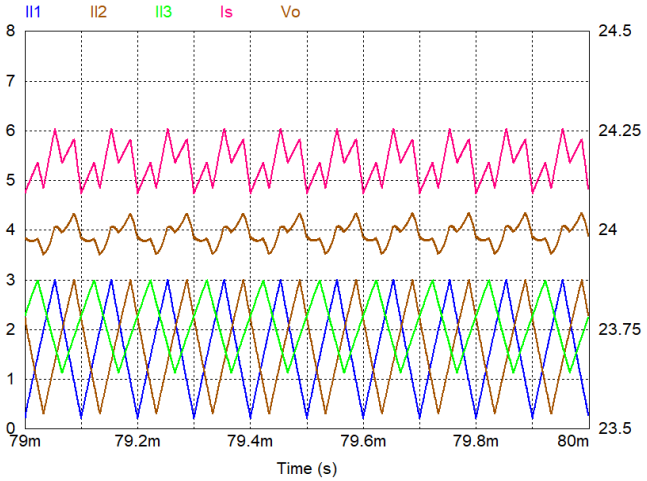

Figure 9. Steady-state operation with the PCC method: V_i=48 V, V_o=24 V, P_o=P_n. [Left vertical scale for currents: right vertical scale for the voltage].

Comparing with the ideal condition, where the ripple frequency occurs only at three times the switching frequency, when there are different inductances some important differences are noticed in both methods. The ripple current and the ripple voltage appear at the switching frequency and, in the PCC method, the average current values per phase are different. Regarding the output voltage, the effect is more important since the ripple voltage magnitude depends not only on the equivalent switching frequency but also on the ripple current.

An additional test is shown in Fig. 10 for the PCC method: operation with $V_o = 12$ V (which means $m = 0$), $P_o = P_n / 2$, maintaining the other conditions for the inductances, input and output voltages and switching frequency.

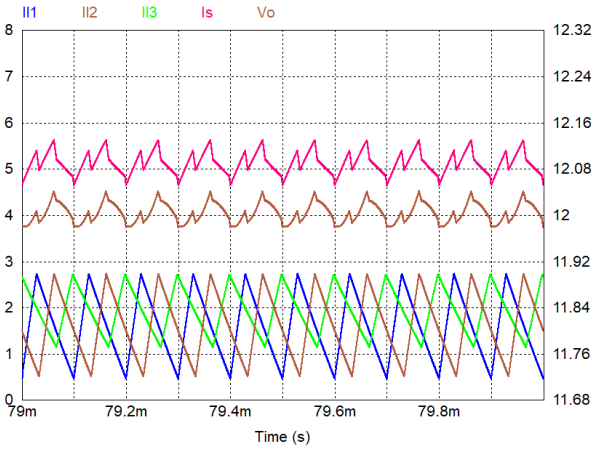

Figure 10. Steady-state operation with the PCC method: V_i=48 V, V_o=12 V, P_o=P_n/2. [Left vertical scale for currents: right vertical scale for the voltage].

When comparing the results in Fig. 9 and Fig. 10 with the ideal condition (in Fig. 6), it can be concluded that the same behaviour occurs regardless of the output voltage level: higher output voltage ripple and appearing at the switching frequency. The same changes happen when using the ACC method for $V_o = 12$ V.

3.2. Transient Operation

It was also simulated the transient operation of the converter with both current control methods: in Fig. 11 and Fig. 12 for the ACC the PCC method, respectively. In the two figures the load changes from $0.1P_n$ to P_n. For the transient operation it was allowed some overshoot in order to get a faster dynamic response.

The transient operation is very similar in both methods allowing to conclude that this factor is not relevant for choosing the more appropriate control method for this topology.

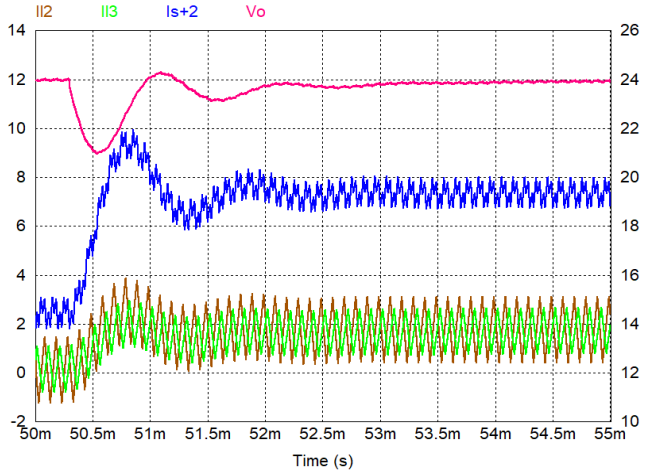

Figure 11. Transient operation with the ACC method from $0.1P_n$ to P_n, with V_i=48 V, V_o=24 V. [Left vertical scale for currents: right vertical scale for the voltage].

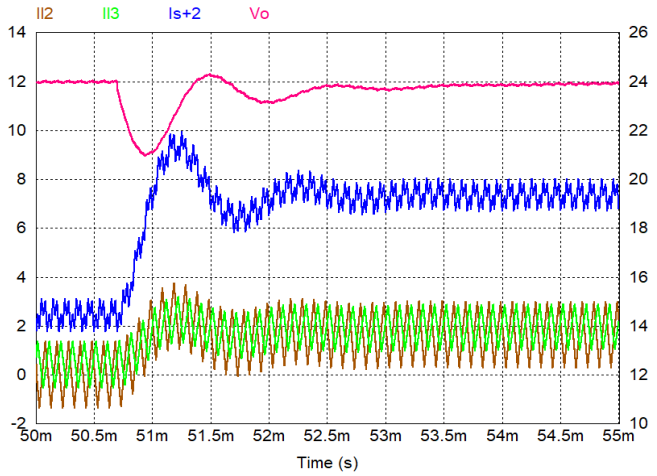

Figure 12. Transient operation with the PCC method from $0.1P_n$ to P_n, with V_i=48 V, V_o=24 V. [Left vertical scale for currents: right vertical scale for the voltage].

Load step changes of negative sign were also simulated but since the converter always operates in continuous conduction regardless of the control method the behaviour is the same.

Since the full converter is based on the parallel connection of equal elementary converters, it must have some degree of redundancy and fault tolerance capability. It is in fact the case and the control approach only needs small adaptations in order to maintain the advantages of ripple reduction in the input and output stages (the case of symmetrical interleaving).

In the case of failure of one single converter, the PWM signals of the remaining two only have to be reshaped, i.e. instead of a delay of $T_S/3$ between converters, it should be $T_S/2$ in the failure mode. In Fig. 13 is shown a simulation in the following conditions: PCC method, $P_o = P_n$, $V_i = 48$ V, $V_o = 24$ V, $L_1 = 430$ μH, $L_1 = 440$ μH, $L_3 = 630$ μH, converter 2 fails and recovers after some time interval.

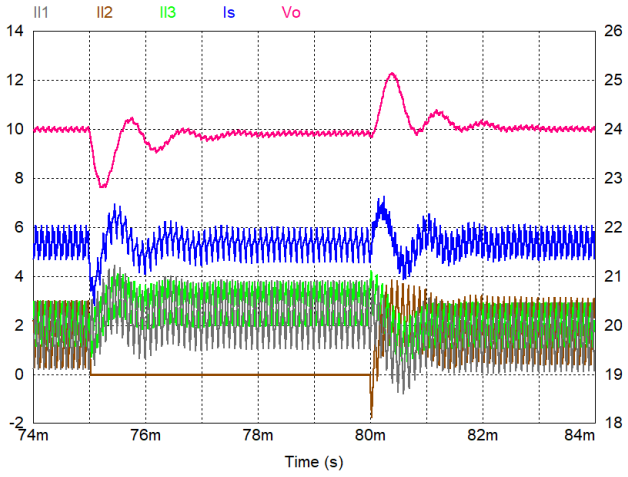

Figure 13. Fault tolerance operation: converter 2 is out of service between t=75 ms and t=80 ms. PCC method, V_i=48 V, V_o=24 V, P_o=P_n. [Left vertical scale for currents: right vertical scale for the voltage].

When converter 2 fails, and after a small transient, the two remaining ones take the total load current with an increased average value. Since the two converters in operation (1 and 3) have quite different inductance values, the equivalent output current maintains almost the same ripple it had before failure of converter 2. The transient is also propagated to the output voltage. When converter 2 recovers a similar transient is observed in the output voltage; the three converter currents return to their original shape before failure. It should be noticed that a similar behaviour is associated with the ACC method.

4. Experimental Results

An experimental set-up was built to validate and compare the two control methods, either in steady-state and transient operation; the main parameters are the same as in Table 1, but with the following inductance values (and loss resistance) already used in the simulations: $L_1 = 430\ \mu\text{H}$, $r = 0.9\ \Omega$; $L_2 = 440\ \mu\text{H}$, $r = 0.9\ \Omega$; $L_3 = 630\ \mu\text{H}$, $r = 1.2\ \Omega$. The controller digital implementation was made using a XMC4500 board.

4.1. Steady-State Operation

Figures 14 and 15 show the steady-state operation with the ACC method (with $P_o = 0.1P_n$ and $P_o = P_n$, respectively) while Fig. 16 and Fig. 17 provide the same waveforms for the same conditions but with the PCC method.

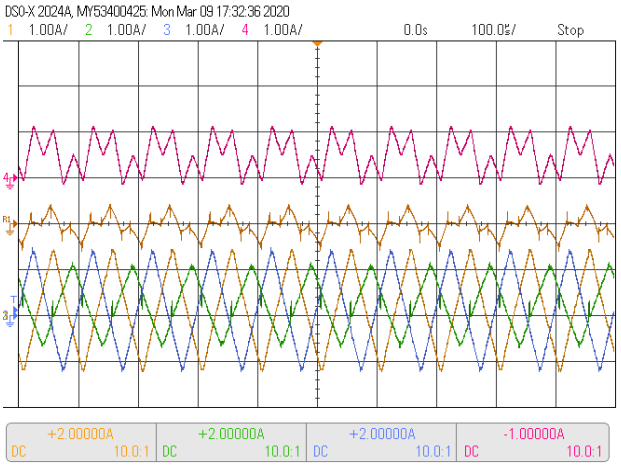

Figure 14. Steady-state operation using the ACC method with V_i=48 V, P_o=0.1P_n. [V_o=24 V and V_o: 0.1V/div, in brown color].

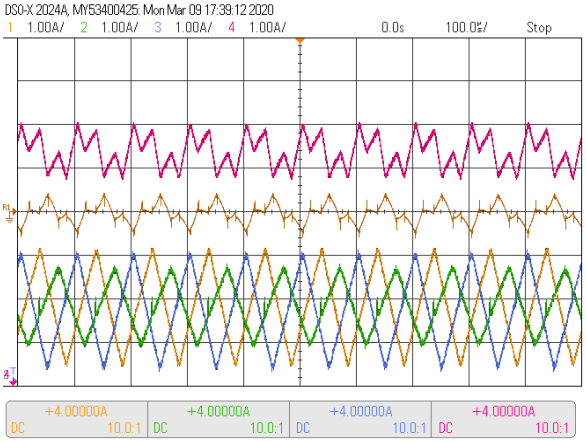

Figure 15. Steady-state operation using the ACC method with V_i=48 V, V_o=24 V, P_o=P_n. [V_o: 0.1V/div, in brown color].

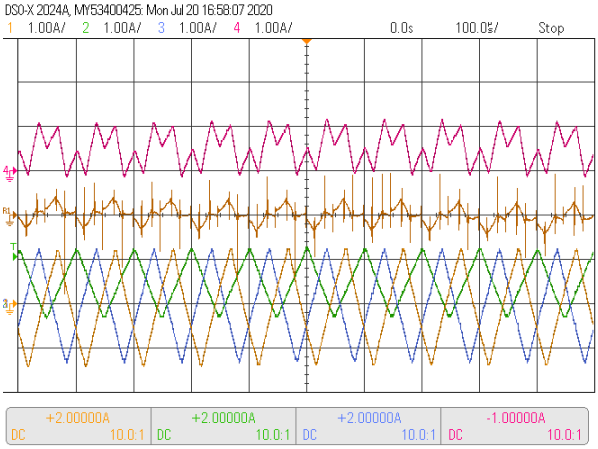

Figure 16. PCC method in steady-state operation with V_i=48 V, V_o=24 V, P_o=0.1P_n. [V_o: 0.1V/div, in brown color].

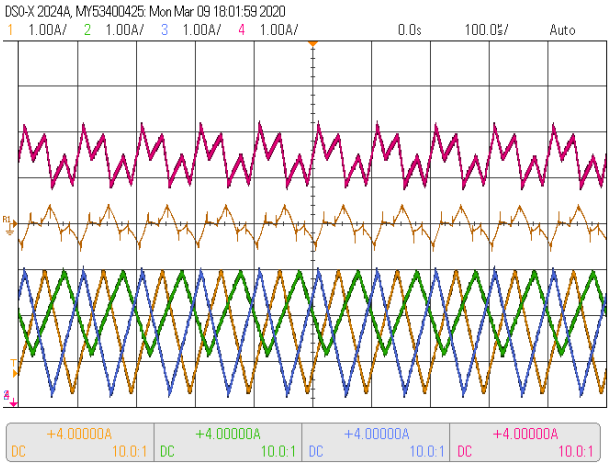

Figure 17. PCC method in steady-state operation with V_i=48 V, V_o=24 V, P_o=Pn. [V_o: 0.1V/div, in brown color].

The experimental conditions in Fig. 14 and in Fig. 16 were not shown in the simulation section due to space limitations; they are now presented to show that the converter behavior is the same in no load and full load operation. Due to synchronous switching it is not possible the discontinuous current mode, as can be verified in the two figures.

Comparing Fig. 15 with Fig. 8 for the ACC method and Fig. 17 with Fig. 9 for the PCC method, one can conclude that simulation and experimental results match with a very high degree of similarity.

In order to further validate the PCC method, Fig. 18 shows the steady-state operation in the following conditions, the same as those in Fig. 10: $V_i = 48$ V, $V_o = 12$ V, $P_o = P_n / 2$, $F_s = 10$ kHz. Again, apart some noise in the output voltage, there is a high matching degree between simulation and experimental results.

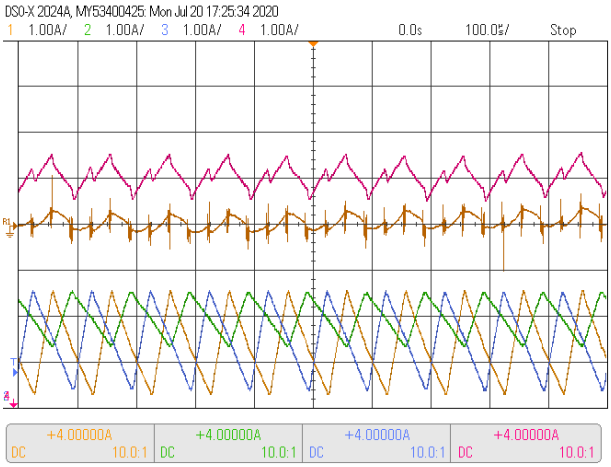

Figure 18. PCC method in steady-state operation with V_i=48 V, P_o=P_n/2. [V_o=12 V and V_o: 0.1V/div, in brown color].

4.2. Transient Operation

The dynamic operation of ACC and PCC methods is demonstrated in Fig. 19 and Fig. 20, respectively. As in the simulation results section, the applied load varies from $P_o = 0.1P_n$ to $P_o = P_n$.

The experimental transient operation of the converter when controlled by both methods matches very good the one shown in simulation environment; in this case, comparison is made between Fig. 19 and Fig. 11 for the ACC method and between Fig. 20 and Fig. 12 for the PCC method. As discussed in the simulation section, the same transient behaviour applies to negative load steps.

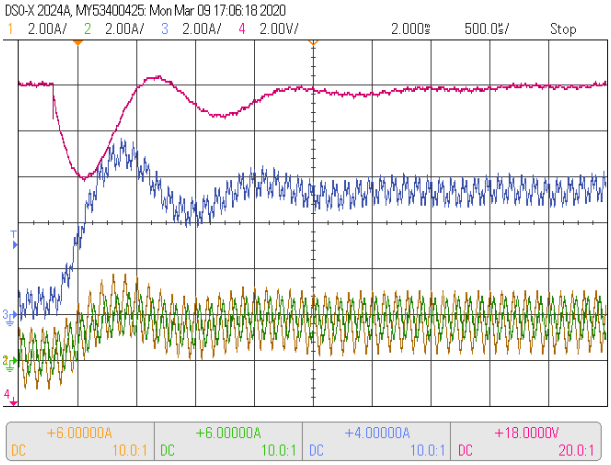

Figure 19. Transient operation with the ACC method with V_i=48 V, V_o=24 V, and a load change from 0.1P_n to P_n. [V_o with an offset of 10 V].

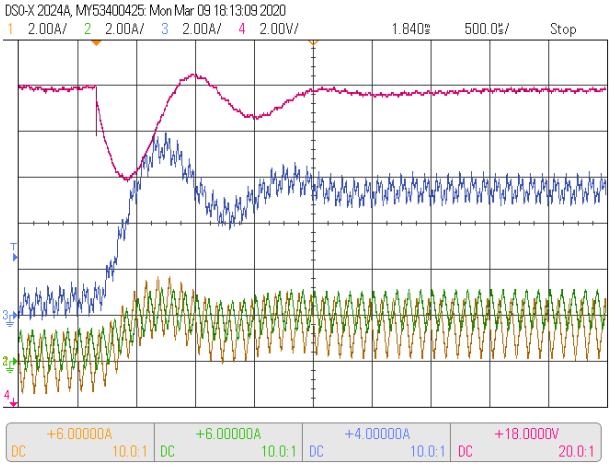

Figure 20. Transient operation with the PCC method with V_i=48 V, V_o=24 V, and a load change from 0.1P_n to P_n. [V_o with an offset of 10 V].

5. Conclusion

Multiphase dc-dc converters offer several advantages over conventional ones: fail-safe parallel operation between the modules, reduced input current ripple and output voltage ripple, small passive components sizing. Current sharing between the sub-modules can be implemented under several approaches. This paper compared, using simulation and experimental results, with large asymmetries between the sub-modules, the average current control and the peak current control methods.

It is concluded that they offer almost the same steady-state and transient characteristics. The controllers digital implementation is somewhat more elaborated in the ACC method but this is not enough to rank it better.

Acknowledgments

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