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Design and Performance Analysis of a Low Jitter Charge Pump-Phase Locked Loop Architecture and Loop Filter in CMOS Process

Journal of Electrical Systems

Abstract: - Phase-locked loop technology has made a substantial contribution to the development of communication and data transmission technologies. Moreover, several recent studies in phase-locked loop systems and state-of-the-art IC technology makes phase-locked loop devices essential system components. For usage in Phase Lock Loop (PLL) systems, a circuit for a tri-state charge pump and a circuit for a low pass filter of second order were devised. The non-ideal effects, such charge sharing and current mismatch, are lessened by the suggested design. It could be reduced by giving the two switches UP and DOWN equal values. Conversely, the outcome of low pass filter condition is found by the charge pump's output. The suggested design has been simulated. We used Cadence TM Spectra for our simulations. The charging or discharging curves of the load capacitor exhibit a clear rise in slope in between the condition of pump up and pump down, as demonstrated by the simulation results.

Keywords: Phase Lock Loop, Tri-state Charge Pump, Current Mismatch, Charge Sharing, Complementary Metal Oxide Semiconductor.

I. INTRODUCTION

Charge pumps are used as key component in phase locked loop, switched-capacitor circuits, Analog to Digital and Digital to Analog converters, and DRAM circuits. CP circuit in the PLL system have two switches of transistor, generating I_{UP} and I_{DW} current pulses that control the VCO and control the capacitor's voltage. Three major concerns of CP circuits are area, power, and output voltage ripple [1]. A fluctuation in output voltage affects the working of the circuits that the CP is providing power, hence in most conditions, a low output fluctuation is required. Moreover, the extreme power efficiency of the CPs eliminates the advantage of scaling down the supply voltage and, consequently, makes it unsuitable for portable applications. Finally, more area- efficient is better because a smaller chip area is always cheaper to fabricate. Among the various types of PLL, the charge-pump is usually used in today's wireless technology. Since different system designs benefit from the phase lock's advantages, this type of PLL has a bigger gain, larger range acquisition [2]. It was programmed, which allows satisfying the modern RF system's needs reconfigurable to different protocols and standards [3,4]. Phase Frequency Detector (PFD), Charge Pump (CP) and Loop Filter, and Voltage Controlled Oscillator (VCO) are the three main components of the Phase Lock Loop (PLL) system [5,6]. Since a PLL is a feedback loop that works inside a single chip and approach the Fout from the given F_{div}, it is highly preferred. PLLs are typically utilized in high- performance wireless, well-timed clock generators, signal recovery from noisy communication channels, and other PLL-related applications [7]. A PLL system's fundamental block diagram is shown in Figure 1.

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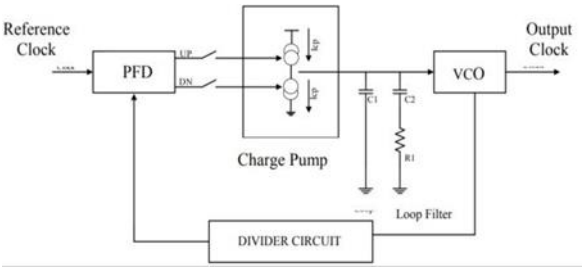

Figure 1: PLL Block Diagram

In the sphere of data communications, the phase locked Loop is also utilized as a clock recovery device since it reduces the skew of the external frequency source [8]. During the PLL design phase, CP-PLL design was used to overcome the problem of signal skewness. This architecture has a large frequency, low jitter, and having less loop locking time, and it has been frequently implemented in discrete form [9,10]. These characteristics would make CP-PLL very useful in high-performance integrated circuits. Furthermore, CP-PLL has been gaining popularity as a trend study due to technical improvements and needs for integrated devices with high packing density, fast speed, and low power [11]. The jitter parameter should be the focus of study for the CP-PLL. Jitter is the discrepancy between the jitter refers to the small, unintended variations or fluctuations in the timing or amplitude of signals, typically caused by factors such as noise, interference, or imperfections in the circuit components. instances where the setup and hold requirements are not met in digital circuits may result from the PLL's waveform's deviation of zero crossings. Additionally, the chip's overall functionality is compromised by instances where the setup and hold requirements are not met. Which result in data transmission mistakes [12,13]. Because of its severe influence on PLL quality, jitter is therefore important to PLL research [14].

II. Challenges with Charge Pump PLL Design

Within a PLL design, the CP is built using integrated circuit technology, which includes an on-chip capacitor and pull-up and pull-down transistors. PFD outputs signals, which function as switches to turn on and off the respective signals when UP is on [15,16]. Only one way is possible with it. A low-pass filter is an electronic circuit or signal processing technique that allows signals with a frequency lower than a certain cutoff frequency to pass through it while attenuating (reducing the amplitude of) signals with frequencies higher than the cutoff frequency. It is constructed with a resistor and capacitor. The capacitor is a reactive component. current naturally flows through the path of least resistance. Consequently, when dealing with high-frequency signals in a circuit, the capacitor, symbolizing minimal resistance, becomes predominant [17,18]. Accurate zero input phase error characterizes an ideal CP-PLL model; nevertheless, real circuits introduce some phase error due to mismatch. This shows a direct relationship of the phase inaccuracy of the entire PLL system and the matching accuracy of CP. The switch induced error voltage affects the accuracy of Analog to Digital, Digital to Analog converters, capacitor filters. Non-ideal behavior of charge pump can considerably contribute to PLL output jitter [19,20, 21].

2.1 Integration Issues

Since charge sharing, charge injection, and clock traversal are the main causes of non-idealities in MOS analog switches, switch sizing of transistor is a crucial design variable to optimize the performance of CPs [22, 23].

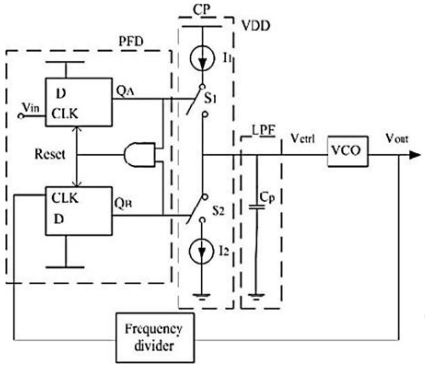

Figure 2: Conventional CP-PLL architecture

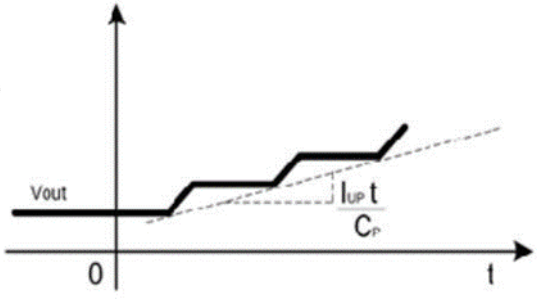

Figure 3: Step response of CP-PLL architecture

The correlation among V_{ctrl}, I_{UP}, I_{DW} and phase difference ΔΦ can be fixed from the dynamic behavior of CP-PLL [9].

$$V_{ctrl}(t) = \frac{I_{UP}T_{in}}{2\pi C_P}\Delta\phi = \frac{I_{UP}\phi_0}{4\pi f C_P} \quad (1)$$

The Equation (1) elaborate that V_{ctrl} increases in steps in proportionate to the ratio I_{UP}/C_P. For example, if Cp = 5pF, I_{UP} = 10uA, and the clock frequency is 10MHz, the voltage step size that arises is 100mV. Equation 1 indicates that doubling I_{UP} should cause the slope of the V_{ctrl} vs. t curve to double, generating a 200mV voltage step height (Figure 3). As a result, we can utilize this behavior to modify the degree at which the capacitor filter is being charged/discharged [24, 25]. Put another way, we can adjust the PLL system's speed response by using I_{UP} current as an additional variable control.

2.2 Tri-state Charge Pump Circuit

The low current consumption of a tri-state charge pump is generally attributed to its dependence on the PFD's frequency (Figure 4).

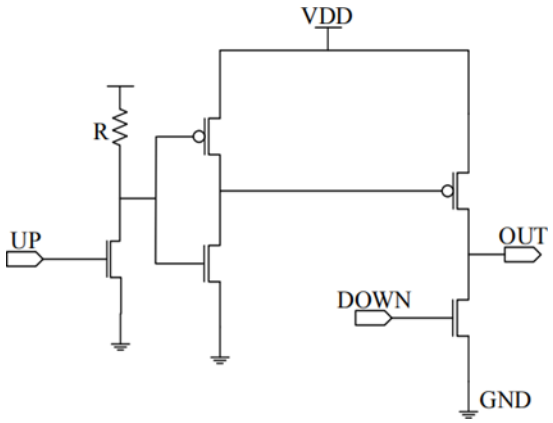

Figure 4: Tri-state Charge-Pump

One amplifier, one inverter, and five transistors make up this tri-state charge pump. The charge pump into the filter is also low when the input is low. An amplifier was introduced, depicted in Figure 4, positioned between the UP switch and the inverter, aiming to boost the amplitude of both voltage and current signals within the circuit. To neglect current mismatch in the proposed charge pump circuit, equivalent values for switches UP and DOWN are provided. The supply voltage used in this circuit is 1.2 V. As indicated in Table 1, the delay assigned for switching UP and DOWN is 100 ps and 500 ps correspondingly. A PLL system's loop filter must be carefully selected to avoid locked loops being unlocked because of incorrect values and minute changes in the data input. The primary purpose of the low pass filter of second order employed in the loop filter is to filter out noise and then transform the current produced by the CP converted a voltage signal for the VCO as input [26,27]. To stabilize the loop and get rid of the charge pump's high frequency signal component and noise, a loop filter is employed[28].

TABLE 1: Parameters for UP and DOWN Switches

Parameters	**Switch UP**	**Switch DOWN**
DC Voltage (v)	1.0	1.0
Voltage 1 (v)	200m	200m
Voltage 2 (v)	1.0	1.0
Delay (s)	100p	500p
Rise Time (s)	10p	10p
Fall Time (s)	10p	10p

Pulse Width (s)	5n	5n
Period (s)	1n	1n

III. PROPOSED CHARGE PUMP ARCHITECTURE IN CMOS PROCESS

In PLL systems, tri-state charge pump has also utilized. Do not have a lot of charge pump architectures. Consider a traditional tri-state, which has three switch topologies for the source, gate, and drain. The lower current consumption of this kind of charge pump is contingent upon the PFD's frequency.

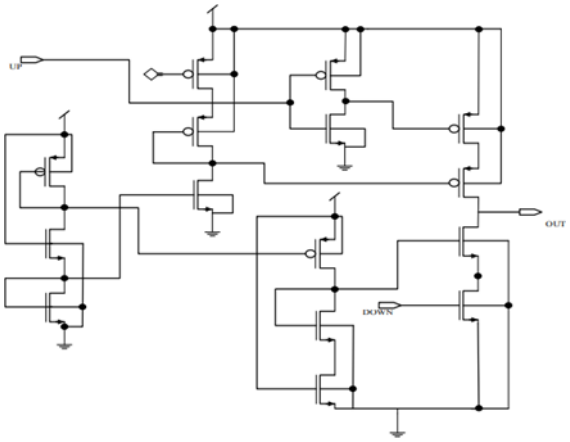

Figure 5: Transistor Level diagram of a Charge Pump

Following appropriate biasing is within the topologies, the output voltage increased between 0.5 and 2.5 volts with a 3-volt supply. The important and crucial conceptual depiction of a CP circuit with adjustable magnitude currents I_{UP} & I_{DW} is displayed in Figure 6. Switch S1 and switch S2 with the transistors MB1, MB2, MB4, MB5, and MB7 form a traditional Charge Pump circuit. I_{UP} & I_{DW} current is set by MB1 via a current source that consists of MB2, MB4, and MB5 (MB5 and MB7). Enable switches are used to give the CP circuit the choice to drive an alternative I_{UP} & I_{DW} current (Figure 6). The fundamental working principle is as follows: transistor MB6 goes ON and the "enab_b" switch closes when an enable signal is assigned. The charging speed of the filter capacitor doubles if MB6 and MB7 have equal sizes because the I_{UP} current doubles. This is also true for the complimentary portion, that is, I_{DW} tripling current upon turning on MB3 by shutting "enab." Transistors MB1 and MB2 make up the "enable" switch, whereas MB3 and MB4 make up the "enab_b" switch.

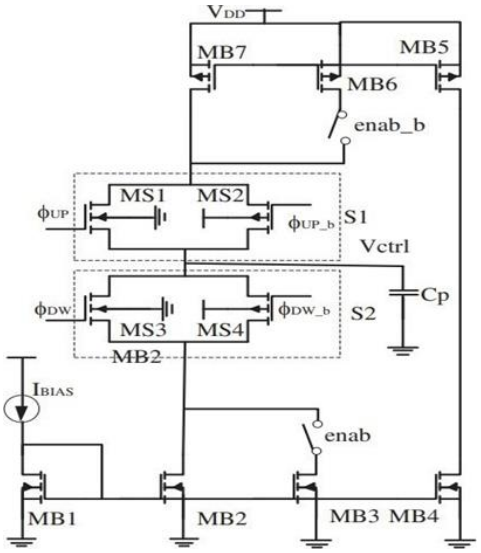

Figure 6: Conceptual illustration of a CP circuit used to drive various I_{UP} and I_{DW} currents

The deployment of Transmission Gate topology for switches S1 and S2 aims to mitigate injection current and clock feedthrough concerns. Ultimately, this circuit connects the charge pump, phase frequency detector, low-pass filter, and divider. In our suggested design of the CP-PLL in Figure 6. Transfer function of this circuit is determined by the expression in Equation (2).

$$CPPLL(s) = K_{PFD} \times K_{VCO} \times \frac{s + \frac{1}{R_0 \times C_0}}{C_1 \times s^2 \times \left(s + \frac{C_0 + C_1}{R_0 \times C_1 \times C_2}\right)} \quad (2)$$

Where, K_{PFD} = PFD Gain

K_{VCO} = VCO Gain

C1, C2 = Capacitance of Loop filter

R1, R2 = Resistance of Loop filter

The lack of a model to accurately quantify the circuit's properties has forced the circuit designer to develop and investigate novel designs through a variety of simulation and optimization techniques. Three main tasks comprise the process of designing analog circuits: (1) choosing the topology; (2) sizing the components; and (3) ensuring that the cells fulfil specifications. The design time increases in tandem with the circuits' complexity.

IV. RESULTS AND PERFORMANCE ANALYSIS

Following the design phase, the parameters of the suggested CP-PLL are shown and examined in this part. The Spectra tools carry out the intended CP-PLL's simulation process. The simulation environment vigilantly considered while examining CP-PLL optimization, taking into account changes to both the input and output of the CP-PLL. The testbench circuit selects the following input parameters to be combined with: the operating voltage is 1 V, the temperature is 27^0C, and the input oscillator is 20 MHz Additionally, simulation outcome examines important parameter variations like jitter, output voltage, and operating frequency. Using the capacitance load C_{load} (2 femtofarad, 5 femtofarad, 6 femtofarad, 7 femtofarad, 8 femtofarad, 9 femtofarad, 9.5 femtofarad), and the risetime and fall time of the input signal V_{slope} (0.01 nanoseconds, 0.02 nanoseconds, 0.04 nanoseconds, 0.06 nanoseconds, 0.08 nanoseconds, 0.09 nanoseconds, 0.095 nanoseconds). However, in many instances, these simulation models can evaluate the CP-PLL's quality, which is essential for designing CP-PLL for real-world use. Simulations is being conducted using a 0.5µm spectra simulator from cadence TM. Figure 7 shows the aberration between the voltage levels of the F_{ref} and F_{div}. Figure 8 shows the output voltage of the PFD. A closed-up view of I_{UP} current levels during the pumping-up phase is shown in Figure 9. The step sizes of V_{ctrl}, which double when I_{UP} doubles, are in great deal with the model provided by Equation 1. In Figure 10 and Figure 11 shows alike characteristics that have noted during the pumping-up and pumping-down period. Moreover, the readings of a steeper slope validate this technique.

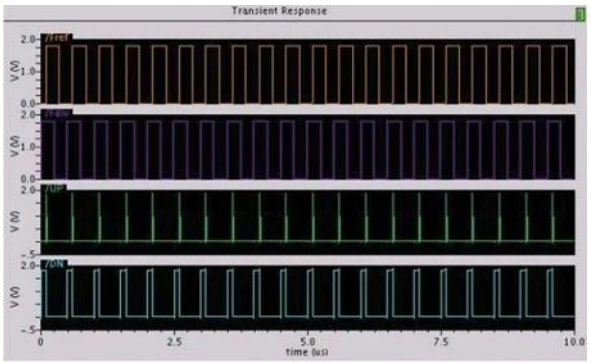

Figure 7: PFD When F_{ref} is leading

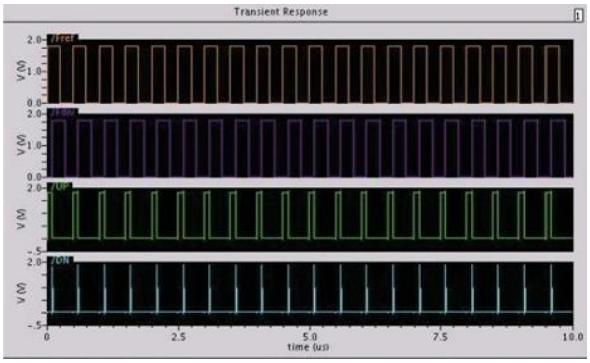

Figure 8: PFD When F_{ref} is lagging

Figure 9: Current(I) in CP between UP and DOWN

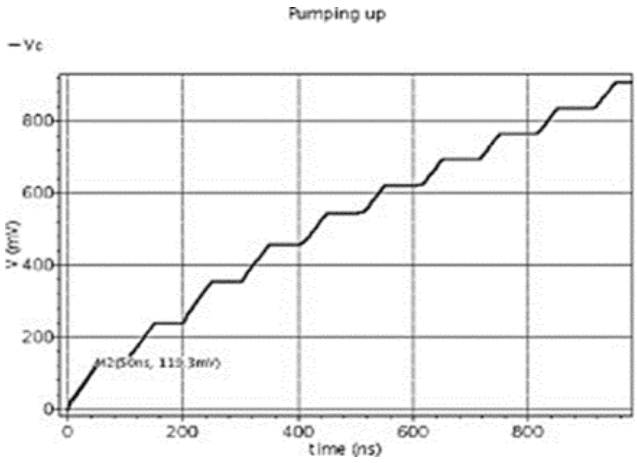

Figure 10: Phase Frequency Detector- Charge Pump in pumping-up

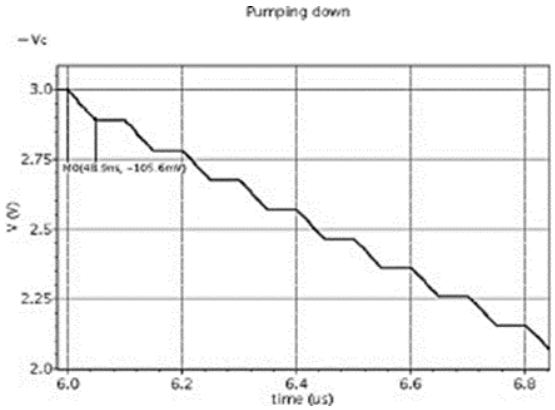

Figure 11: Phase Frequency Detector- Charge Pump in pumping down

V. CONCLUSION

This research has led to the development of a novel high-performance CMOS charge pump design tailored for phase-locked loop synthesizers. Utilizing Cadence tools in 130nm CMOS technology, a tri-state charge pump paired with a second-order low-pass filter is being designed. The power and frequency requirements are met by the suggested design. The test findings indicate that the charging and discharging rate of the filter capacitor can be adjusted by selecting the I_{UP} & I_{DW} current by the addition of an enable switch to the conventional charge pump circuit. The suggested CP features a high as such, it lends credence to the notion that the dynamic output power in CP-PLL design can be reduced. Furthermore, these output voltage values may be use in many designs that rely on a low threshold voltage for activation. Carefully designing these parameters will enable it to drive load circuits while securing the PLL's dynamic power. matching precision and a broad current match range. High-performance CP-PLLs can use this CMOS charge pump architecture.

ACKNOWLEDGMENT

We would like to thank the departments of doctoral studies in Integral University for providing the Manuscript Communication number **IU/R&D/2024-MCN0002669**. This unique identification number makes it easier to track and communicate of our research as it moves through the publication process. We would also like to express our sincere thanks to everyone who helped us to build this work.

CONFLICT OF INTEREST

The author declares that there is no conflict of interest regarding the publication of this manuscript.

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