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Enhanced Low Power Carry-Select Adder using Transmission Gate Logic

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Abstract: - Power reduction strategies are becoming increasingly significant in low power VLSI applications. A digital circuit called an adder is utilized in numerous applications, such as DSP and microprocessors, to execute addition operations. This work presents the design of a low power XNOR gate that utilizes transmission gate logic and is implemented in Carry Select Adder for low power VLSI applications. Simulation is performed using Tanner tool at 180nm technology. Power, latency, and layout area were among the performance metrics that were compared to the circuits that were already in effect. It has been determined that the current approach offers a notable improvement in terms of power and speed when compared to the current designs.

Keywords:Carry Select Adder; Power; Latency; Transmission Gate; Area.

I. INTRODUCTION

The adder core is the most crucial part of microprocessors and digital signal processors. Three inputs, two outputs (sum and carry), and two outputs are usual for a 1-bit complete adder core. Multipliers work together to produce complex arithmetic circuits, such as those for division, multiplication, and subtraction operations. The entire arithmetic system is affected by the performance of an adder. The development of low-power VLSI systems has gained popularity recently because to the quick advancement of computation and mobile communication technologies. Battery technology is not developing at the same rate as microelectronics. Thus, designers face additional hurdles when it comes to low power consumption, limited silicon space, high throughput, and quick speed. Thus, there is a lot of interest in creating adder cells with good performance at cheap power. This study presents an organized method for adder design analysis. Its foundation is the division of the full adder into smaller components. These modules are all implemented, tuned, and tested independently. The CMOS logic design method is being employed to create high-performance circuits. In order to outperform designs that employ a single logic style, this design-type concurrently takes advantage of the best aspects of several logic styles.

Furthermore, because there are fewer connecting wires and complementary transistor pairs, the complementary CMOS circuit structure is easy to use and effective by means of area. A different type of adder is the 32-transistor Complementary Pass Transistor Logic (CPL) with swing restoration. The CPL adder generates a large number of intermediary nodes and their corresponding outputs. The most important aspects of CPL are its low swing internal node and short stack height, both of which contribute to lower power consumption. The CPL employs static power as a result of the low swing at the output inverters' gates. Double Pass-Transistor logic (DPL) and Swing Restored Pass-Transistor logic (SRPL) are related to CPL. The CPL is where the SRPL style originated. This latch structure, which simultaneously handles output buffering and swing restoration, is cross-coupled to the output inverters. SRPL gates only function satisfactorily in extremely specific circuit configurations due to their extreme sensitivity to transistor size. It switches slowly, can't drive an output well, and has high short-circuit currents. Circuit types such as LCPL and SRPL are utilized to reduce the power consumption of CPL circuits. Double pass-transistor logic, or DPL, employs complementary transistors to maintain full swing functionality and reduce DC power usage.

As a result, no restoration circuitry is required. The enormous space required by DPL because of the pMOS transistors is one drawback. One particular type of pass-transistor logic circuit is the Transmission Gate (TG)

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logic circuit. There are 20 transistors in a TG gate full adder cell. The full adder has several concerns, including performance, noise immunity, area, power consumption, regularity, and good driving ability. Based on output, all full adder circuits can be split into two groups. The building of the first set of full adders is full swing. TG, TGA, C-CMOS, CPL, 14T, and 16T are in the first category. Full adders (10T, 9T, and 8T) without full swing outputs make up the second category. This full adder often uses less power and takes up less area because it contains fewer transistors. When creating larger circuits, the second group of non-full swing full adders can be used as multipliers and adders with multiple bit input.

II. RELATED WORKS

The adder cell consisted of three main parts. The first module is required in order to generate the XOR and XNOR routines. One way to do this is to first create the XOR function, and then use an inverter to produce the XNOR function. As far as the authors are aware, six transistors is the lowest number that has been used. Because it is believed that designs with more transistors won't be competitive for low power, a maximum of ten transistors is enforced. In Figure 1, three inverters and two transmission gates make up the first module. It is the one that TG-CMOS utilizes.

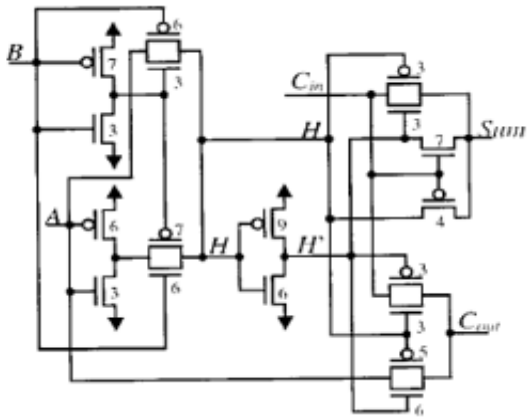

Figure 1. 1-bit CMOS full adder cell.

The first module's outputs load the second and third modules' inputs. This load consists of gates and sources/drains of transmission gates. The average load is calculated using the actual designs that were used for the second and third modules. Three transistor gates and one transistor source/drain that each must drive are averaged to determine the load. Considering the inputs H and H' (generated by the first module, Cin, this module must produce the total. Most of the designs provided here are the same as those used in the first module. Enough power to drive the following gates is a critical requirement for this module. For certain cells, the outputs of the primary module (H and H') may not be pure signals are what drive the inputs of this module. Thus, it was determined to control the module's inputs using these real outputs in an attempt to provide accurate simulation results. Because it is the sole module with the fewest transistors and no power supply or ground rails to allow for the prevention of short circuit current, it has the lowest average power consumption.

In order to generate Cout given H, H, A, or B as inputs, the third module is necessary. Similar to the second module, supplying adequate driving power is necessary to load the next gates. The method employed by all widely used adders to create the Cout—a multiplexer that passes either A, B, or Cin—depending on the value of H—is the same. With these inputs, it appears to be the only device that can produce Cout with just four transistors. Other configurations will require two additional transistors, or the complement of Cin, for a total of six transistors. Eight transistors are needed for other designs. Thus, it was determined that the third module would only use this architecture. It is seen in Figure 1. Since either of the input signals A or Cin will pass, the driving power of the signal relies on them. It also relies on the size of the transistors utilized in the transmission gates. A or Cin be the outputs of an earlier cascaded adder cell, the Cout n signal will not have enough driving power as a result of these signals decaying. Therefore, circuits where a latch or buffer follows the outputs of the adder cell are advised to utilize this design.

III. PROPOSED METHODOLOGY

A. Modified XNOR Module

Three blocks indicate the 1-bit full adder. The output carry signal (Cout) is produced by Module 3 of the XNOR modules, whereas Modules 1 and 2 supply the sum signal (SUM). By designing each module independently, the total adder circuit's power, latency, and space are maximized. The XNOR module is responsible for the majority of the power used by this hybrid 1-bit full adder circuit. Consequently, this module is designed to minimize power consumption while averting the possibility of voltage degradation.

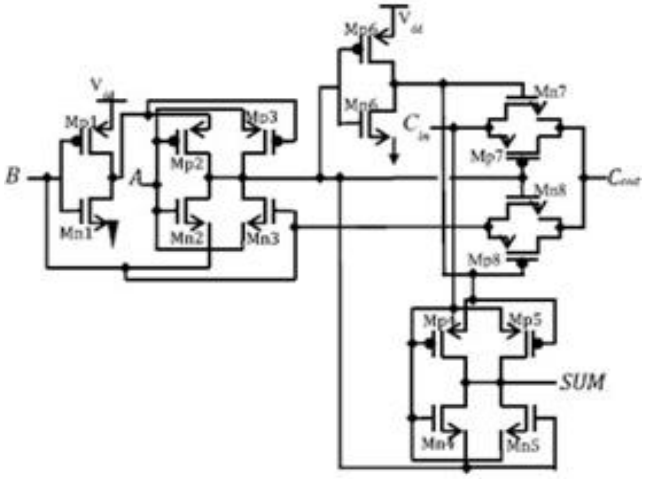

Figure 2. Modified XNOR circuit

The redesigned XNOR circuit is shown in Figure 2, where the intentional use of a weak inverter—a transistor combination made up of transistors Mp1 and Mn1—significantly reduces power usage. Level restoring transistors Mp3 and Mn3 ensure full swing of the output signal levels. Four transistors are used in the XOR/XNOR, but the logic swing is reduced. In contrast, the XOR/XNOR employs six transistors in order to achieve a higher logic swing than the 4 T XOR/XNOR. Although the transistor layout for the XNOR module differs from that of the 6 T XOR/XNOR, it still uses 6 T in this work. In comparison to 6 T XOR/XNOR, the improved XNOR described in this work offers low power and great speed.

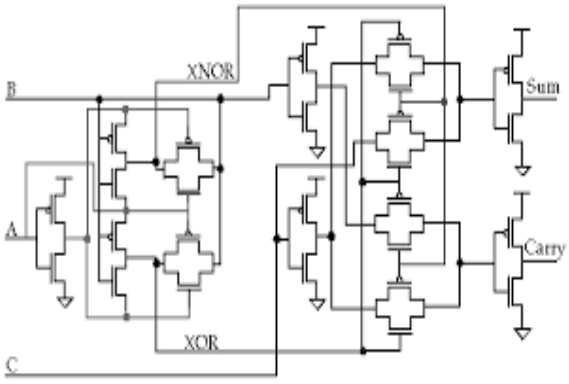

Figure 3. Transmission gate based full adder

Building on the half-adder circuit, Figure 3 depicts the full adder circuit that uses transmission gates to enable us to add two single-digit binary integers together and obtain a result. Three basic logic gates—an OR, an AND, and an XOR gate—make up the entire adder circuit. The complete spectrum of two-input actions is possible because each of these gates is coupled to two inputs. The final total bit is then obtained by combining the outputs of the OR and XOR gates. An electrical switch known as a transmission gate is used to either selectively allow or prohibit signals. It consists of two gates: one that allows switching to occur and another that prevents it.The signal flows through while the gate is activated and is blocked when it is disabled. There are various benefits to building

a full-adder circuit with a transmission gate. First of all, it does away with the requirement for extra parts like relays or transistors. Second, by shortening the signal path, power consumption is decreased and response times are improved. Thirdly, it enables more effective design and quicker switching processes. The full-adder circuit with transmission gates has several useful benefits, but it can also make design easier. A circuit's complexity can be decreased while maintaining the intended functionality by doing away with the requirement for additional components.

B. 8-bit Ripple Carry Adder

As illustrated in Figure 4, an enlargement of the hybrid 1-bit full adder is built as an 8-bit ripple carry adder. In this non-carry look-ahead adder arrangement, the carry propagation continues all the way to the last adder block. Stated otherwise, a ripple carry adder is a logic circuit in which the carry out of each full adder is equal to the carry in of the next, most significant full adder. Before the sum and carry out bits of that stage are valid in this adder, the carry in of a half adder stage must occur. A propagation delay within the logic circuitry is the reason of this. The propagation delay is the amount of time that elapses between applying an input and the corresponding output occurring.

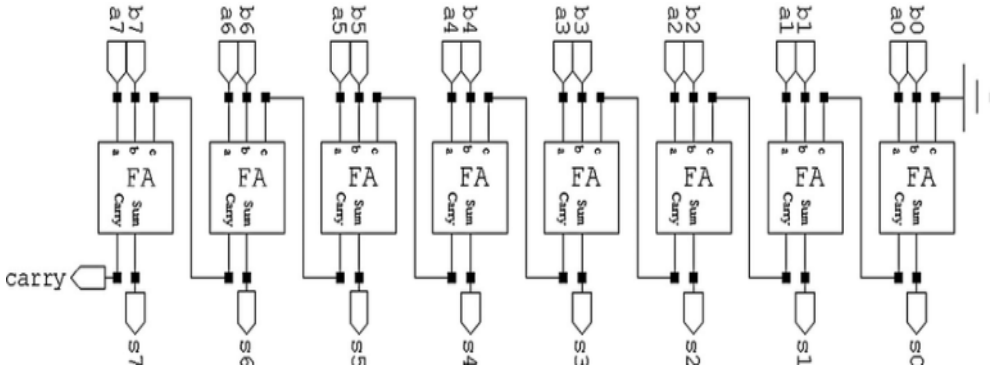

Figure 4. Ripple Carry Adder

C. Carry Select Adder using Transmission Gate based XNOR Gate

A key component in lowering the carry propagation time is the carry-select adder. One for a logical zero input carry and another for a logical one input carry. To expedite execution, the carry-select adder supplements the ripple-carry adder with conjecture or prediction. It computes the top bits differently from the bottom bits, which are computed in the same way as by the ripple-carry adder. According to Figure 5, the 4 bit addition operation is carried out based on the input signal zero (or) one. Adders are then chosen, and ultimately, line output total and carry are generated concurrently based on multiplexer select line. As a result, the carry select adder's operating speed rose at the expense of twice as much area.

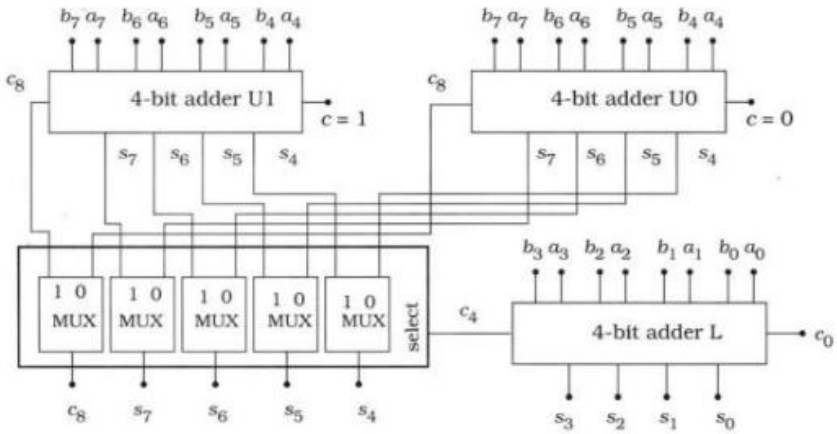

Figure 5. Carry Select Adder

IV. RESULTS AND DISCUSSION

The implementation of the proposed work is done using Tanner tool at 180nm technology and the output waveforms are shown in Figure 6 and 7.

A. Simulation output of XOR using Transmission gate

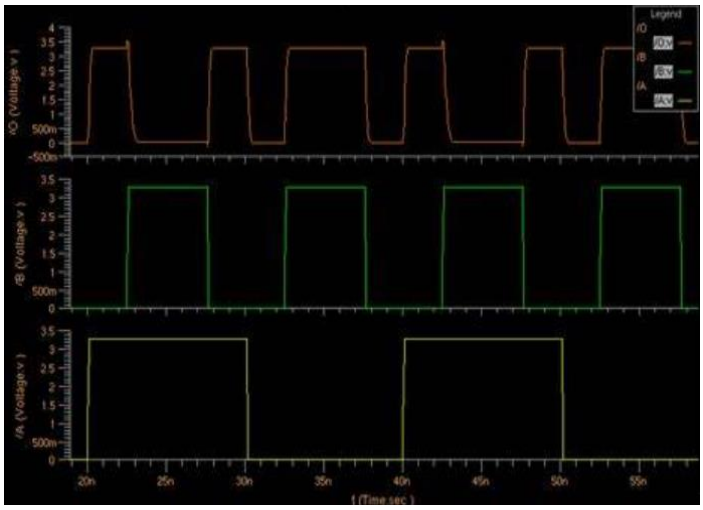

Figure 6. Output waveform of XOR gate using transmission gate logic

B. Simulation output of Full adder using Transmission gate

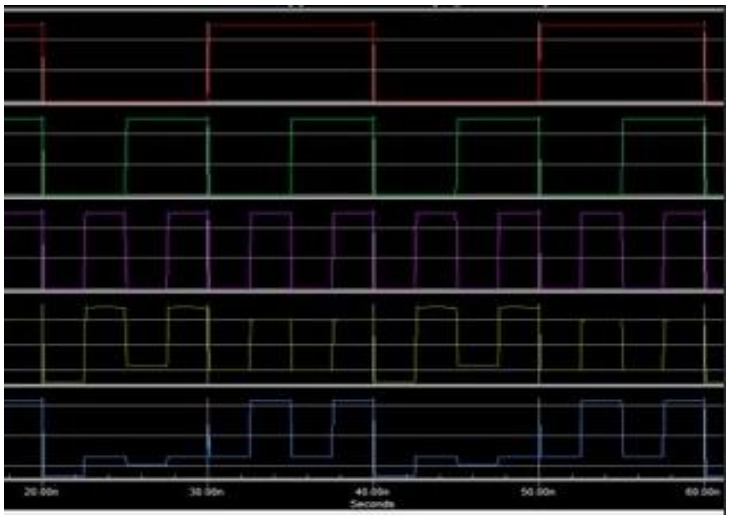

Figure 7. Output waveform of full adder using transmission gate logic

Table 1:Comparison of adders using transmission gates

Design	Area	Power (mW)	Delay (ns)
CMOS Full adder	1792	38	1.918
Full adder using transmission gates	1376	24	1.84
Carry select adder using transmission gates	1123	12	1.62

The findings of transmission gate based carry select adder design shows that the performance parameters such as area, power and delay are reduced. Also, full adder using transmission gate provides better performance when compared to the existing designs of full adder design as shown in Table 1.

V. CONCLUSION

A low power consumption 8-bit carry select adder has been proposed in this work. Using Tanner, the simulation was done and the results were compared to the full adder design that was at the time. The outcomes of the simulation demonstrated that, contrasted with current full adder, the proposed adder provided better PDP. The proposed full adder uses an average of 24 mW of power, which is substantially less than the 38 mW of power used by the current full adder. The carry select adder operates faster when fewer transistors are used. Since average power consumption and propagation delay are reduced, the PDP of the proposed carry choose adder is significantly higher than that of the full adder.

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