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Reduced Switch Count Seven Level Inverter Topology for Standalone Applications.

Abstract: - Recently, multilevel inverter (MLI) topologies gaining their popularity because of compact size, lower (dv/dt) stress, higher efficiency, and lower THD. But they are having limitations in using more devices, capacitors, and complex control. This paper presents a seven-level inverter topology with a reduced number of switches and inherits the principle of the switching capacitor technique for voltage level boosting. This proposed topology has the property of the self-balancing of capacitors. This inverter topology is controlled with the level shifted PWM technique. Dynamic performance of the topology is also addressed. The proposed circuit is also distinguished from conventional MLIs in terms of the number of components used like switches, diodes, capacitors, losses, and THD. Simulation results of the proposed circuit is validated with the help of MATLAB/Simulink.

Keywords: Multilevel Inverters (MLIs), Switched Capacitor (SC), Pulse Width Modulation (PWM), Total Harmonic Distortion (THD).

I.INTRODUCTION

Usage of non-renewable resources like coal, oil, gas in various applications like power generation, transportation causes pollution in our environment. Environmental pollution is becoming a serious problem in recent years. So, people around the globe are looking towards the renewable energy sector. Solar PVs, wind energy systems, and other types of renewable energy sources (RES) are emerging into the power generation sector to replace the position of fossil fuel-based power generation. Conventional fuel vehicles are also replaced by electric vehicles (EVs). These technologies are rapidly developing because of advancements and developments in the power electronics area.Inverters play an important role in above-mentioned applications [1].

Multilevel Inverters (MLIs) are broadly classified into the following types. [a]Neutral point clamped MLI(NPC), [b]Flying capacitor MLI(FC), [c]Cascaded H Bridge MLI(CHB) [1].

Due to the availability of individual dc sources, CHB is primarily used in the renewable energy sector, such as solar PVs, whereas NPC is primarily used in the adjustable speed drives domain. The main drawback of flying capacitor MLI is that, having a greater number of capacitors and their balancing. Power electronic components like switches, diodes and auxiliary circuits like gate drivers and heat sinks have become more prevalent as output voltage levels have increased. Thus, decreased switch count topologies have gained popularity during the past few years. [2-3].

Solar PVs are unable to generate maximum power at all times. To overcome this problem DC-DC boost converters or inverters combined with transformers were used traditionally. Both practices will increase the size and cost of the system. To encounter this problem, the switching capacitor technique becomes a solution. The boosting characteristic in switched capacitor based topologies is produced by charging the capacitors in parallel with the input dc voltage and discharging them in series. The larger output voltage is the consequence of connecting several switching capacitor units in series, either with or without a supply voltage.SC-based technologies easily bypass the boosting problems [4].

Due to lower THD in output voltage and boosting gain utilising a smaller number of switches, switched capacitor (SC) based MLIs are becoming an attractive alternative solution. Several SC based MLI topologies are addressed in literature.

This paper is presenting a reduced switch count seven level inverter topology for standalone applications. This topology consists of a single dc source, two capacitors, and seven switches. Triple output voltage gain, self-balancing capacitors, and lower THD with fewer components are the benefits of this topology. This paper has been organised as follows. In section II, the operation of the reduced switch count seven level inverter topology

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for generating seven voltage levels with matching switching combinations is explained. The switching table, switching logic pattern, and modulation technique used for topology are all discussed in Section III. In Section IV, MATLAB simulation results of proposed circuit at different loading conditions are discussed. The dynamic performance of the topology is investigated by varying different indices like amplitude modulation (m_a), frequency modulation (m_f), and switching frequency (f_s), and a comparison with other topologies in the literature is presented in Section V. Finally, In Section VI paper is concluded.

II.REDUCED SWITCH COUNT SEVEN LEVEL INVERTER TOPOLOGY

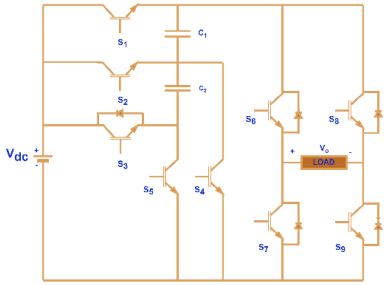


Fig.1 Proposed Seven level inverter topology.

The proposed seven-level inverter topology generates seven levels of output voltage with a voltage gain of three. It consists of a single dc voltage source, two capacitors, and nine switches. Out of nine switches five are with body diode and remaining four are without body diode. In addition, one dc voltage source with magnitude Vdc and two switched capacitors C1 and C2 are connected parallel to the DC source. The capacitors are connected in parallel to the DC source its get charged to a voltage level equal to the dc voltage source Vdc and discharged in series connection with DC source. The seven-level output voltage consists of seven voltage levels which are as follows, zero, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$.

Switches S_6 and S_9 are turned ON to obtain positive voltage whereas S_7, and S_8 are turned ON to get negative voltage. To avoid shoot through faults S_6 S_7 and S_8 S_9 are turned ON in a complementary manner. S_4 S_5 switches are switched ON for the capacitors C_1, C_2 respectively for charging phenomenon by connecting them in parallel with dc voltage source. S_2 S_3 switches are switched ON for the capacitors C_1, C_2 respectively for discharging phenomenon by connecting them in series with dc voltage source.

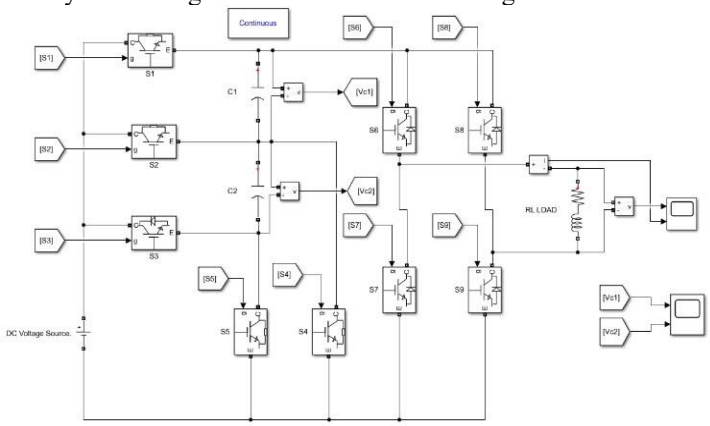


Fig.2 Simulation of Circuit in MATLAB Simulink

Operating Modes of the topology: Each mode of operation is explained with circuit diagram. Red colour path indicated tun ON condition, black colour path indicates turn OFF condition, green colour path indicates charging path. Negative voltage levels are attained with the help of H-Bridge.

1)Positive voltage levels: Switching states and paths for positive voltage levels for proposed topology are discussed and shown in below.

a) For zero voltage level ($V_o = 0$):

Zero voltage level can be attained in two different methods. Either S_6, S_8, or S_7, S_9 must be turned ON. During this period capacitors C_1, C_2 are neither charging nor discharging. They are in floating condition. Zero voltage level operation and its paths are shown in fig.3 and fig.4.

b) For positive V_{dc} level (V_o=+Vdc):

To attain positive V_{dc} voltage level, switches S_1, S_6, S_9 are turned ON, through this path dc voltage source is connected with load. At the same time switch S_4 is turned ON which creates a parallel path for capacitor(C_1) to charge. Positive V_{dc} level operation and its path is shown in fig.5.

c) For positive $2V_{dc}$level (V_o=+$2V_{dc}$):

To get the positive $2V_{dc}$ voltage level, the dc voltage source is connected in series with charged capacitor(C_1) by switching ON switches S_2, S_6, S_9. Here the capacitor(C1) discharges to load. At the same time capacitor(C2) is connected in parallel with dc source by switching ON S_5. Positive $2V_{dc}$ level operation and its path is shown in fig.7.

d) For positive $3V_{dc}$level (V_o=+$3V_{dc}$):

At this voltage level dc source is connected in series with both capacitors C_1, C_2 to the load. This path can be created by switching ON S_3, S_6, S_9. Here both capacitors will discharge simultaneously. Positive $3V_{dc}$ level operation and its path is shown in fig.9.

1)Negative voltage levels: Switching states and paths for positive voltage levels for proposed topology are discussed and shown in below.

a) For negative V_{dc} level (V_o=-Vdc):

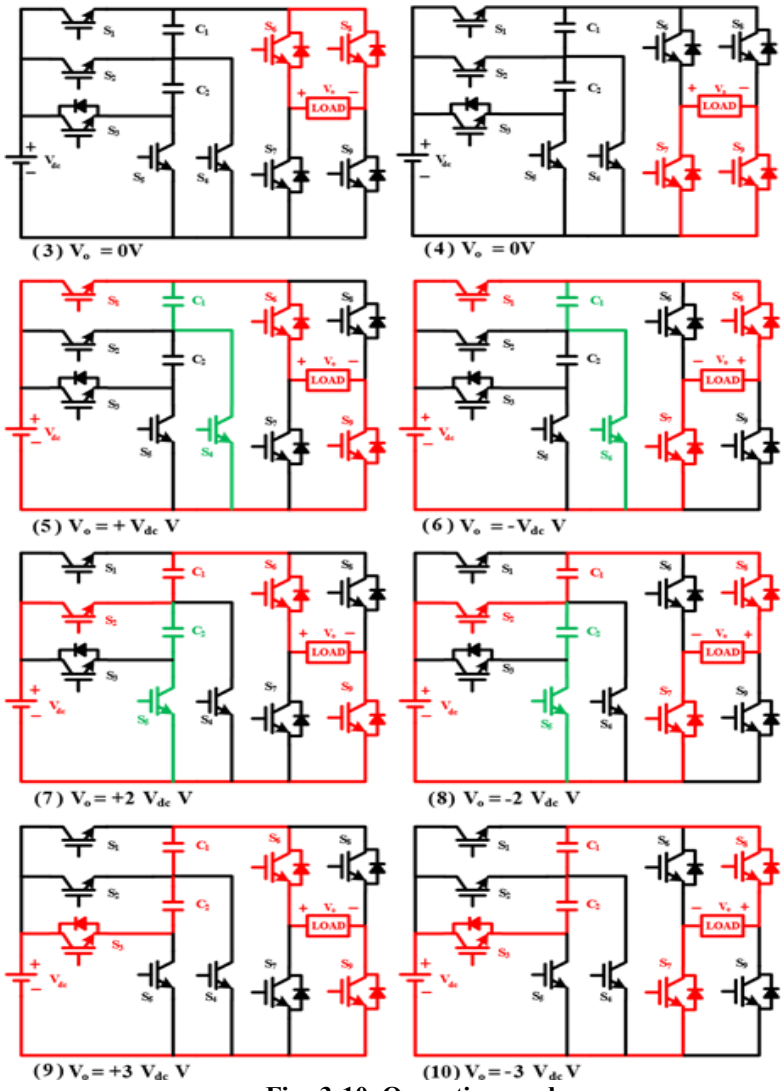
To attain negative V_{dc} voltage level, switches S_1, S_7, S_8 are turned ON, through this path dc voltage source is connected with load. At the same time switch S_4 is turned ON which creates a parallel path for capacitor(C_1) to charge. Negative V_{dc} level operation and its path is shown in fig.6.

b) For negative $2V_{dc}$level (V_o=-$2V_{dc}$):

To get the negative $2V_{dc}$ voltage level, the dc voltage source is connected in series with charged capacitor(C_1) by switching ON switches S_2, S_7, S_8. Here the capacitor(C_1) discharges to load. At the same time capacitor(C2) is connected in parallel with dc source by switching ON S_5. Negative $2V_{dc}$ level operation and its path is shown in fig.8.

c) For negative $3V_{dc}$level (V_o=-$3V_{dc}$):

At this voltage level dc source is connected in series with both capacitors C_1, C_2 to the load. This path can be created by switching ON S_3, S_7, S_8. Here both capacitors will discharge simultaneously. Negative $3V_{dc}$ level operation and its path is shown in fig.10.



Figs.3-10. Operating modes.

III. SWITCHING TABLE AND SWITCHING LOGIC

According to modes of operation, a switching table is formulated. Based on the switching table, switching logic is also written and implemented with the help of the level-shifted PWM technique. Because our inverter has seven levels, we have used six high-frequency carrier waves in a level-shifted manner, which are compared with a low-frequency sine wave. Carrier waves are of unit amplitude, whereas the amplitude of a sine wave is three. According to switching logic, switching pulses are generated and given to the respective switches.

Levels	S1	S2	S3	S4	S5	S6	S7	S8	S9	C1	C2
+3Vdc	0	0	1	0	0	1	0	0	1	**	**
+2Vdc	0	1	0	0	1	1	0	0	1	**	*
+Vdc	1	0	0	1	0	1	0	0	1	*	--
0	0	0	0	0	0	1	0	1	0	--	--
0	0	0	0	0	0	0	1	0	1	--	--
-Vdc	1	0	0	1	0	0	1	1	0	*	--
-2Vdc	0	1	0	0	1	0	1	1	0	**	*
-3Vdc	0	0	1	0	0	0	1	1	0	**	**

Table.1 Switching Table and capacitor states.

(1-Switch ON, 0-Switch OFF, *-Capacitor charging, **Capacitor discharging)

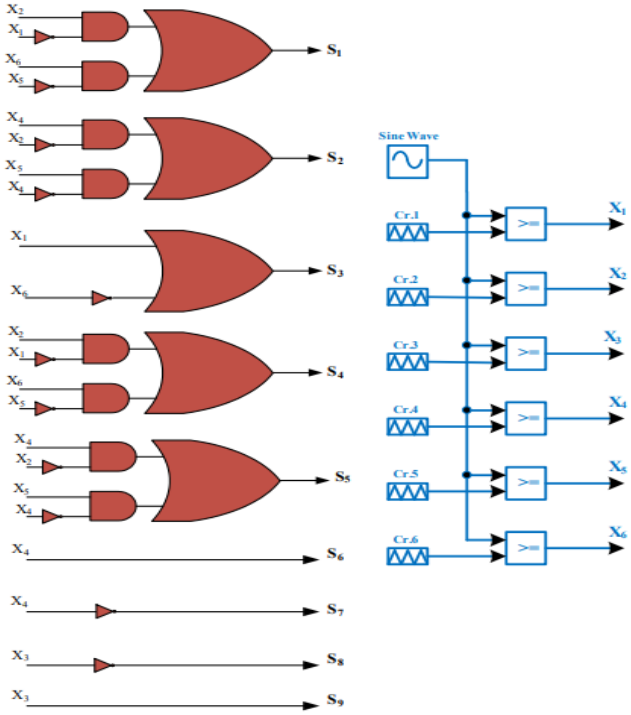


Fig.11.Switching logic pattern modulating and reference waves comparison.

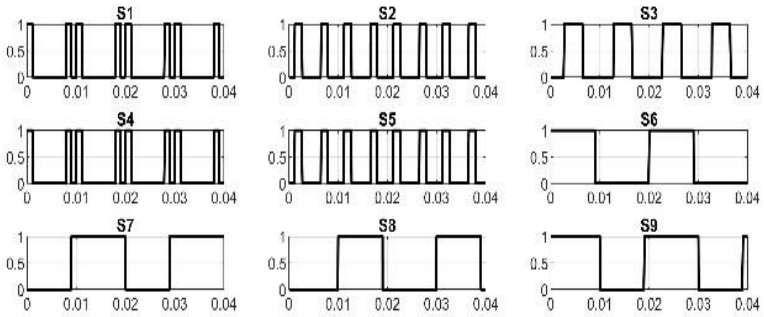


Fig.12.Switching Pulses to switches.

The output voltage waveform, modulating and carrier waves diagram is also shown below.

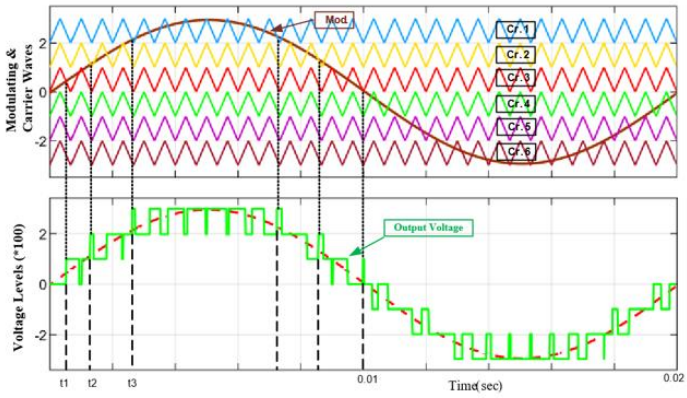


Fig.13.Carrier, modulating waves and output voltage waveforms

IV.LOAD VARIATIONS

To observe the performance of proposed topology, we have varied the loading conditions like R, RL natured. During load variations load current and capacitor voltages are observed. Capacitor voltages are well balanced at below given loading conditions.Fig.14. represents results of output voltage (V_o), output current (I_o), and capacitor voltages (V_{c1}, V_{c2}) at R-Load of 100ohm. Fig.15. represents results of output voltage (V_o), output current (I_o), and capacitor voltages (V_{c1}, V_{c2}) at different loading conditions like no load condition, pure resistive load condition with R-Load of 100ohm, and finally RL load condition with R=100ohm and L=150mH. Fig.16. represents results of output voltage (V_o), output current (I_o), and capacitor voltages (V_{c1}, V_{c2}) at RL-load variations like R=100ohm L is varied and results taken at 20mH, 100mH and 200mH. Fig.17. represents results of output voltage (V_o), output current (I_o), and capacitor voltages (V_{c1}, V_{c2}) for supply voltage variations.

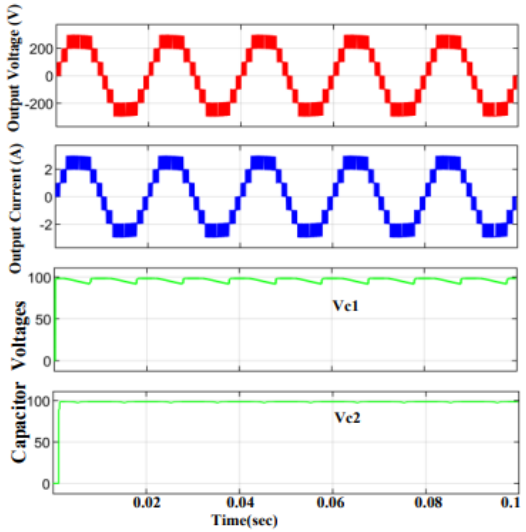


Fig.14.Output voltage, output current and capacitor voltages at R=100ohm.

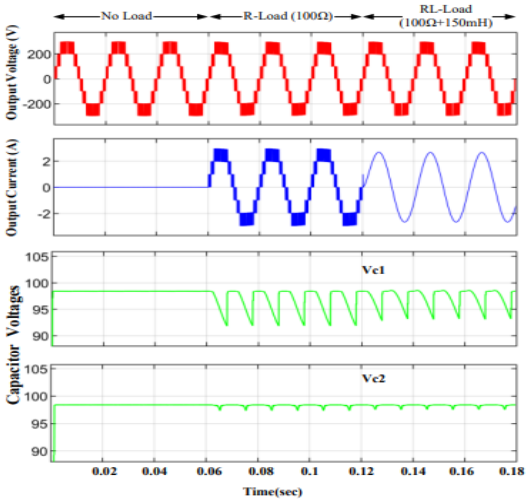


Fig.15.Output voltage, output current and capacitor voltages at no load condition, with R=100ohm, with RL = 100ohm+150mH.

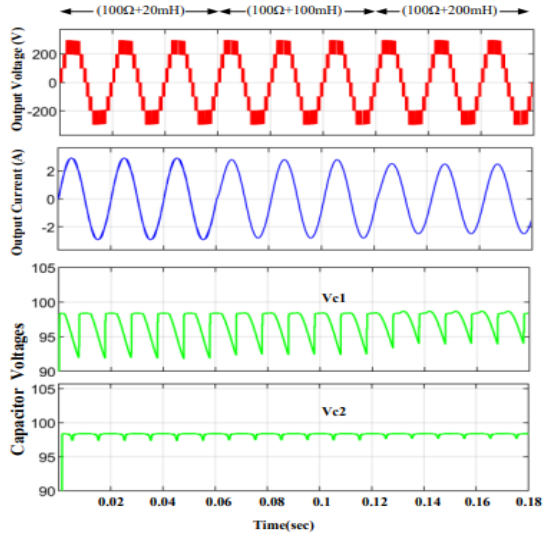


Fig.16.Output voltage, current and capacitor voltages at RL load variations at (100ohm+20mH), (100ohm+100mH) and (100ohm+200mH).

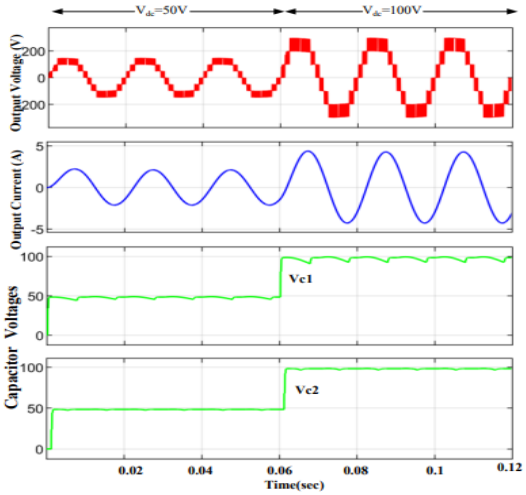


Fig.17.Output voltage, output current and capacitor voltages at input voltage variations from 50V to 100V.

During the input supply variation from 50V to 100V at 50ohm+150mH load, it is clearly observed that output voltage also varied from 150V to 300V, output current varied from 2.1A to 4.3A, capacitor voltages vary from 50V to 100V respectively as shown in fig.17

1. DYNAMIC PERFORMANCE

Dynamic performance of the proposed converter is examined by variations of amplitude modulation, frequency modulation, and switching frequency.

Furthermore, a change of modulation index is also considered for the validation of proposed topology and is illustrated in Fig.18

The modulation index is changed from a value of 0.3 to 0.6 , 0.6 to 0.8 and 0.8 to 1. With a modulation index of 0.3 the number of levels obtained is three and the peak voltage is reduced to 100V. With the modulation index of 0.8 and 1.0, the number of levels is seven. A satisfactory result has been obtained from all these changes in modulation indexes. Both capacitors voltages are maintained at 100V irrespective of change of modulation index.

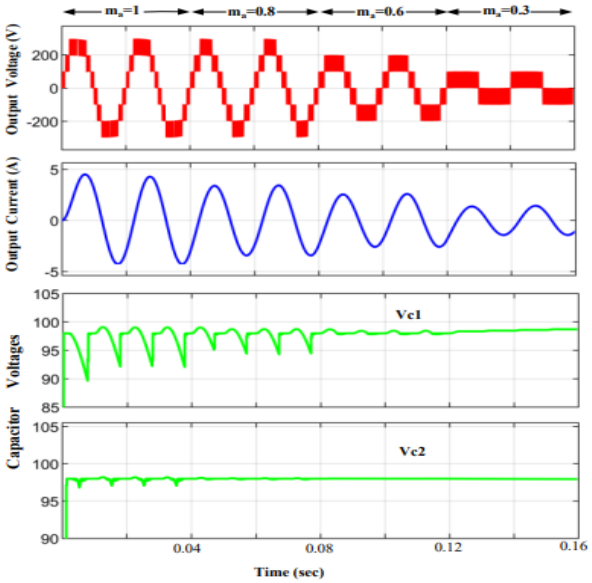


Fig.18. Output voltage, current and capacitor voltages at RL load (100ohm+150mH) with amplitude modulation index(m_a) variation.

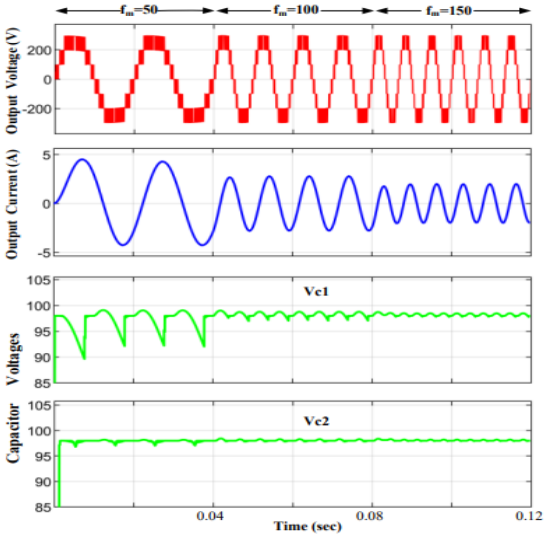


Fig.19. Output voltage, current and capacitor voltages at RL load (100ohm+150mH) with frequency modulation index (f_m) variation.

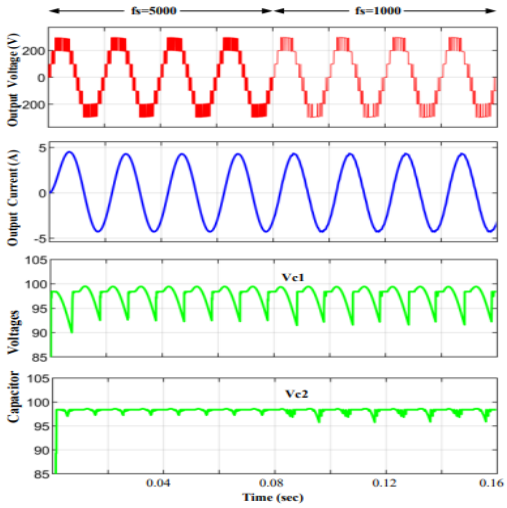


Fig.20. Output voltage, current and capacitor voltages at RL load (100ohm+150mH) with switching fequency (f_s) variation.

COMPARISON TABLE:

In terms of the number of switches used, the number of gate driver circuits needed, the number of diodes (apart from body diodes with switches), the number of capacitors, the output voltage gain of the topology, and the total standing voltage, the proposed seven level topology is compared with conventional topologies and other seven level topologies that are known to exist in the literature. Table 2 makes it evident that any topology needs more components than the one that is suggested. Additionally, there is no need for a power diode in the suggested design.

$$TSV_{pu} = \frac{\Sigma V_{sw\_off}}{V_{o\_max}}$$

Only topologies with a single voltage source can use the formula above. In this case, Vo_max is the maximum output voltage and Vsw_off is the blocking voltage of each switch. The suggested seven-level triple boost multilevel inverter has a TSVp.u of 6.67.

Table.2 Comparison of proposed topology with other topologies.

Topology	X_{sw}	X_{GD}	X_D	X_{CAP}	Gain	TSV (p.u)
CHB	12	12	0	0	3	1.0
FC	12	12	0	7	3	1.0
NPC	12	12	10	6	3	1.0
ANPC	10	10	0	4	3	1.0
[5]	10	9	1	1	3	1.0
[6]	12	12	0	3	3	N.A.
[7]	9	9	2	0	1	N.A.
[8]	10	10	0	4	3	N.A.
[9]	12	12	2	3	3	N.A.
[10]	11	11	1	4	3	N.A.
[11]	12	11	0	2	3	N.A.
Proposed	9	9	0	2	3	6.67

(X_{sw} - number of switches, X_{GD} - number of gate drivers, X_D - number of diodes, X_{CAP} - number of capacitors, TSV- Total standing voltage expressed in per unit (p.u))

FFT ANALYSIS:

FFT analysis of output voltage and output current is done for the proposed topology in MATLAB/Simulink(fig.2) for load R=100ohm

Table.3. FFT analysis of topology for R-Load of 100ohm.

Parameters	Fundamental Component in (Magnitude)	THD in (%)
Output Voltage (V_o)	293.3	18.43
Output Current (I_o)	2.93	18.43

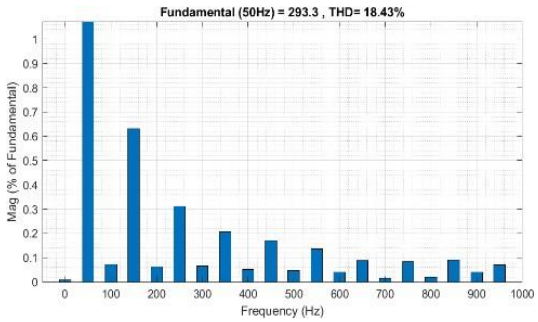


Fig.21.FFT graph for output voltage (V_o).

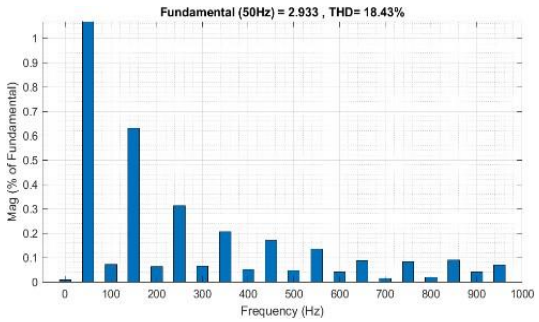


Fig.21.FFT graph for output current (I_o).

FFT analysis of output voltage, output current with R(100ohm) and RL (50ohm+150mH) loads by varying the amplitude modulation index(m_a) is listed below in tables.

Table.4. FFT analysis of topology for R-Load of 100ohm.

m_a	Fundamental Component of voltage in (Magnitude)	THD in (%)
1.0	293.3	18.43
0.9	264.5	22.69
0.8	235.7	24.52
0.7	207.1	25.35

Table.5. FFT analysis of topology for R-Load of 100ohm+150mH.

m_a	Fundamental Component of voltage in (Magnitude)	THD in (%)
1.0	294.4	18.36
0.9	265.3	22.63
0.8	236.2	24.47
0.7	207.2	25.33

RATINGS OF THE COMPONENTS USED IN SIMULATION:

Table.6. Components used in simulation.

Component	Quantity	Ratings/Values
DC Voltage Source	1	50V,100V
Capacitors	2	2200microF
R-Load	1	50,100,150ohm
L-Load	1	20,50,100,150,200mH

2. CONCLUSION

A reduced switch count seven level inverter topology for standalone applications is proposed in this paper. This topology is an alternative solution for reduced switch counts multilevel inverters. This topology is constructed with nine switches, out of these five switches will operate as bi-directional and total nine will operate as unidirectional switches. Using switched-capacitor based technology, the output voltage is boosted up to three times. Proposed topology is validated with different loading conditions. Dynamic performance is verified with variations in amplitude modulations, frequency modulations, and switching frequencies. Output voltage is stable for different loading conditions and capacitor voltages are also balanced properly. Thus, the performance of proposed topology at different loading conditions and its dynamic performance also validated.

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