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Design and Analysis Latch Sense Amplifier Used in SRAM IC by Using Low Power Techniques

Abstract: In today's technologically advanced society, semiconductor chips are integral to most of our gadgets, necessitating small footprints and low power consumption for data storage and memory. SRAM plays a crucial role in meeting these requirements. This study employs Cadence Virtuoso software to design a high-performance sense amplifier circuit tailored for low-power SRAM applications. Various power reduction strategies were explored, leading to the implementation of an optimal solution in a modified SRAM design. The study examines the impact of power consumption and response time of the proposed sense amplifier by adjusting the width-to-length (W/L) ratio of transistors, power supply, and nanoscale technology. Detailed metrics on power usage and transistor count for different approaches are provided to identify the ideal technique. Our proposed low-power sense amplifier design demonstrates promising results, utilizing three variations of VLSI power reduction techniques to enhance efficiency. Low-power SRAMs are poised to advance memory-centric neuromorphic computing applications.

Keywords: SRAM, High Speed, Cross-Coupled Sense Amplifier**, S**ense Amplifier; Low power, Decoder, Power, Delay, DRAM.

I. INTRODUCTION

High-speed memories, such as Static Random Access Memory (SRAM), are essential for handling the vast amounts of data in today's digital systems. In an SRAM, a sense amplifier detects stored data bits (1 or 0) by amplifying differential input signals for accurate interpretation. Since only one row of content is accessible per read cycle, each SRAM column requires only one sense amplifier. Integrating differential logic networks reduces complexity and average delay.

Modeling high-speed sense amplifiers is challenging due to the continuous reduction in memory cell size by one-third and the increase in chip size by 1.5 times with each new generation of complementary metal-oxide semiconductor (CMOS) SRAMs, leading to higher power consumption. Achieving minimal power consumption and robust CMOS analog VLSI circuits is crucial. Scaling down chip area enables the integration of more circuit components on a single chip, thereby reducing parasitic capacitances, power consumption, and production costs while increasing operating speed.

The sense amplifier performs two critical functions: sensing and amplifying data signals. However, the accuracy of sensing data signals decreases with a reduction in supply voltage. Consequently, many memory cells are constantly engaged in loading numerous bitlines, significantly increasing sensing delay. This paper initially analyzes popular and conventional sense amplifier designs and their limitations. It then proposes an improved high-performance sense amplifier design that achieves minimal sensing delay and low power consumption operation.

This is achieved by studying and applying various power reduction techniques to conventional designs iteratively, resulting in the final desired model. In our proposed design, the negative wordline technique was utilized to enhance power efficiency.

The contributions of the proposed work include the following:

1. Development of a high-performance sense amplifier circuit for low-power SRAM ICs.

2. Investigation of the effects of power consumption and response time of the proposed sense amplifier by varying parameters such as the Width to Length (W/L) ratio of the transistor, power supply, and different nanometer technologies.

3. Comparative analysis of the proposed sense amplifier with various existing types, including differential voltage sense amplifiers, cross-coupled sense amplifiers, and latch-type sense amplifiers, based on performance metrics.

The remaining sections of the paper are organized as follows **Section 2** Describes the methodology, design approach, standards used, and constraints of the methodology employed in this work. **Section 3** Discusses the various power reduction techniques used to optimize the existing model, along with simulations and the

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corresponding waveforms generated using Cadence Virtuoso software. **Section 4**: Presents the results obtained from the current work and provides a detailed comparison between all the sense amplifier designs. **Section 5**: Concludes the paper with a discussion of the results and their future implications.

1. Implementation and Design of SRAM cell

2.1 Read and Write Peripherals of Sense Amplifier

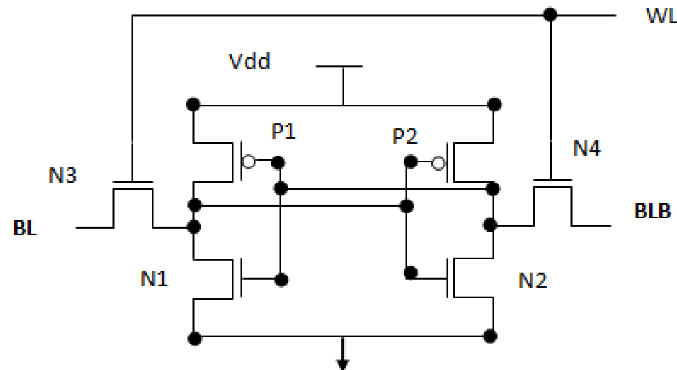

Figure 1. Static Random Access Memory (SRAM) Cell.

Since only one row and one cell per column can be accessed at a time, read and write peripherals are crucial. These peripherals are shared by all SRAM cells in a column, optimizing efficiency.

2.2 Write Circuit

When writing a value into the cell, bitlines are utilized. The cell's value is stored at node Q, while the inverse value is stored at node Q bar. According to the circuit's behavior, logic 1 and logic 0 are not written in their direct forms; instead, only logic 0 is written at node Q or Q bar, depending on the desired value. To write a value into the cell, one bitline should be set to Vdd, while the other bitline should be set to Vss. This operation enables the cell to function as a latch.

2.3 Precharge

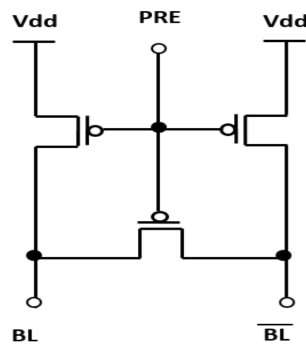

Figure 2. Precharge Circuit for Sense Amplifier.

Before initiating the read cycle, the precharge circuitry equalizes the voltage on both bitlines. This basic precharge circuitry typically consists of three transistors, either NMOS or PMOS. Two of these transistors connect the bitlines to Vdd, while the third transistor connects the bitlines to each other, ensuring a constant voltage across them. Figure 2 illustrates a precharge circuit with three PMOS transistors. In this configuration, the bitlines are precharged by setting the signal PRE to zero, which turns on the PMOS transistors and raises the bitline voltage to Vdd.

2.4 Sense Amplifier with SRAM

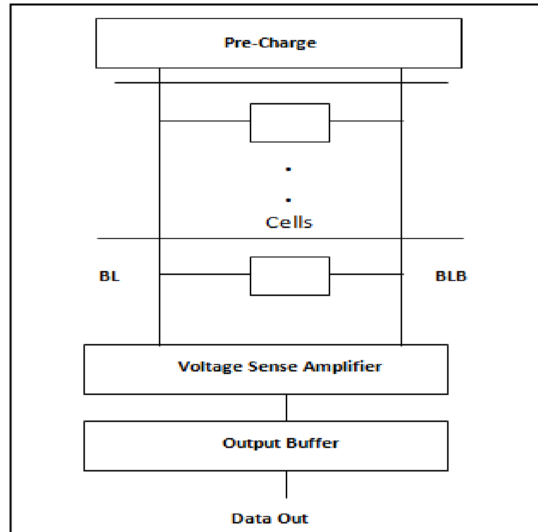

Figure 3. SRAM Model with Sense Amplifier.

Sense amplifiers are fundamental components in modern computers, specifically within IC memory chips. The term originates from magnetic memory technology. A sense amplifier reads information from memory by detecting the low-power signals produced by the bitlines, which indicate data bits (1 or 0) stored in the memory section. It then amplifies these tiny voltage swings to identifiable logic levels so the data can be captured and used.

Modern sense amplifier designs typically use 4-6 transistors, a significant reduction from the 10-14 transistors used in earlier designs. Hundreds or thousands of nearly identical sense amplifiers are commonly deployed in a single application. Memory cells store information on the chip, generally within volatile memory cell sections. Figure 3 illustrates the rows and columns of SRAM memory cells.

2.5 Wordlines and Sense Amplifier Operation

Each memory cell is connected to a line called a wordline, which is activated by applying a specific voltage. The voltage level for each wordline is determined by the technology node used in the transistor design. This article focuses on the sense amplifier implementation at the 180 nm technology node, where the voltage level is set at 1.8 V. Each sense amplifier is connected to two complementary lines, interacting with both the wordline and the bitline. The same bitlines are used for both reading and writing data.

2.6 SRAM Operation: In read mode, the wordline is set to high, activating the cell in that row. The stored values, 0 and 1, create a differential signal that the sense amplifier, located at the end of the lines, amplifies to a normal logic level. The bit from the requested cell is then latched into a buffer and sent to the output bus.

2.7 Sense Amplifier Goals and Types

The primary goals of a sense amplifier are to reduce sensing delay, increase amplification, minimize power consumption, fit within the allotted space, and ensure high reliability.

2.8 Types of Sense Amplifiers

This includes all designs such as:

a. Differential voltage sense amplifier

b. Basic latch sense amplifier

c. Basic latch sense amplifier with sleep transistors

a. Differential Sense Amplifier

The differential amplifier circuit shown in Figure 4 is a widely used standard design. This dynamic voltage mode amplifier consists of a differential pair with an active current mirror load (M3, M4 - PMOS transistors) connected to the end of the biasing current source or ammeter. The gates of the differential pair transistors (M1, M2 - NMOS transistors) are connected to the bitlines, and the output is obtained from the side of V2. V1 and V2 are the supply voltages for the NMOS transistors.

As the current source is connected at the end, the sum of the currents flowing through both transistors remains constant at all times. The transient response of the differential amplifier is plotted in Figure 5. Since the gate-to-

source voltage of both PMOS transistors is identical, the input current equals the output current, which remains static, enhancing the sensing speed. However, this comes with the drawback of a power consumption of 179 µW.

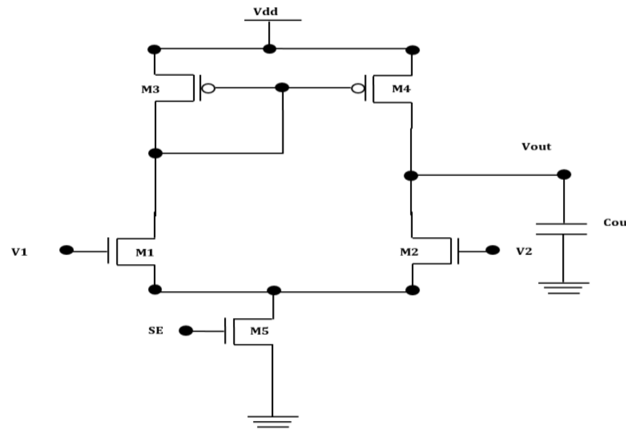

Figure 4. Differential Sense Amplifier Schematics.

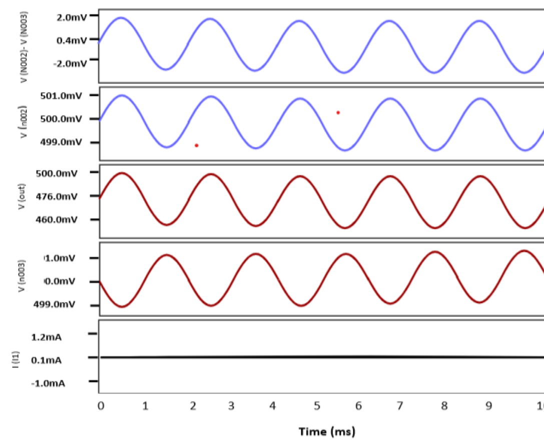

Figure 5. Output waveform of Differential Voltage Sense Amplifier.

b. Basic Latched Sense Amplifier

While the differential amplifier is a dynamic type, the basic latch sense amplifier is a static voltage mode sense amplifier. It employs two cross-coupled inverters to create positive feedback, enabling its latching behavior, as shown in Figure 6. During the read cycle, the bitlines are precharged to a certain voltage level to establish a common starting point, ensuring the voltage difference can be clearly sensed later.

These precharged bitlines are connected to the inputs of the sense amplifier. This connection allows a small voltage bias to develop at the gates of the MOSFETs before the inverters are activated and the sense amplifier is enabled. The response of the basic latch sense amplifier is depicted in Figure 7.

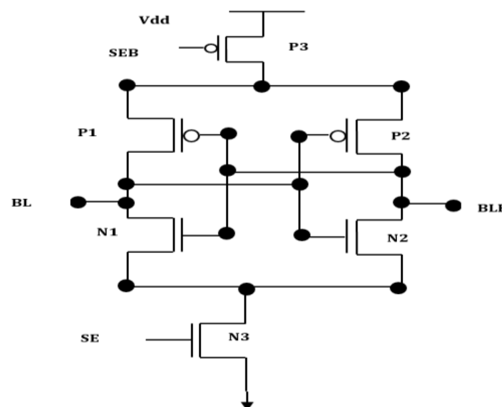

Figure 6. Basic Latched Sense Amplifier Schematic.

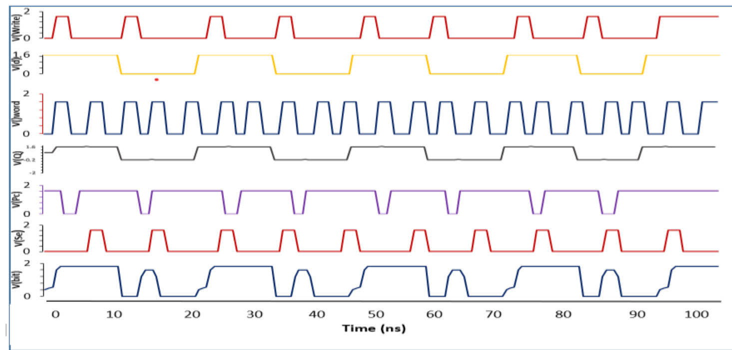

Figure 7. Output waveform of Basic Latch Sense Amplifier.

c. Basic Latched Sense Amplifier (Modified)

The amplifier shown in Figure 8 operates similarly to the basic latch sense amplifier but includes a sleep transistor that separates the inputs and outputs of the amplifier from the bitlines. This design ensures that the sense amplifier drains the bitlines before storing the input data in the SRAM.

The sleep transistor remains active even when the sense amplifier is disabled, allowing the voltage on the gate to continue developing while the bitlines discharge. Once the sense amplifier is powered on, the pass transistor deactivates, decoupling the bitlines from the amplifier. After the sense amplifier is enabled, the bitlines can no longer discharge. The transient response of this design is shown in Figure 9. The drawback of this configuration is that the pass transistors are isolated from the other transistors.

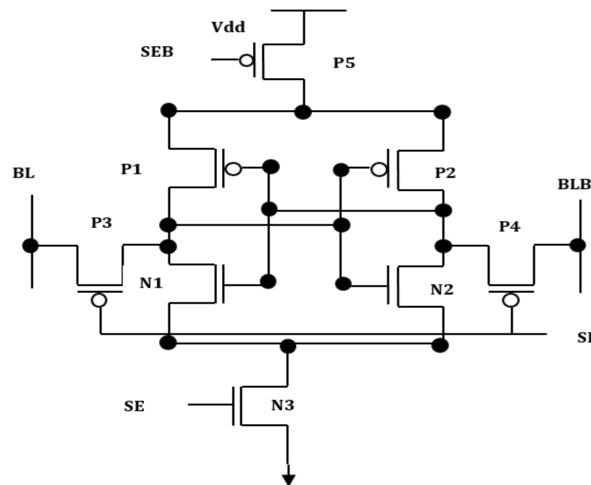

Figure 8. Basic Latched Sense Amplifier (Modified).

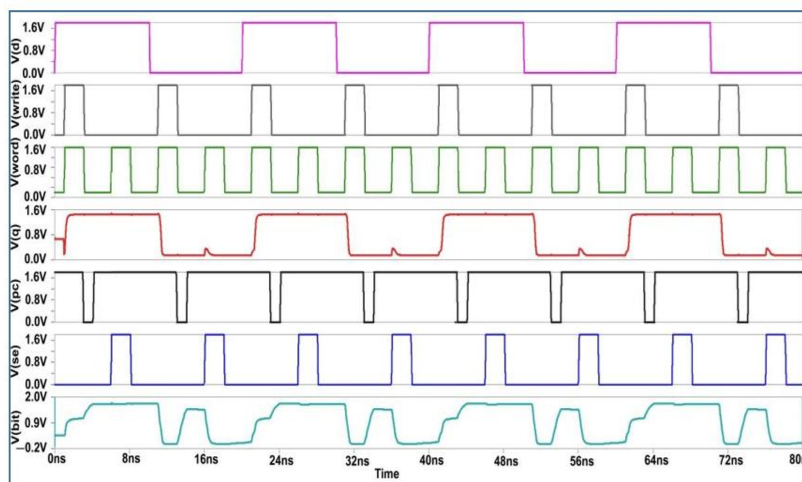

Figure 9. Output waveform of Basic Latch Sense Amplifier with sleep transistors.

d. Cross-Coupled Sense Amplifier

The cross-coupled sense amplifier, shown in Figure 10, includes transistors P1, P2, N2, and N3, which form a current conveyor as a column selector. When the Bit signal is low and the cell is accessed, transistors M2 and N3 turn on, allowing the differential signal to flow from the bitlines to the data lines.

In this voltage mode operation circuit, P1, P2, N2, and N3 create two MOS amplifiers. The output of these amplifiers is proportional to the equivalent resistance of N2 and N3. These two amplifiers are interconnected with positive feedback within the current conveyor circuit.

At the end of the reading operation, the column select signal (CS) transitions from low to high. This increases the equivalent resistance of N4 and N3, as well as the gains of the MOS amplifiers. After the reading procedure, these high-efficiency amplifiers will amplify the voltage difference between nodes instead of automatically eliminating it.

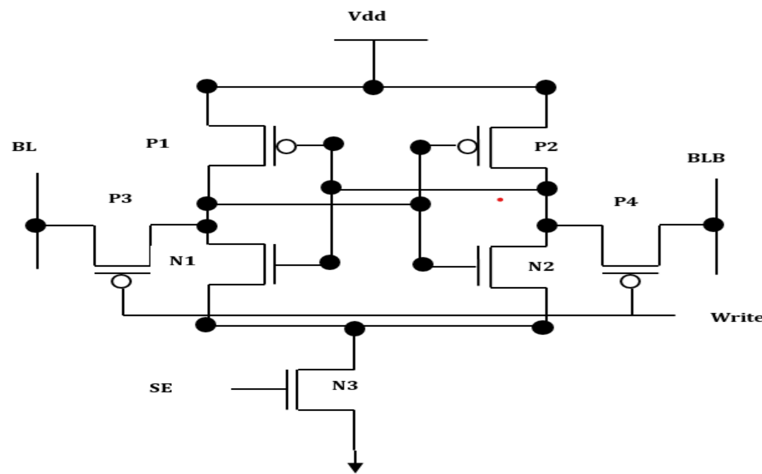

Figure 10. Schematic of the cross-coupled sense amplifier.

Simulations with varying transistor sizes show that the cross-coupled transistors P1 and P2 maintain the unbalanced configuration even when the column select signal (CS) drops again. Previous studies assumed that the nodes had equivalent voltages.

This 6T-SRAM circuit is designed using CMOS inverters, which minimizes power dissipation. At the micro-scale, the primary challenge is leakage current. In this design, the output terminals serve as internal lines or bitlines to store data bits, and they complement each other, as depicted in Figure 10. The power consumption spectrum of the cross-coupled sense amplifier is illustrated in Figure 11.

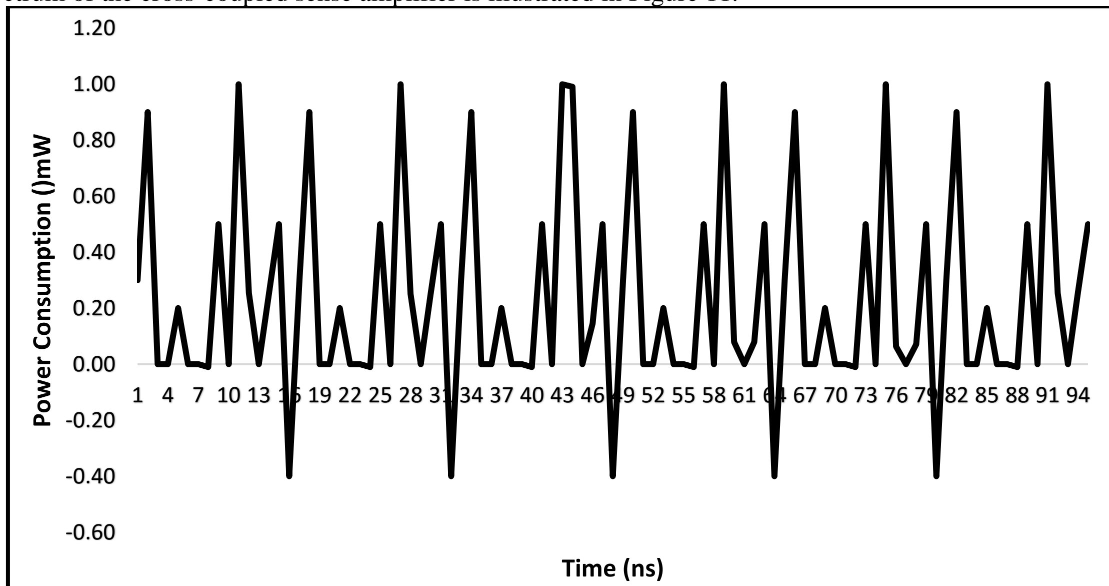

Figure 11. Power Consumption Waveform of Cross Coupled Sense Amplifier.

Write and Read Operations in Cross-Coupled Sense Amplifier

During the write operation, data is supplied at the bitline connections: the data bit is written using the bitline, and its inverted logic value is provided on bit_bar. The wordline is activated, allowing the bitlines to overwrite the cell with new values. For example, if out = 0, out_bar = 1, and bit = 1, bit bar = 0, this forces out to high and out_bar to low.

During the read operation, logic values are addressed to bit and bit_bar. The wordline is kept high to enable charge sharing between lines. If out = 0 and out_bar = 1, the bitline discharges through the two adjacent NMOS transistors to ground, while the bit_bar line remains high.

However, the cross-coupled regeneration response and the presence of other devices in the circuit pose challenges. For example, the presence of an equilibrium device between two differential nodes and a tail current source can significantly reduce the circuit's performance.

2. Exploring the Impact of Power Reduction Strategies on Traditional Sense Amplifier Design

3.1 Power-saving Methods

The following sections delve into circuit-level strategies aimed at reducing leakage power in a 6T-SRAM cell. These methods involve manipulating the terminal voltages of the SRAM cell during standby mode [11−16].

Sleep Transistor Technique

In this technique, a PMOS transistor is connected between VDD and the SRAM cell, while an NMOS transistor is connected between the SRAM cell and GND. Both transistors are activated in the active mode, establishing a pathway between VDD and GND. However, in sleep mode, both transistors are deactivated, effectively cutting off the power supply to the SRAM cell and creating a virtual VDD-GND pathway.

Source Biasing Technique

In this approach, a pull-down NMOS transistor is used, with its gate terminal connected to the wordline, creating a connection between GND and the SRAM cell. When the wordline goes high in active mode, the NMOS transistor turns on. Due to its low resistance, the virtual ground voltage VSL behaves similarly to a physical ground line, allowing the SRAM cell to function as usual. In standby mode, when the wordline is set low, the NMOS transistor is turned off, resulting in an increase in the source voltage and a reduction in subthreshold and gate leakage currents.

The Negative Wordline Scheme

The Negative Wordline Scheme involves applying a negative voltage to the wordline during idle periods, maintaining device performance. This approach raises the threshold voltage and reduces leakage current when a majority of NMOS are negatively biased or a majority of PMOS are positively biased. Studies suggest that maintaining the bias below -0.4 V effectively minimizes leakage current [11].

The Dual Sleep Technique

The Dual Sleep Technique involves connecting two pairs of transistors (PMOS and NMOS) in parallel. The first pair is positioned between VDD and the SRAM cell, while the second pair is between the SRAM cell and GND. During active mode, the sleep transistors (NMOS and PMOS) are activated, establishing a pathway between VDD and GND similar to the sleep transistor approach. In "sleep mode," these transistors are turned off, effectively cutting off power to the SRAM cell and creating a virtual VDD and GND path [2].

Table1. Comparison of average power consumption with varying supply voltage for various sense amplifiers P (μW) for180nm

S.N.	VDD(V)	Differential Voltage Sense Amplifier[8]	Basic Latch Sense Amplifier[7]	Basic Latch Sense Amplifier with Pass Transistor [5]	Commonly Cross Coupled Sense Amplifier[1]
1	1.2	119.92	36.425	36.627	36.481
2	1.5	149.93	55.412	55.656	52.983
3	1.8	179.94	80.713	81.061	77.097
4	2.1	209.95	95.995	92.227	101.18
5	2.4	239.96	107.770	112.40	135.63

3.2 Modified Standard Sense Amplifier

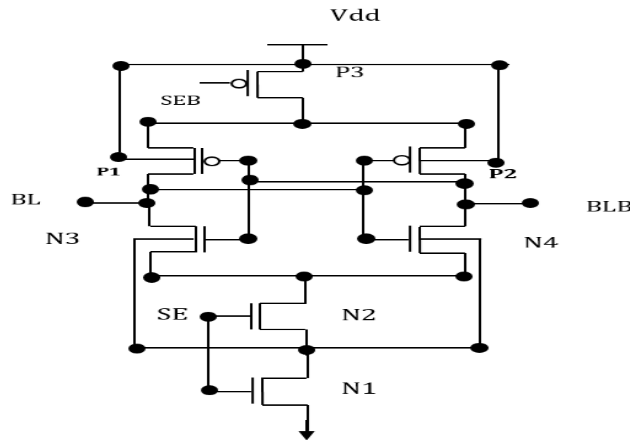

Figure 12. Schematic of Modified Latch Sense Amplifier.

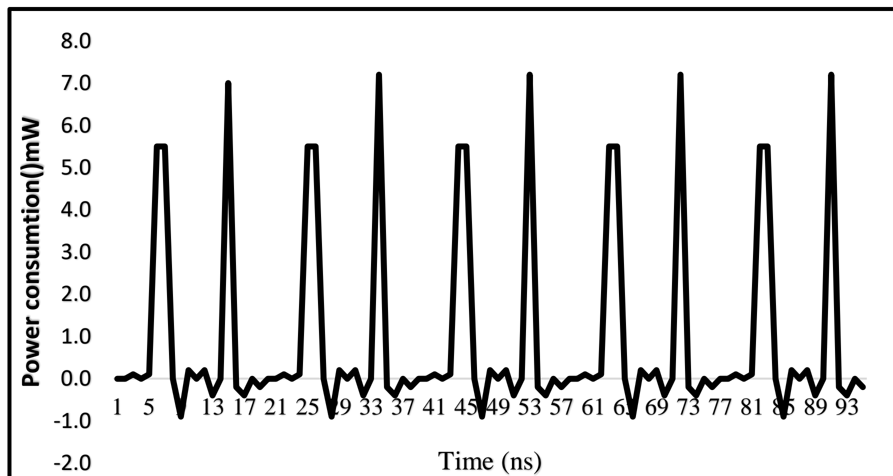

Figure13. Power Consumption Spectrum of Modified Basic Latch Sense Amplifier.

The Average Power Consumption of Modified Standard Sense Amplifier Implementations was evaluated using 180 nm MOS technology. Table 1 presents the average power consumption across different supply voltages. It's evident that increasing VDD leads to higher power consumption across all sense amplifier designs. Figure 12 illustrates the schematic of the basic latch sense amplifier design, while Figure 13 depicts its power consumption spectrum. This sense amplifier prioritizes fast differential signal reading on the bitlines to enhance throughput and minimize power usage, maintaining a power consumption level around 7.2 mW.

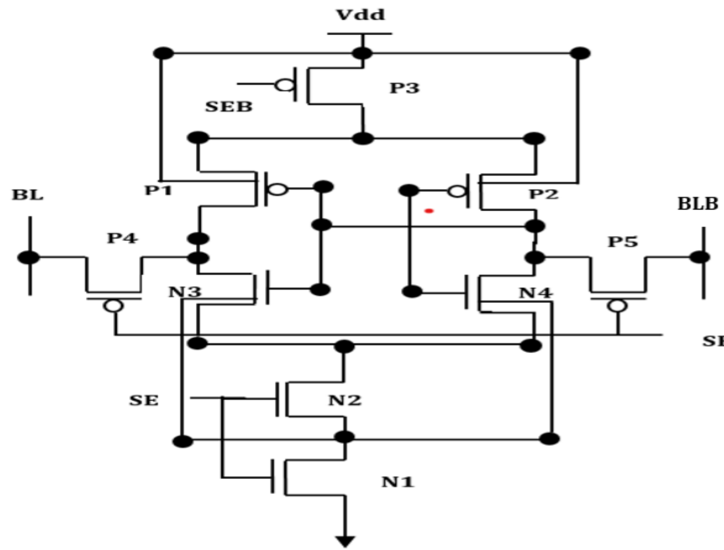

Figure14. Modified Basic Latch Sense Amplifier.

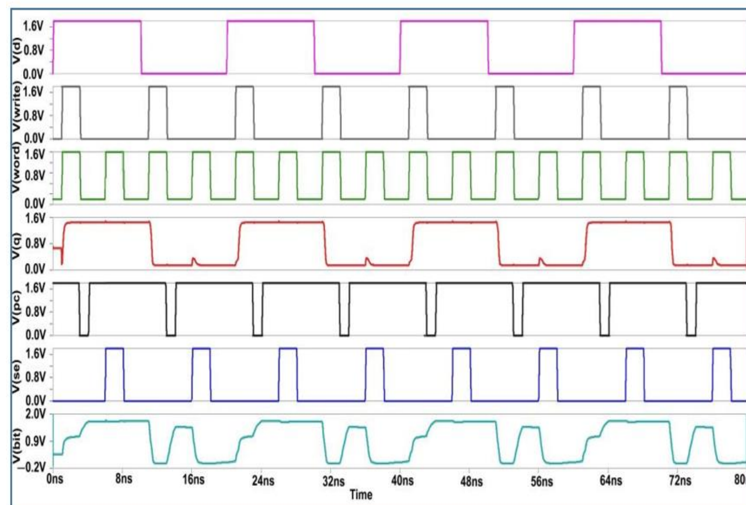

Figure15. Output Waveform of Modified Basic Latch Sense Amplifier.

However, the introduction of pass transistors in the basic latch sense amplifier design, as depicted in Figure 14, separates the amplifier inputs and outputs from the bitlines. This eliminates the possibility of the sense amplifier mistakenly reading the SRAM value retained in the cell after the bitlines are fully discharged, which was a concern in the previous design due to shared physical nodes. While this modified design with pass transistors benefits from having distinct physical nodes, the inclusion of two NMOS transistors on each side introduces a voltage drop across them, as shown in Figure 15. This could potentially lead to biased logic values due to variations in transistor size during fabrication.

In Figure 16, the cross-coupled sense amplifier design is illustrated, emphasizing the shared connection of the "Sensing Enable (SE)" signal. This schematic decreases the number of transistors needed for separate write and sensing enable signals, as demonstrated in Figure 10. Figure 17 shows the resultant decrease in power consumption to 0.8 mW at 180 nm.

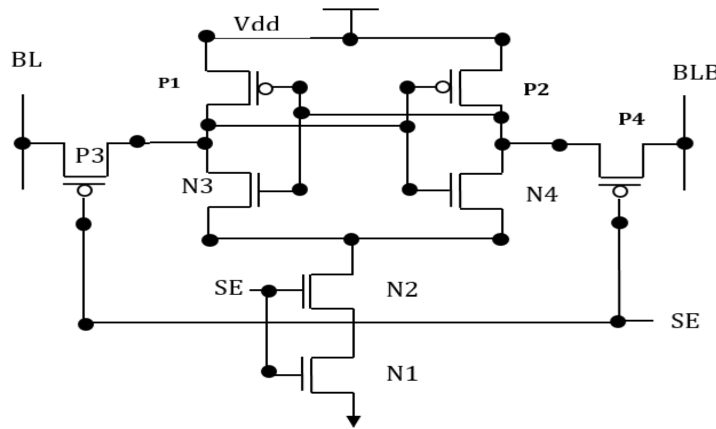

Figure16. Cross Coupled Sense Amplifier.

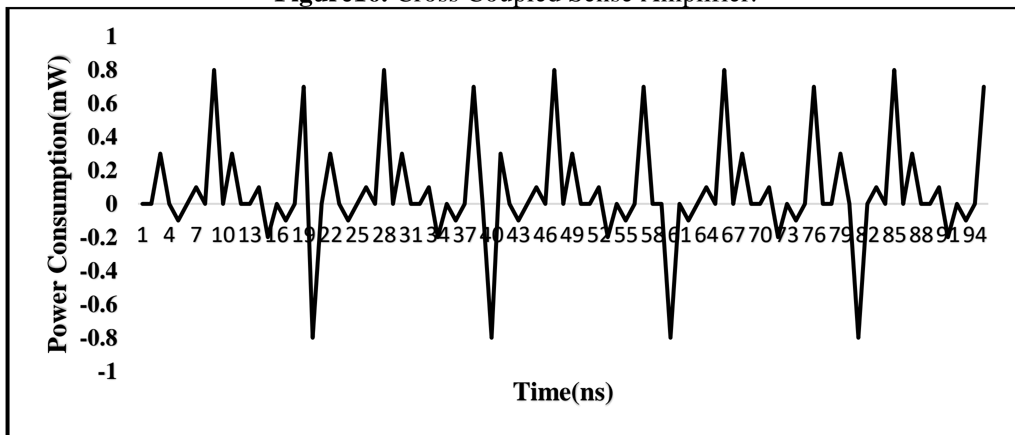

Figure17. Power Consumption Spectrum of Commonly Cross Coupled Sense Amplifier.

Table 1 presents a comparison of average power consumption alongside the corresponding transistor sizes for all three conventional designs. Additionally, the power reduction techniques employed in our proposed design, namely source biasing and negative wordline, were applied to the conventional designs as well. The resulting power readings and their associated transistor sizes were recorded and organized in Table 2.

Table2. Comparison of average power consumption with supply voltage and their transistor sizing for all three conventional designs.

S.N.	Design Name	Supply Voltage	N0. of Transistor used	Average power consumption
1	**Differential sense amplifier [8]**	**1.8**	**4**	**179.94**
2	**Basic Latched Sense Amplifier[7]**	**1.8**	**6**	**80.713**
3	**Latch sense Amplifier with pass transistor[5]**	**1.8**	**8**	**80.713**

II. PROPOSED SENSE AMPLIFIER IMPLEMENTATION: RESULTS AND DISCUSSION

We can confidently affirm that the primary role of sense amplifiers is to amplify the minute voltage difference between bitlines into a logically high value, as elaborated in the comprehensive overview of sense amplifiers. The bitlines carry a significant capacitive load, leading to RC delays. Recent advancements in SRAM designs [17–26] showcase innovative device architectures such as 6T SRAM with FinFETs, and Junction less TFETs, claiming lower power consumption. In line with this, our proposed sense amplifier design integrates power reduction techniques with pass transistor and optimizing energy efficiency.

Additionally, as mentioned in prior designs, sense amplifiers incorporate a differential logic circuit to elevate the sophistication of logic circuits and reduce the delay experienced by the differential circuit [13]. A key challenge arises during the design of large-scale SRAMs in CMOS technology, as these large SRAMs entail numerous bitlines, leading to considerable delays [11].

Another challenge arises when designs operate at voltages lower than the supply voltage, which hampers the primary goal of fast sensing [4]. The cross-coupled sense amplifier is among the most commonly used designs, featuring a complementary structure consisting of two pull-up and two pull-down transistors. The speed and

loading attributes of this design hinge on discharging conductivity and cross-coupled capacitance values. Notably, conductivity is inversely related to capacity, yielding higher conductivity for lower capacity. In the proposed design, the two cross-coupled inverters are replaced by two transistors, as illustrated in Figure 18. When the wordline is activated, transistors N4 and N5 turn on, allowing the bitline voltage to flow to the output terminals. To further minimize power consumption, a technique known as source biasing is employed to reduce leakage current. Source biasing involves adding an NMOS transistor at the circuit's end, operated by the sense enable signal, creating a virtual ground when activated. This technique serves as a power-saving and leakage current reduction method, where a pull-down NMOS transistor is introduced between the ground and source lines of the SRAM cell, with its gate terminal connected to the wordline [4]. The transistor activates when the wordline goes high in active mode. Due to its low resistance, the virtual ground voltage (VSL) effectively functions as a true ground line, enabling normal SRAM cell operation. In standby mode, when the WL is set low and N4 is turned off, the source voltage increases, reducing subthreshold and gate leakage currents.

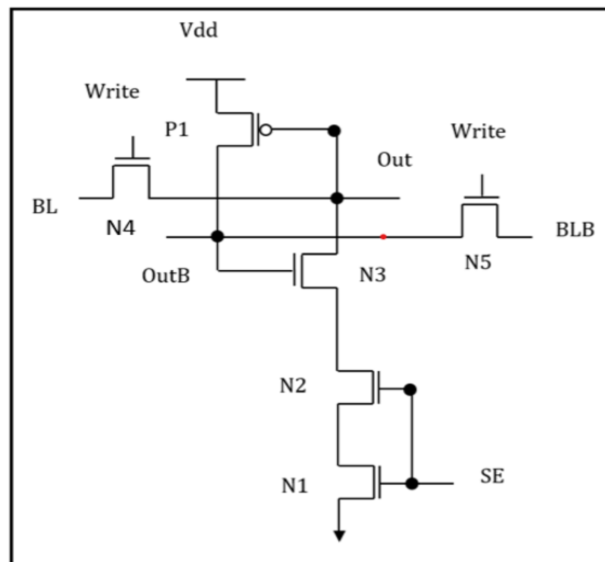

Figure18. Schematic of Proposed design (Modified Cross-Coupled SRAM).

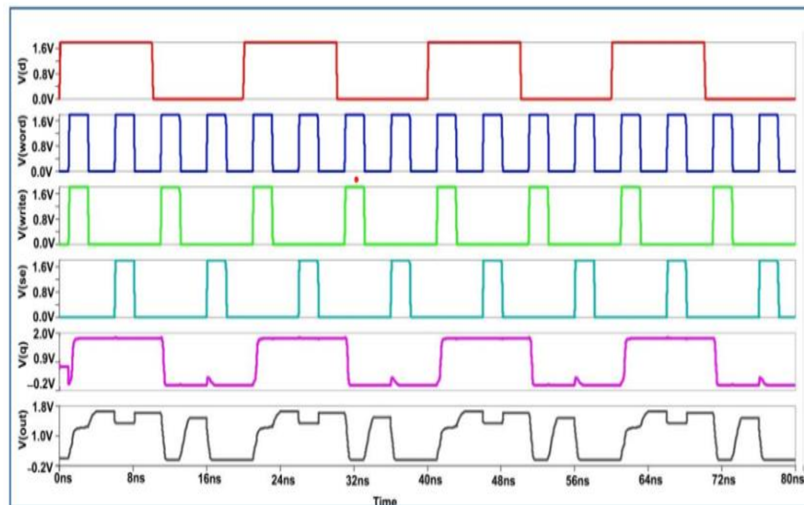

Figure19. Output Waveform of Proposed Sense Amplifier.

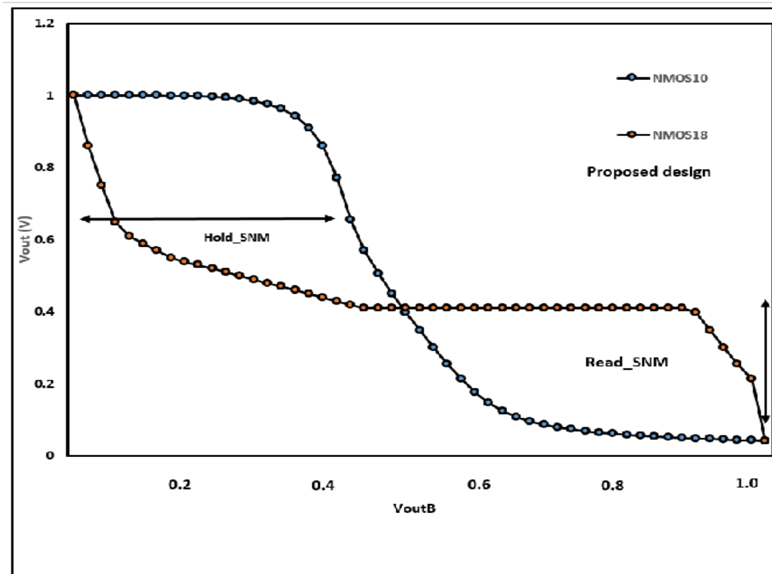

Figure20. Hold and Read (SNM) Static Noise Margin of Proposed Sense Amplifier.

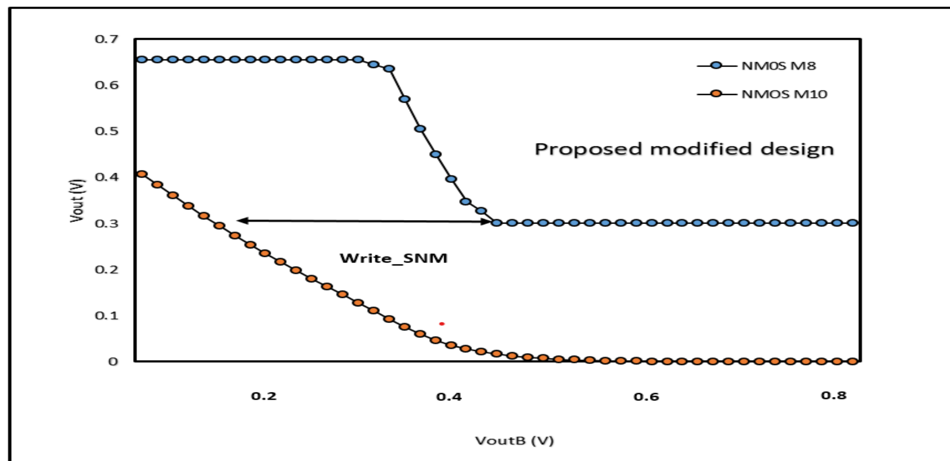

Figure21. Write (SNM) Static Noise Margin of Proposed Sense Amplifier.

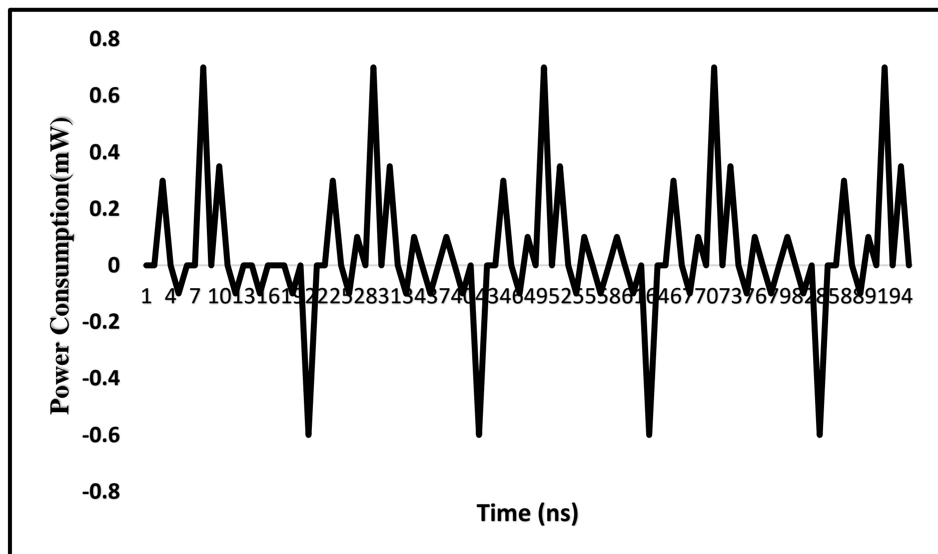

Figure22. Power Consumption wave of Proposed Sense Amplifier.

We observe that strategies aimed at reducing power consumption also lead to lower access times for large memories. By combining the cross-coupled FET configuration with negative wordline and source biasing techniques, the bitlines in the proposed design experience reduced capacitance effects, resulting in decreased RC delay. This is evident in the "Modified Cross-coupled design" depicted in Figure 19. Returning to our proposed design, during READ mode, we integrated the negative bitline technique, serving the same purpose as source biasing by supplying a negative voltage to the wordline during idle periods without impacting device performance or Soft Error Rate (SER) [4]. This action significantly reduces sub-threshold leakage current as the access transistors are turned off. However, one drawback of this technique is the potential increase in gate leakage current of the access transistor due to widened gate-source and gate-drain voltage differences. Essentially, this technology stabilizes the write signal value within a narrow range. Consequently, by incorporating these two designs into the modified setup, power consumption is notably diminished.

Figures 20 and 21 depict the Static Noise Margin (SNM) measurements for the hold, read, and write operations of the proposed sense amplifier configuration in static RAM. These results affirm that the recommended device exhibits robust noise resilience, crucial for ensuring accurate SNM window frames during read and write operations. A higher noise margin is indicative of superior signal quality. In comparison to the circuit's propagation delay time, a pulse width lasting a few microseconds is unusually long for high-speed ICs. Therefore, the reasonable noise margin achieved in the proposed design leads to reduced delay, making the Modified Cross-Coupled sense amplifier more suitable for implementing high-speed SRAM circuits. Additionally, the average power consumption spectra for both waveforms are displayed in Figure 22.

During the write cycle, when both the word and write signals are set to HIGH input (logic 1) simultaneously, data is transferred from data D to Q. In the read cycle, we begin by precharging the circuit and enabling the SE (sensing enable). When writing a logic 1 to the left side of the SRAM cell, the bitline doesn't reach full charge to VDD (1.8 V) due to the NMOS transistor not transmitting a perfect or strong 1. This results in two voltage drops at the Q output due to the threshold voltage of the transistors, while the bitline on the opposite side is fully charged to 0. This difference is enough to toggle the cell to the desired state. The PC (precharge) signal is set to logic 0, allowing the PMOS transistor to transmit a full or strong 1, leading to full charging of the bitlines to VDD. For the read operation, both the wordline and SE signal must be set to HIGH logic simultaneously to copy the data from the Q output to the bit output [9].

S.N.	**Design Name**	**Area (Transistors)**	**Power Consumed (µW)**	**Area (Transistors)**	**Power Consumed (µW)**
1	**Basic Latch Sense Amplifier [7]**	**6**	80.713	**7**	**39.504**
2	**Basic Latched Sense Amplifier with Pass Transistor[5]**	**8**	81.061	**9**	**9.46**
3	**Cross Couple sense Amplifier [1]**	**7**	77.097	**8**	**7.5912**
4	**Proposed Design**	**5**	80.64	**6**	**7.0015**

Table3. Comparison of average power consumption for all the designs with their modified versions.

Table 3 presents the power reduction techniques applied in the conventional designs, as shown in the "modified" column.

The addition of the source-biased transistor results in reduced power consumption across all cases. The modified cross-coupled sense amplifier exhibits an average power consumption of 7.5912 µW, which is close to our proposed design's power of 7.0015 µW. However, the transistor sizing area is smaller in our proposed design, making it the optimal choice for a high-performance and low-power sense amplifier ideal for high-speed SRAM applications.

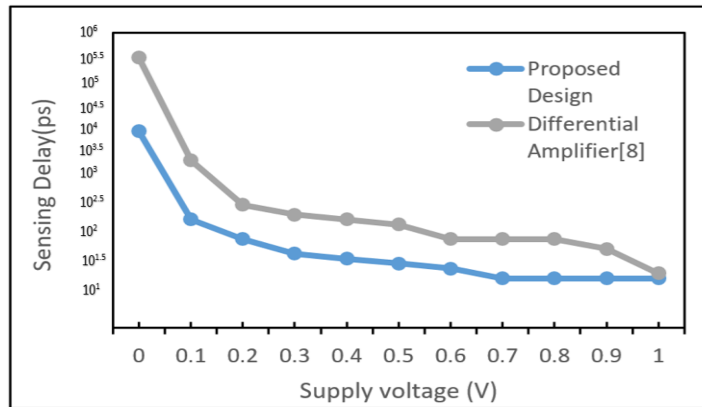

Figure 23. Sensing Delay of Proposed Sense Amplifier.

The performance of the sense amplifier relies heavily on the overall sensing delay, as depicted in Figure 23. Through the implementation of negative bitline and source biasing techniques, the proposed Modified Cross-Coupled SRAM design showcases a reduced sensing delay when compared to the differential sense amplifier [8]. At an initial supply voltage of 0.1 V, the proposed design exhibits a substantial (nearly 99%) decrease in sensing delay, credited to the minimized capacitance effect on the bitlines, resulting in a significant reduction in latency. This reduction in capacitance effect is achieved by applying a negative voltage to the wordlines, maintaining noise margin, power, and delay integrity. As the supply voltage varies from 0.1V to 1.0V, the sensing delay decreases from 5.5 ns to 55 ps.

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