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Regular paper

Converter Configurations for Battery Management and Power Control in Standalone Solar PV fed Cascaded Multilevel Inverter

Bulk power supply using solar PV (SPV) system is a demanding option. Standalone solar PV system along with battery support isnow apopular option for large and continuous power transfer. In this manuscript, a single-phase cascaded H-Bridge multilevel Inverter (CHBMLI) has been used to address the concern of large power controlalong withbattery management. In this paper, two configurations of solar PV system with CHBMLI have been proposed, one with multiple battery banks sitting on DC side along withbidirectional DC to DC converter and the other one with battery banks employed on AC side with controlled AC/DC converter designed for the same power management. The DC side battery system can be used with multiple units of standard battery charge controllers, whereas in the AC side battery system a common battery bank can be used with controlled AC/DC converter. The sliding mode control has been used for the inverter output AC voltage control. The result of power management using seven-level CHBMLI with two configurations has been shown through the simulation studies carried out in PSCAD 4.2.1 platform. Dynamic operation with transformation in SPV power conditioning at various load condition, along with power control by battery discharging/charging has been shown through the simulation results.

Keywords:SPV system, CHBMLI, AC/DC converter, power control, battery banks.

1. Introduction

The dependency on renewable sources has increased in past few years due to depleting limited conventional energy sources. The energy demand is growing exponentially, and it has forced us to use a renewable source. The renewable energy, especially the SPV based resource is a better option in the places where solar energy is uniform across the year[1].

Various maximum power point tracking (MPPT) algorithms had been discussed for SPV array in [2]-[6]. The Perturb and Observe (P&O) techniqueis the most popular method for the maximum power extraction. The sliding mode control (SMC) is an important technique to track the desired voltage at the output of the voltage source inverter (VSI). Different types of SMC methods have been discussed in [7]-[9]. The SMC for voltage control offers several advantages which include good robustness under external parameter variation, parameter insensitivity, and good dynamic response. However, the SMC operates at infinite switching frequency under its ideal implementation. The use of hysteresis band can limit the switching frequency with the compromise on ripples in the output [10]. The method to obtain fixed switching frequency from the variable frequency in SMC has been discussed in [11]. The H-bridge inverter has simplicity in control and full utilization of input DC to obtain output voltage and power levels compared to other types of single-phase inverters [12]. Also, the H-bridge inverter has better reliability because of its modular topology. Pulse width modulation is the mostly used method for controlling the output voltage of the VSI [13]. Power quality assessment of a SPV suppliedfrom seven-level CHBMLI has been

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carried out with different magnitude of voltage sources applied to the VSI in [14]-[15]. The output voltage quality is better when equal dc voltages are applied to each H-bridges compared to when unequal dc voltages are applied to the VSI. To reduce switches, count in SPV fed cascaded multilevel inverter a digital logic function has been used in [16].

For charging as well as discharging of the batteries through converters, current control methods can be implemented. Various linear and nonlinear current control methods have been proposed which have their own advantages and disadvantages. Linear current control methods which are characterized by fixed switching frequency include pulse width modulation, PI controllers etc. However, they have performance limitations. Nonlinear current control methods like hysteresis current control method (HCC) are characterized by varying switching frequency but offer a quick response to transients [17], [18]. Double hysteresis band has also been proposed which offers several advantages like reduced harmonic distortions, easy implementation, and control etc [19]-[20].

In this manuscript, a seven-level CHBMLI has beenemployedto condition the DC power obtained from the solar PV towards the AC load[21]. The battery banks are connected on DC side through controlled DC to DC converter as already proposed in [22]. Another option of connecting battery bank on ACside through a controlled AC-DC converter for balancing the power requirement of load and generation from the SPV system has been proposed and compared with configuration of [22] in this paper. For both the configurations the sliding mode control has been employedfor the control of the output AC voltage of the CHBMLI as was done in [22].

2. System Topology

Two types of topologies for SPV system with seven-level CHBMLI is considered here. The battery banks are connected at DC side through a controlled DC to DC converter in the first configuration [22] and in the second configuration as proposed in this paper the battery banks are connected on AC side through controlled AC-DC converter. The role of batteries in both the cases is for balancing the power requirement of load and generation from the solar PV system.

2.1. Configuration A: The battery banks are connected at DC side through controlled DC to DC converter [22]

The schematic block diagram of SPV fed CHBMLI for standalone framework appears in Figure 1. Three boost/step-up DC to DC converters are employed throughevery module of the array for MPPT under varying radiation levels. Signals B_1, B_2 and B_3, produced from the MPPT controllers, for switching control of the DC-to-DC converter. For control of voltage on the load side, the DC link voltage of each H-bridge uses droop control (V_{Load}/V_d), simultaneously. The voltages V_{dc1}, V_{dc2}, V_{dc3}represents the DC link voltages on DC link capacitors C_1, C_2, C_3, respectively, and V_{Load} is the load voltage. The voltages variation in V_{dc1}, V_{dc2}, V_{dc3} are indicative of the control of the voltages along with power in standalone mode operation [22].

The storage device stores/supplies the surplus/required power when the load has reduced/increased or the generation from solar power increases/reduces. The battery is

connected through a bidirectional converter as well as buck/boost converter to charge/discharge the battery, correspondingly.

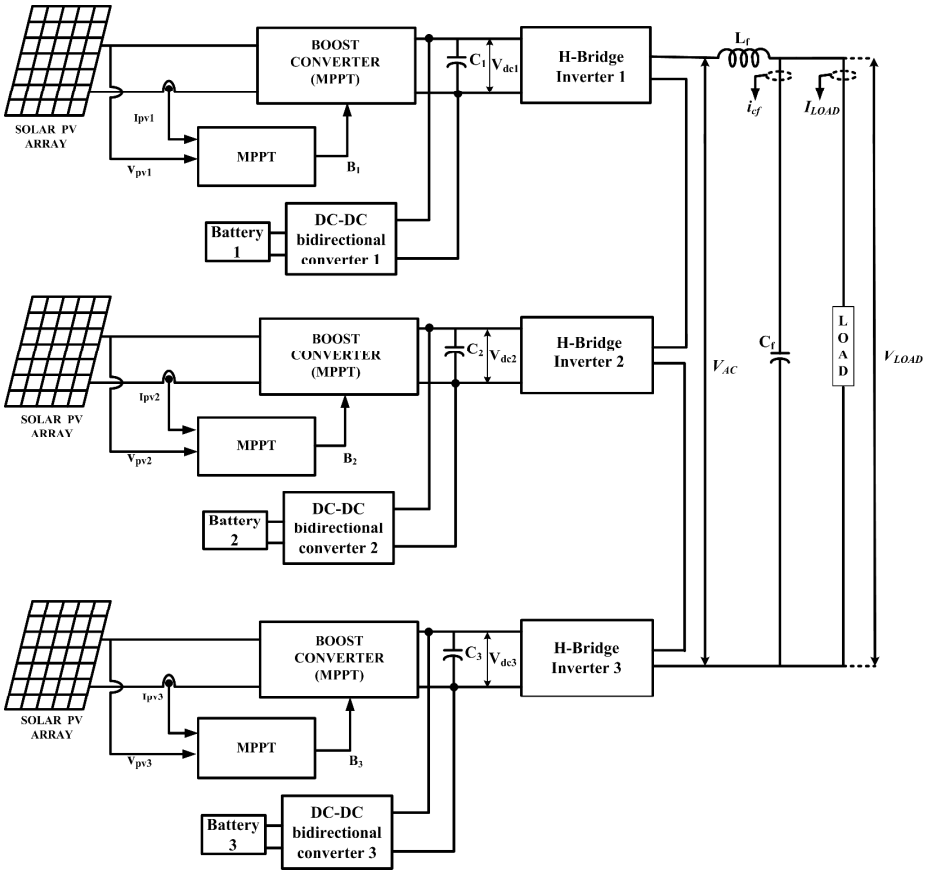


Figure 1. Block diagram of SPV array poweredCHBMLI with battery bank connected on DC side [22].

2.2. Configuration B: The battery banks are connected on AC side through controlled AC-DC converter

In this configuration ofSPV array fed CHBMLI, the battery bank is connected through the AC-DC converter as shown in Figure 2. Where, I_{pv1}, V_{pv1}, I_{pv2}, V_{pv2}, and I_{pv3}, V_{pv3}, are the currents and voltages provided from the three SPV arrays, respectively. The boostconverters are again employed here for the MPPT. The DC-DC converter outputs suppliesthe DC-link of the H-bridges. The currents I_{LOAD}, i_{cf} and I_{SH} are the current of the load, filter capacitor C_f and battery, respectively; V_{LOAD} is the voltage across filter capacitor C_f. The inductor (filter) is couplednext to the output of the CHBMLI and is denoted by L_f. A sliding mode voltage control technique is used to maintain load voltage V_{LOAD}through the filter capacitor C_f. A current control method is employed totrack the battery charging reference current I_{SH}.The SPV modules are connected in series and parallel to make an array for large power transfer. The DC-DC converter is used toobtain the maximum power

from the SPV array, using perturb and observe (P&O) algorithm. The algorithm adjusts the duty cycle to achieve maximum power point (MPP) [2].

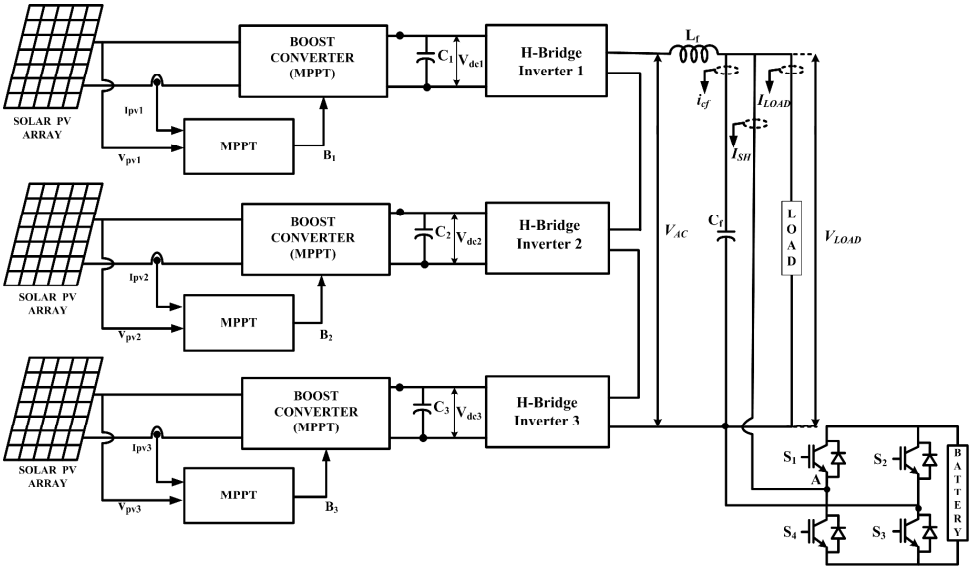


Figure 2. Block diagram of SPV array fed seven-level CHBMLI with battery bank connected on AC side.

For obtaining controlled sinusoidal waveform with good dynamic performance, the sliding mode control is used on AC side. The three SPV array including MPPT controlled boost converter shown in Figure 2 makes isolated DC sources for the CHBMLI. The switches used in the three H-bridges are (S_{11}, S_{12}, S_{13}, S_{14}), (S_{21}, S_{22}, S_{23}, S_{24}) and (S_{31}, S_{32}, S_{33}, S_{34}), respectively.

3. Control Techniques

3.1. Control Strategy for Configuration A

Inner voltage control loop as shown in Figure 3 controls the voltage at the load[22], [23]. The reference voltage V^*_{Load} is set by the deviation in V_d from reference V_{dref}. The reference voltage can be obtained as follows.

$$V^*_{Load} = V_{Load} + k(V_{dref} - V_d) = V_{Load} + k\Delta V_d \quad (1)$$

Where,*k*isa droop constant. The SMC is utilized to track the reference load voltage V^*_{Load}. The sliding surface condition [5] can be achieved in the VSI as follows.

$$\sigma(v_{Load}, t) = K_1(v^*_{Load} - v_{Load}) + K_2(\dot{v}^*_{Load} - \dot{v}_{Load}) = 0 \quad (2)$$

Where K_1, and K_2, are the sliding gain factors; $v_{Load}$and v^*_{Load} are the instantaneous values of the reference voltages. The next term in (4) exists defined through derivatives of $v_{Load.}$ and v^*_{Load}.

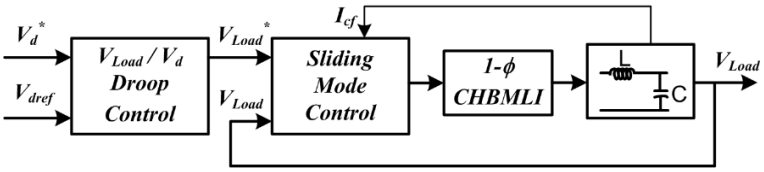


Figure 3. DC link voltage droop control block. (* indicates set values).

The manuscript [22], [23]demonstrates the outer power control loop which adjusts power into the framework. Following this the powerbalance and voltagecontrol can be achieved in the standalone system. The voltage across theDC link capacitor, power, and AC voltage across the load are controlled based on the solar PV output. The RMS estimation of the AC voltage is obtained within the predefined limits. In case the voltage is crosses the limits, another reference is set which is tracked by the VSI using SMC technique.

3.2. Control Strategy for Configuration B

The power produced by the SPV arrays using MPPT is supplied to the standalone load via the multilevel inverter for a desired load voltage V_{LOAD} which is controlled by the sliding mode control. The balance power needs to be exchanged by suitably controlling the current I_{SH} into the battery. Fig. 4(a) shows the SMC to control the output reference voltage using CHBMLI.

$$V^*_{Load} = V_{Load}\sin(\omega t) = V_{Load}\sin(2\pi ft) \tag{3}$$

Where, reference voltage has magnitude V_{Load} (rms) and frequency 50 Hz, $\omega = 2\pi f$

For equation (1), filter capacitor reference current $I_{cfref}$is defined as below.

$$I_{cfref} = C_f \frac{dV^*_{Load}}{dt} = 8\times10^{-6}\times2\pi f\times V_{Load}\cos(2\pi ft) = 0.0025\times V_{Load}\cos(2\pi ft) \tag{4}$$

Instantaneous reference values defined in (3) and (4), are continuously compared with the actual load voltage V_{LOAD} and filter capacitor current I_{cf}, using the difference to produce the two errorsV_{err} and I_{cferr}. The errors are multiplied with the sliding gain coefficients to generate the sliding function, which is then compared with the carrier signals V_{c1}, V_{c2} and V_{c3} for the H-bridges 1, 2 and 3, having phase angles of 0^o, 60^o and 120^o, respectively. The output pulses are produced at the frequency, of the carrier signal. Each H-bridge will produceathree-level output $+V_{dc}$, 0, $-V_{dc}$. The cascading of three H-bridges will produce the output of seven-levels $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$.

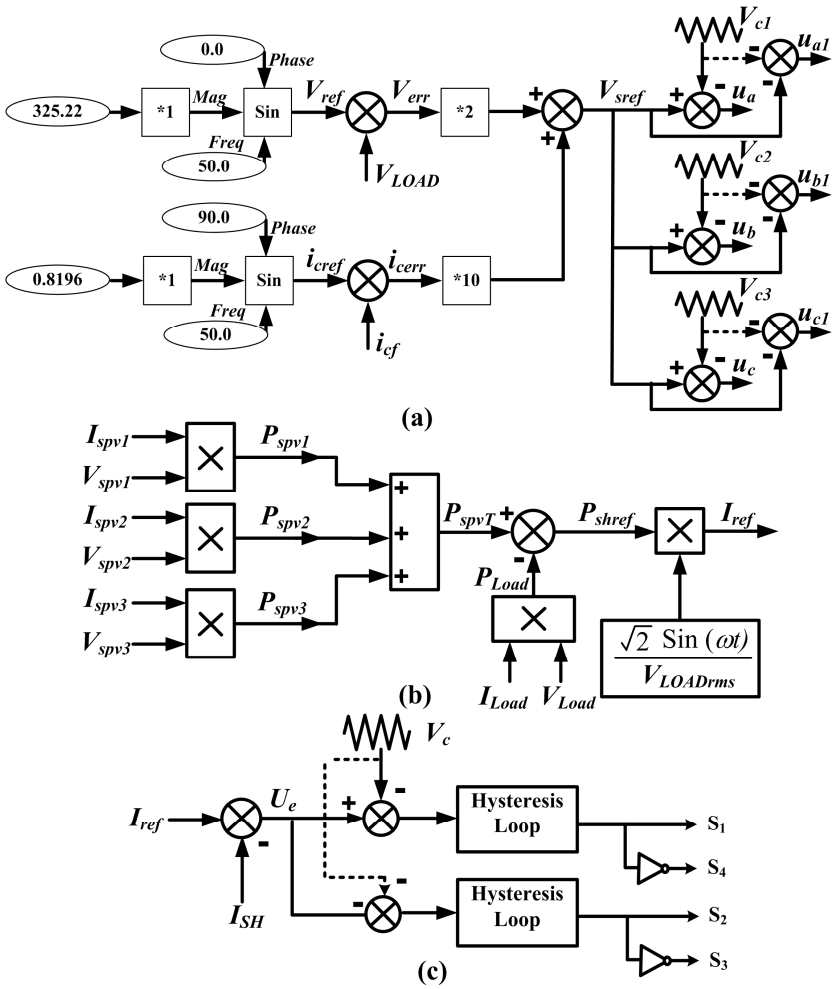


Figure 4. Control circuit for implementing sliding mode voltage control for seven-level inverter and three-level converter current control, (a) seven-level inverter current control, (b) reference current generation, (c) carrier based current control method.

The reference for the battery current I_{SH}can be obtained by subtracting the entire SPV power and the load power discussed below.

$$P_{spv1} = I_{spv1} \times V_{spv1} \tag{5}$$

$$P_{spv2} = I_{spv2} \times V_{spv2} \tag{6}$$

$$P_{spv3} = I_{spv3} \times V_{spv3} \tag{7}$$

Where, P_{spv1}, P_{spv2} and $P_{spv3}$are the powers generated from the three SPV arrays, as demonstrated in Figure 4 (b). Now the complete SPV powerP_{spvT}can be defined using equations (5)-(7).

$$P_{spvT} = P_{spv1} + P_{spv2} + P_{spv3} \tag{8}$$

$$P_{LOAD} = V_{LOAD} \times I_{LOAD} \tag{9}$$

The complete battery powerP_{shref}can be defined as a difference of equation (8) and (9).

$$P_{shref} = P_{spvT} - P_{LOAD} \tag{10}$$

To generate the shunt current for battery reference I_{ref}, following can be employed [24].

$$I_{ref} = \frac{\sqrt{2}P_{shref}\sin(\omega t)}{V_{LOADrms}} \tag{11}$$

Where, $V_{LOADrms}$ is the RMS of load voltage V_{LOAD}, the term sin(ωt) is a unit template of the voltage achievedby employing phase locked loop through a template of load voltage V_{LOAD}. The shunt current for battery I_{SH} is supposed to be in-phase with the load voltage [24]. Reference current for battery is illustrated in Figure 4 (b).

The carrier based current control methodemployed produces the reference asdemonstrated in Figure 4 (c) [9]. $I_{ref,}$ is producedusing (9), along with shunt current for battery I_{SH}. The difference of two produces an error function $U_e$which is compared with the carrier signal V_c for the H-bridges. This signal passes through a small hysteresis loop with a band limit of ±h [21].

4. Simulation Results

The SPV standalone systemwith CHBMLI and battery management has been simulated through PSCAD 4.2.1 platform. The control algorithm as discussed in previous section is used forthe voltage controlalong withpower balance. The system parameters employedduring the simulation is listed in Table I and SPV parameters are listed in Table

II. The module parameters are defined as V_{MPP} = 29.90 V, I_{MPP} = 8.20 A,V_{OC} = 38.23 V, I_{SC} = 8.67 A.

TABLE I. SYSTEM SIMULATION PARAMETERS

Simulation parameters	Numericalvalue
DC link voltage at 1000 watts/m^2 radiation levels	150 V
Switching frequency	01.25 kHz
Frequency of system	50 Hz
DC-link Capacitor	1470 µ F
Load voltage	325.25 V (peak)
Filters Capacitor	8 µF
and Inductor	10 mH

TABLE II. SIMULATION PARAMETERS FOR SOLAR PV ARRAY

Simulation parameters	Numericalvalue	
Voltage at MPP V_{MPP}	89.9 V	Standard Test Conditions
Current at MPPT I_{MPP}	8.2 A	(STC):
Open circuit voltage V_{OC}	114.69 V	Temperature, T = 25^{0}C
Short circuit voltage I_{SC}	8.67 A	Radiation, G = 1000 W/m^2

The capacitor voltage and current tracking through sliding mode control for configuration-Ais demonstrates in Figure 5 [22], with Figure 5 (a) demonstrate the tracking of reference voltage. Similarly, Figure 5 (b) demonstrates the tracking of reference capacitor current. The seven-level voltage generated through CHBMLI is shown in Figure 6.

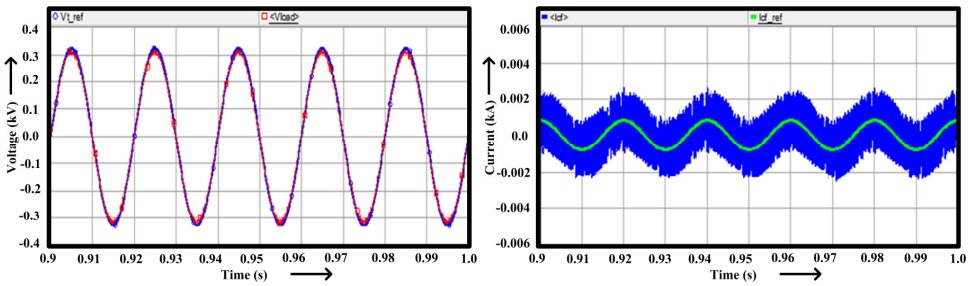


Figure 5. Sliding mode control (a) capacitor voltage and (b) capacitor current tracking.

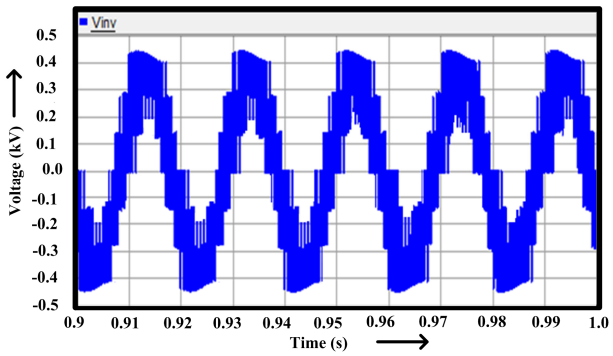


Figure 6. Seven-level inverter output voltage.

The simulation results for Configuration Aare shown in figures 7, 8 and 9. Figure 7(a), demonstrates the deviation in load from 45-36Ω at time t = 0.8 second and after that to 20Ω at time t = 1.2 second. The tolerance in voltage considered is±(10%) of 230V, i.e., V_{min} = 207V and V_{max} = 250V. With increment in load leads to drop in voltage. The power control loop becomes an integral factor and balance power remains supplied from the battery as well as the voltage is controlledwithin reasonable limits.

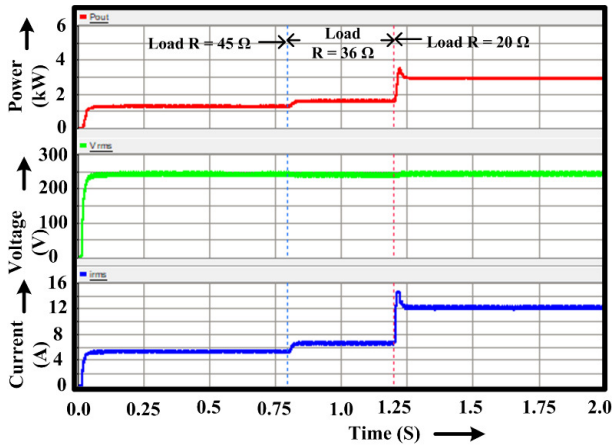


Figure 7. (a) Output power, (b) voltage, and (c) current, at load.

Output power is given by P = VI.

Case I: for, t < 0.8 sec, P1 = 250×6 ≈ 1.5 kW

Case II: for, 0.8 sec < t < 1.2 sec, P2 = 240×7 ≈ 1.68 kW

Case III: for, t > 1.2sec, P3=250×13 = 3.25 kW

Subsequently, P1 = P2, for t< 1.2 sec, .i.e., power remains adjusted throughadjustment ofV_{pcc}. Figure 7(b). P3 > P2 or P1, for t> 1.2 sec as well asremainder of the power is

supplied from the battery to bring the voltage in bounded limits. Figure 7(c) explainsload current variations with the load.

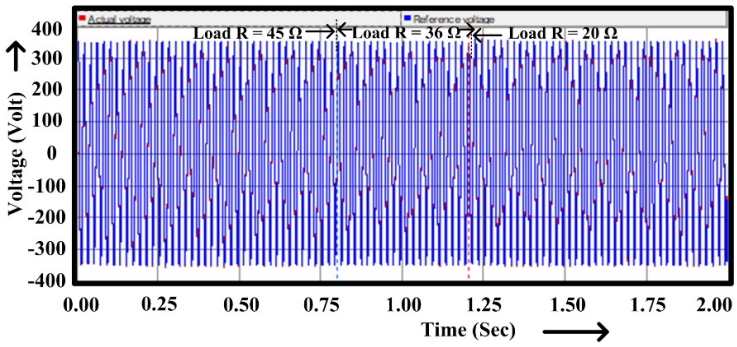


Figure 8. Load voltage tracking by inverter using SMC method.

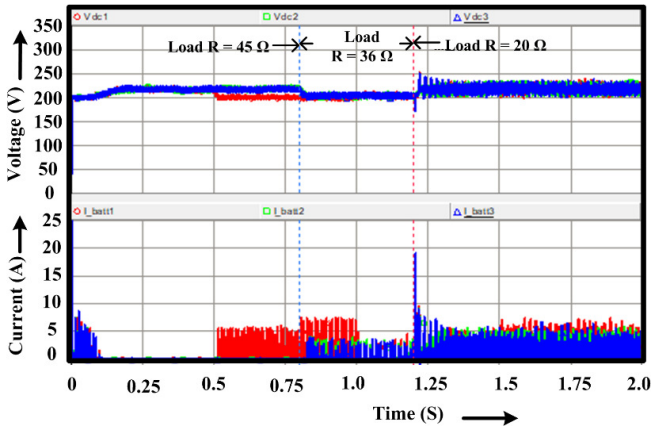


Figure 9. (a) DC link voltages and (b) battery currents.

Figure 8 demonstrates the tracking of the reference voltage obtained through the droop controller. The voltage shifts from 350V (p-p) to 340V (p-p) at t = 0.8 sec and changes back at t = 1.2sec to 350V (p-p). The increase in voltage is visible in Figure 8. Figure 9 demonstrates the change in DC link capacitor voltage. The battery provides the current at time t = 1.2 second once voltage limit is surpassed as visible in Figure 9 (b).

The figures 10, 11, 12 and 13 shows the simulation results for the Configuration B. Figure10shows proposed system performance under different load conditions. Figure 10 (a) shows power at a different stage: Like load power, inverter output power, PV power after MPPT, power at DC link capacitor and PV power. Figure 10 (b) shows voltage tracking at MPPT. Figure 10 (c) shows ac load voltage and load current. Figure 10 (d) show shunts current for battery reference generation and tracking along with tracking error. It is seen

from Table III that the load current decrease when the shunt current for battery increases and vice versa.

TABLE III. POWER LOAD VARIATION.

Load	P_{INV} (watts)	P_{LOAD} (watts)	$P_{BATTERY}$ (watts)
R=25 Ω , L=0.002 H	2153.37	1961.70	190.50
R=30 Ω , L=0.002 H	2009.92	1687.44	308.89
R=35 Ω , L=0.002 H	1878.42	1457.62	398.09
R=40 Ω , L=0.002 H	1760.64	1280.06	476.82

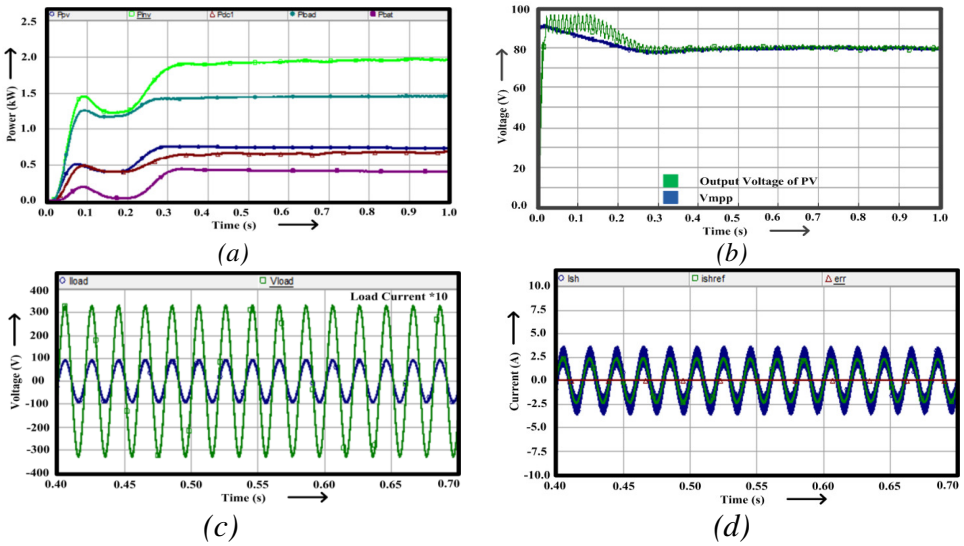
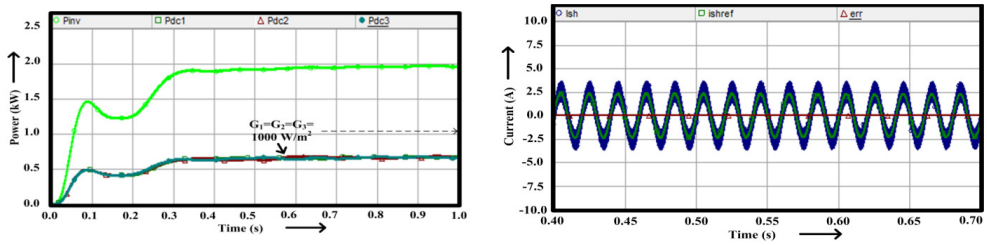
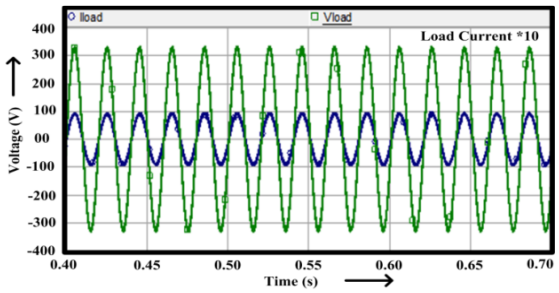


Figure 10. For R=35 Ω and L=0.002 H (a) power at different stages, (b) MPPT plot, (c) inverter load voltage and current and (d) shunt current for battery reference generation and tracking along with tracking error.

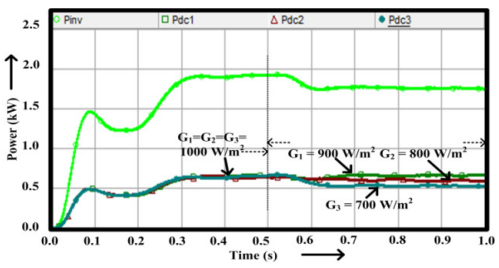




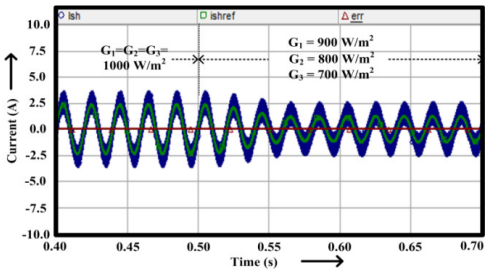
(c)

Figure 11. Under normal solar irradiation condition (G_1= G_2 = G_3 =1000W/m^2), R=35 Ω and L=0.002 H (a) power at different stage in experiment setup, (b) shunt current for battery reference generation and tracking along with tracking error and (c) inverter load voltage and current.

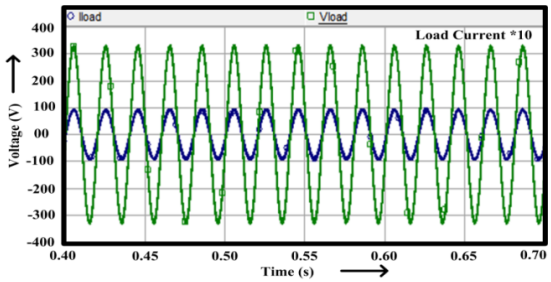
Figure 11 (a) depicts the net power generated by the solar arrayconsidering the fact that all solar modules have equal irradiation levels (G1= G2 = G3 =1000W/m^2). Considering the control strategy, all the DC link voltages settle down at the same level, alongside injecting a constant amount of power to the AC side by the shunt current with peak value I_{sh} = 2.5 Amp, as shown in Figure 11 (b). The sliding mode control is utilized in the CHBMLIto control the output voltage, V_{Load} = 325.22 V, over the load terminal and the resulting in peak loads current I_{Load} = 9.5 Amp, as appeared in Figure11 (c). For evaluating the transient condition of the proposed control strategy, solar irradiation level has been varied for each solar module (G1=900 W/m2; G2= 800 W/m2; G3=700W/m2).



(a)



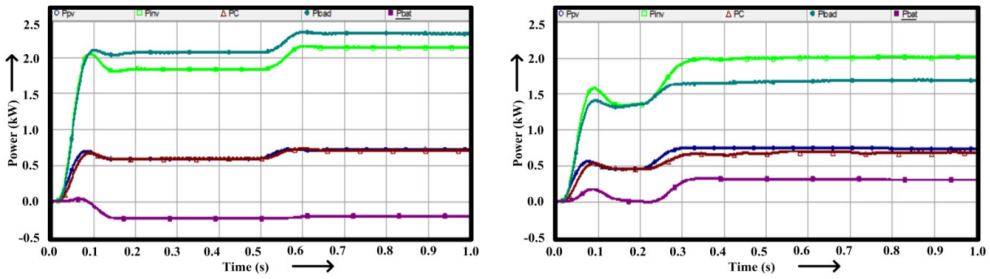
(b)



(c)

Figure 12. Under partial shading condition (G_1=900 W/m^2; G_2= 800 W/m^2; G_3=700W/m^2), R=35 Ω and L=0.002 H (a) power at different stages, (b) shunt current for battery reference generation and tracking along with tracking error and (c) inverter load voltage and current.

The corresponding changes in the total power output and the hysteresis current control tracking for the test case have been depicted in Figure 12(a) and 12(b), respectively. In this shunt current with peak value I_{sh} = 2.5 Amp, decrease to peak value I_{sh} = 1.2 Amp. Figure12 (c) demonstrates the load terminal voltage as well as current of the CHBMLI, which shows that the load terminal voltage and current are changes under dynamic change in environmental conditions. Further, the possibility of the suggested scheme has been validated by analysing the power level of the different power components involved, like load power, inverter output power, PV power after MPPT, power at DC link capacitor and PV power.



(a) *(b)*

Figure 13. Power at different stages, (a) battery unit is operating under discharging mode and, the (b) battery unit is operating under charging mode.

Figure 13 shows proposed system performance under different load conditions. Figure 13(a) shows that the inverter generated power is less than the load power, battery unit is operating under discharging mode to meet power demand and vice-versa. Figure 13(b) shows that the inverter generates power more than the load power; battery unit is operating under charging mode to use extra power to charge the batteries.

5. Conclusion

The implementation of the SPV fed seven-level CHBMLI in standalone mode with different converter configuration and battery management has been demonstrated through the PSCADE 4.2.1. Generated PV power needsto be transferred towards the load via the inverter as well asleftover power is consumedby the batteries. For integrated operation, the batteries are used on the DC side in the first topology and on AC side in another topology. Outcomesdemonstrates the effectivepower management of the entire system through the proposed strategy. The use of CHBMLIboosts the power limits as well as power quality of the output. It also helps in transformer less solar power management in standalone system as well as power redundancy. Further, the effect of varying solar irradiation level on the operating system has been illustrated. The DC side battery system can be preferred when standard battery charge controller through bidirectional DC/DC converter is available, however it requires multiple units. The AC side battery system involves a smaller number of components and complexity and reduces an overall size of the system;however, it requires controlled AC/DC converter.

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References

[1] R. Majumder, S. Chakrabarti, G. Ledwich and A. Ghosh, "Control of battery storage to improve voltage profile in autonomous microgrid," IEEE Power and Energy Society General Meeting, 1-8, (2011).
[2] N. Femia, G. Petrone, G. Spagnuolo and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," IEEE Trans. Power Electron., 20 (4), 963- 973, (2005).
[3] T. Dineshkumar and M. Subramani, "Design and implementation Maximum Power Point Tracking in photovoltaic cells," International Conference on Energy Efficient Technologies for Sustainability (ICEETS 2013), 792-795, (2013).
[4] N. Femia, G. Petrone, G. Spagnuolo and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," IEEE Trans. Power Electron., 20 (4), 963- 973, 2005.
[5] K. Harini and S. Syama, "Simulation and analysis of incremental conductance and Perturb and Observe MPPT with DC-DC converter topology for PV array," IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT 2015), 1-5, (2015).
[6] M.A. Elgendy, B. Zahawi, D.J. Atkinson, "Evaluation of perturb and observe MPPT algorithm implementation techniques," 6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012), 1-6, (2012).
[7] L. Zhang and S. Qiu, "Analysis and implementation of sliding mode control for full bridge inverter," International Conference on Communications, Circuits and Systems (ICCCAS 2005), 2, 1384, (2005).
[8] S. K. Gudey and R. Gupta, "Second order sliding mode control for a single-phase voltage source inverter," IEEE Region 10 Conference (TENCON 2014), 1-6, (2014).
[9] S. K. Gudey; R. Gupta, "Reduced state feedback sliding-mode current control for voltage source inverter-based higher-order circuit," IET, in Power Electronics, 8 (8), 1367-1376, (2015).
[10] E. Alarcon-Gallo, L.G. de Vicuna, M. Castilla, J. Miret, J. Matas, A. Camacho, "Decoupled sliding mode control for three-phase LCL VSI operating at fixed switching frequency," IEEE International Symposium on Industrial Electronics (ISIE 2012), 1572-1578, (2012).
[11] GoldvinSugirthaDhas, S. N. Deepa, "Fuzzy logic based dynamic sliding mode control of boost inverter in photovoltaic application," J. Renewable Sustainable Energy 7(4), 043133 (2015).

[12] T. Porselvi, R. Muthu, "Comparison of Cascaded H-Bridge, Neutral Point Clamped and Flying Capacitor multilevel inverters using multicarrier PWM," Annual IEEE India Conference (INDICON 2011), 1-4, (2011).

[13] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L.G. Franquelo, Wu Bin, J. Rodriguez, M.A. Perez and J.I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," IEEE Transactions on Industrial Electronics, , 57 (8), 2553-2580, (2010).

[14] B. Raj Kiran, M. Jayaraman, V.T. Sreedevi, "Power quality analysis of a PV fed seven level cascaded H-bridge multilevel inverter," International Conference on Advanced Communication Control and Computing Technologies (ICACCCT 2014), 281-285, (2014).

[15] R.K. Antar, B.M. Saied, R.A. Khalil, "Using seven-level cascade H-bridge inverter with HVDC system to improve power quality," First National Conference of the Engineering Sciences (FNCES 2012), 1-7, (2012).

[16] S. Albert Alexander, T. Manigandan, "Digital control strategy for solar photovoltaic fed inverter to improve power quality," J. Renewable Sustainable Energy 6, 013128 (2014).

[17] G.H. Bode, D.G. Holmes, "Implementation of three level hysteresis current control for a single phase voltage source inverter," 31st Annual Conference of the IEEE on Power Electronics Society (PESC 2000), 1, 33-38, (2000).

[18] S. Gautam and R. Gupta, "Unified time-domain formulation of switching frequency for hysteresis current controlled AC/DC and DC/AC grid connected converters," IET, in Power Electronics, 6 (4), 683-692, (2013).

[19] M. Lafoz, I.J. Iglesias, C. Veganzones and M. Visiers, "A novel double hysteresis-band current control for a three-level voltage source inverter," 31st Annual Conference of the IEEE on Power Electronics Society (PESC 2000), 1, 21-26, (2000).

[20] Lo Yu-Kang, Chiu Huang-Jen and Ou Sheng-Yuan, "Dual hysteresis loops for a high-performance four-switch boost rectifier," 26th Annual Conference of the IEEE on Industrial Electronics Society (IECON 2000), 4, 2626-2628, (2000).

[21] R. Gupta, A. Ghosh, and A. Joshi, "Switching characterization of cascaded multilevel-inverter-controlled systems," IEEE Trans. Ind. Electron., 55 (3), 1047–1058, (2008).

[22] A. K. Singh and R. Gupta, "Integrated Battery Management Configurations for Standalone Solar PV fed CHBMLI," *2020 IEEE International Conference on Power Electronics, Drives and Energy Systems(PEDES)*, 2020, pp. 1-5 (2020).

[23] V. Kumar, R. Gupta, "Voltage control and power balance in the standalone microgrid supported from solar PV", 2016 IEEE Region 10 Conference (TENCON), Singapore, pp. 1284-1288, Dec 2016.

[24] R. Gupta, "Generalized Frequency Domain Formulation of the Switching Frequency for Hysteresis Current Controlled VSI Used for Load Compensation," IEEE Trans. Power Electron., 27 (5), 2526-2535, (2012).