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CMOS Based Voltage Reference Designs for Sub - 1V



Abstract: - This review paper presents an analysis of the most recent advancements in sub-1V voltage references, addressing the growing demand for ultra-low power consumption and high precision in modern integrated circuits (ICs). Voltage references are critical components in numerous applications, including IoT devices, wearable electronics, and energy-harvesting systems, where power efficiency and accuracy are paramount. It briefly discusses the challenges associated with designing voltage references at such low voltages, such as limited headroom, reduced noise margin, and process variations. Topics include high-order curvature compensation, modified differential pair configurations, and energy-efficient solutions for integrated energy harvesting. These advancements enhance precision and reliability in low-voltage circuits, paving the way for sustainable, low-power electronics and compact devices in the modern digital landscape. It emphasizes the importance of benchmarking different designs against criteria such as power consumption, line regulation, temperature stability, and supply voltage rejection ratio (PSRR). The paper includes insights into the state-of-the-art sub-1V voltage reference designs, identification of design trade-offs, and recommendations for future research directions. It underscores the importance of continuous innovation in voltage reference design to address the evolving requirements of ultra-low power electronics. The study here is setting the stage for a detailed analysis of the latest developments in sub-1V voltage references.

Keywords: CMOS Voltage Reference, Sub-1V Operation, Bandgap Reference Architecture, Differential Pair Compensation, Instrumentation Amplifiers, Switched Capacitors Designs, Low Power Electronics, Energy Harvesting Applications, Threshold Monitoring Techniques, Semiconductor Technology Innovation

I. INTRODUCTION

In the semiconductor domain, the quest for ultra-low voltage operation has sparked innovative strides in CMOS (Complementary Metal-Oxide-Semiconductor) voltage references. This research paper embarks on a comprehensive journey into advanced CMOS bandgap voltage references functioning at sub-1V levels. Commencing with a foundational overview, the work elucidates the fundamental principles underpinning Sub-1V Linear CMOS Bandgap Voltage References, laying the groundwork for the study. It then traverses the intricate landscape of bandgap voltage reference architectures, introducing specialized designs such as Sub-1V Supply Bandgap Voltage References Based on Asymmetric Differential Pair and Low-Voltage Sub-1V CMOS Bandgap with Modified Differential Pair [1,2]. The current state of Sub-1V voltage reference circuits reflect a dynamic landscape characterized by significant advancements and ongoing research endeavors. These circuits, designed to provide stable and accurate voltage references at ultra-low voltages, play a crucial role in various applications demanding minimal power consumption and high precision [3]. Recent developments in Sub-1V voltage reference circuits have been driven by the escalating demand for energy-efficient electronics, particularly in fields such as IoT devices, wearable technology, and energy harvesting systems. Engineers and researchers have focused on enhancing the performance metrics of these circuits, including power efficiency, line regulation, temperature stability, and supply voltage rejection ratio (PSRR). In addressing real-world applications, the research extends to a Sub-1V CMOS Instrumentation Amplifier customized for seamless integration with sensors, demonstrating the practical significance of these advancements [4]. Additionally, the paper delves into compensation techniques, spotlighting New Curvature-Compensation Techniques and innovative approaches like Modified Differential Pairs [5]. Venturing into switched capacitor designs, the study explores Sub-1V CMOS Switched Capacitor Voltage References, emphasizing their high output current capabilities [6,7]. Moreover, the research delves into specialized realms, encompassing an Ultra-Low-Power Active AC-DC CMOS Converter tailored for integrated energy harvesting applications and a MOS Threshold Monitoring-Based Voltage Reference operating at sub-1V levels. This holistic exploration not only enriches our comprehension of CMOS voltage references but also charts the course for pioneering applications in low-power electronics and sensor interfaces. Existing systems primarily rely on rigid static filters [8,9] that categorize products based on specific feature values. This approach fails to capture

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a user's willingness to compromise on certain features (e.g., price) for more desirable ones (e.g., higher performance) [10].

Lately innovation in the domain of Sub 1V voltage reference designs using advanced CMOS and FinFET Technologies [11], innovative circuit techniques such as sub-threshold operation, dynamic biasing, and modified differential pairs to overcome challenges associated with designing voltage references at ultra-low voltages have been developed. The integration of Sub-1V voltage reference circuits with sensor interfaces, such as instrumentation amplifiers, has facilitated seamless interfacing with sensors, enhancing the applicability of these circuits in real-world scenarios [12]. The development of advanced compensation techniques, including curvature-compensation techniques, has contributed to enhancing the linearity and stability of Sub-1V voltage reference circuits. Researchers have introduced specialized architectures tailored for Sub-1V voltage references, such as asymmetric differential pairs and switched capacitor designs, to achieve improved performance and efficiency. The review work will cater the insights into cutting-edge sub-1V voltage reference designs, highlighting design trade-offs and offering recommendations for future research, all aimed at meeting the evolving demands of ultra-low power electronics.

II. CIRCUIT DESCRIPTION

In the pursuit of advancing sub-1V CMOS bandgap voltage references, a synergistic circuit design is curated by amalgamating 3 innovative features. The first key element is introducing a current mode structure with PTAT and CTAT current sources, coupled with high-order curvature compensation for heightened precision [5]. The second crucial aspect is leveraging an asymmetric differential pair for reference voltage determination, ensuring stability even at low supply voltages. This design encompasses variations with resistive dividers, external/internal bias, and diverse configurations with two current sources [2]. The third pillar is derived by integrating a single MOSFET core solution, inverter-like amplification, and switched capacitor bandgap core, offering stability and offset and flicker noise cancellation through Correlated Double Sampling (CDS). The circuit utilizes zero-threshold MOSFETs for a low-voltage source follower, ensuring high-output current sourcing [6].

Performance metrics showcase a typical output reference voltage of approximately 634.93mV at 27°C and 1.2V supply, with a low-temperature coefficient of 3.65ppm/°C across -40°C to 125°C. The design demonstrates autonomous start-up, and stabilization at 0.48V with 9.6 μA current at 27°C, making it applicable for portable electronics, advanced memory technologies, and low-power analog systems. This integrated circuit represents a cutting-edge approach, capitalizing on the strengths of each paper to deliver a sub-1V bandgap voltage reference with unprecedented precision, stability, and adaptability to low-voltage environments.

2.1 Conventional Bandgap Reference Circuits

The circuit [3], is implemented using standard digital CMOS technology, stands out for its adaptability to a wide voltage range, spanning from sub-1 V to 5 V, as shown in Fig 1. This versatility makes it particularly suitable for contemporary electronic devices with varying power supply requirements.

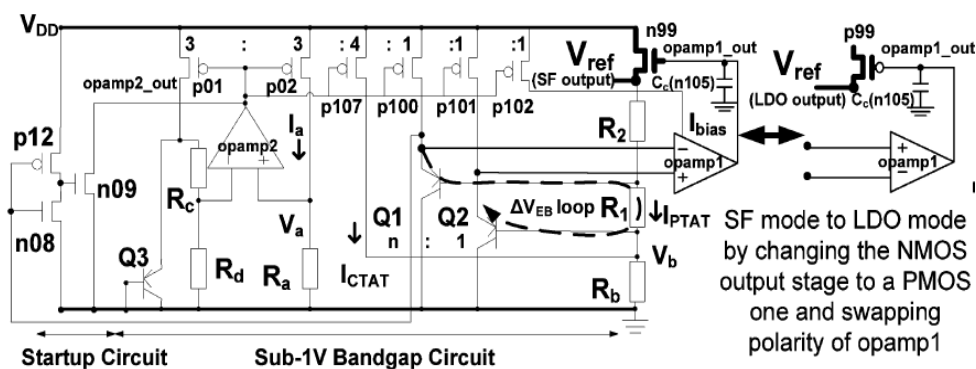


Fig. 1: Conventional Bandgap Reference Circuit [2]

In the circuit design, the authors employ a Low Dropout Regulator (LDO) architecture, which allows the reference voltage to be maintained even as the supply voltage drops close to the desired output voltage. This is crucial for applications where the power supply may vary. Additionally, the Source Follower (SF) mode is integrated, providing an alternative operational mode that enhances the circuit's adaptability. The SF mode is particularly advantageous for scenarios where a low-impedance output is required, ensuring stability and robust performance across different load conditions.

The detailed design includes the use of standard CMOS components, such as resistors, current mirrors, and operational amplifiers. The authors carefully optimize the circuit parameters to achieve low power consumption ($26 \mu\text{W}$) while maintaining a low output impedance. The circuit's dual-mode operation, combined with its efficiency and adaptability to a broad voltage range, positions it as a practical and valuable solution for stable sub-1 V voltage generation in modern electronic systems.

2.2 AFE Bandgap Reference Circuits

The Analog Front-End (AFE) circuits in these papers play a crucial role in interfacing sensors with integrated circuits, particularly in the context of IoT and sensor data acquisition applications. AFEs are essential components that bridge the gap between the analog signals from sensors and the digital domain of integrated circuits. They are responsible for conditioning, amplifying, and processing analog signals before conversion into digital data. The significance of AFE circuits lies in their ability to ensure high precision, low noise, and minimal power consumption, aligning with the energy-efficient and low-voltage requirements of modern electronic systems.

The CCIA [4] is designed to operate at sub-1V power supply levels. This AFE employs innovative techniques such as chopper modulation to significantly reduce noise, resulting in outstanding performance metrics. AFEs are integral in sensor data acquisition setups, acting as a critical element in various applications, including environmental monitoring and healthcare devices. The CCIA's efficient noise reduction and low-power attributes make it a transformative technology for reliable and energy-efficient sensor interfaces in the IoT landscape.

The low-voltage CMOS bandgap reference [7] which, in the broader context, is crucial for AFE systems. AFEs, being key components in sensor data acquisition, benefit from the modified differential pair architecture that simplifies biasing and eliminates the need for a tail current source. This design's flexibility in setting the reference voltage makes it well-suited for power-efficient AFEs in contemporary integrated circuits, addressing the growing demand for low-power operation in sensor-related applications.

The AFEs for energy harvesting applications [8] need to efficiently convert and rectify low input voltages. The active rectifier, comprising a negative voltage converter and an active diode, stands out for its adaptability to low input voltages and high conversion efficiency. This AFE holds promise for powering self-sustaining devices, contributing to developing autonomous systems with minimal environmental impact.

These AFE circuits represent advancements in sensor interface technology, offering solutions that align with the requirements of modern electronic systems, especially in the realms of IoT and low-power applications.

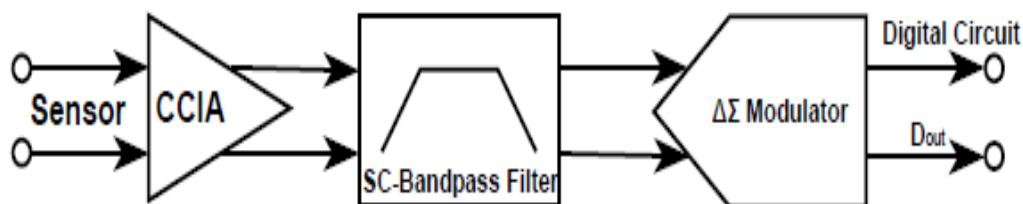


Fig. 2: Analog Front-End[5]

2.3 Improved Bandgap Reference Circuits

The CMOS bandgap voltage reference circuit [1], addresses a critical challenge in low-voltage integrated circuits. The innovative architecture employs two currents, one proportional to the diode's built-in voltage and the other proportional to the thermal voltage. Unlike conventional bandgap reference circuits limited to around 1.25V, this design operates efficiently at supply voltages below 1V, aligning with contemporary low-voltage trends. By

carefully configuring the input voltage nodes for the operational amplifier, the circuit achieves low-voltage operation without the need for complex amplifiers. The novel approach ensures stable voltage references in the sub-1V domain, marking a significant advancement in the field.

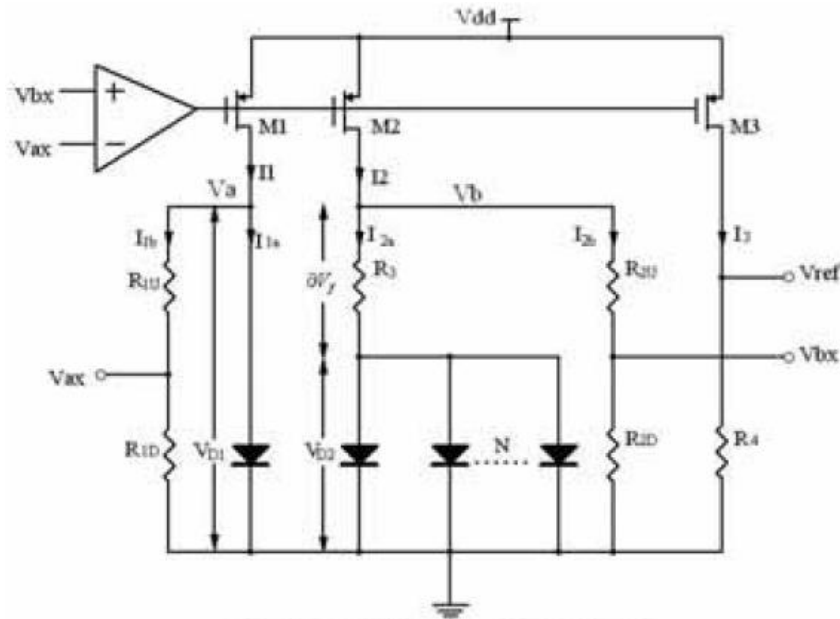


Fig. 3: Improved Bandgap Reference Circuit [1]

Similarly, the development of a capacitively-coupled instrumentation amplifier (CCIA) [4] designed for efficient interfacing with sensors in the Analog Front-End (AFE) system, achieves an impressive balance between high precision, low noise, and minimal power consumption. Leveraging innovative techniques such as chopper modulation, the CCIA significantly reduces noise, leading to outstanding performance metrics. With a total power consumption of $2.6 \mu\text{W}$, an open-loop gain of 87 dB, and a Noise Efficiency Factor (NEF) of 4, this CCIA sets a new standard for sensor interfaces in energy-efficient IoT devices.

As mentioned in [8], the two-stage design incorporates a negative voltage converter (NVC) and an active diode, forming an efficient full-wave rectifier. Operating in the subthreshold region, the AFE achieves high conversion efficiency and low power consumption, making it well-suited for energy harvesting applications. The circuit's adaptability to low input voltages and the active diode's high-speed nonlinear comparator function position this AFE as a promising solution for self-powered devices, ensuring optimal current flow and energy-efficient operation across a wide frequency range (5 Hz-10 kHz).

Experimental results conducted on the fabricated rectifier highlight its remarkable performance. The rectifier can handle input AC signals ranging from 0.5-1.2 V, achieving a maximum conversion efficiency of 94%. It operates across a frequency range of 5 Hz-10 kHz, delivering an output current of $30 \mu\text{A}$ with a minimal ripple of 40 mV. Notably, the rectifier exhibits low power consumption, ranging from 300-650 nW, ensuring energy-efficient operation.

The paper's findings contribute significantly to the development of self-powered devices by offering an active rectification solution that excels in efficiency and adaptability to low input voltages. The innovative circuitry and meticulous design make it a promising candidate for diverse energy harvesting applications, demonstrating its potential for powering autonomous systems sustainably.

2.4 New Curvature Compensation Techniques

Curvature compensation techniques are crucial in the design of CMOS bandgap voltage references, aiming to improve precision and stability, particularly in low-voltage applications. These techniques address challenges related to nonlinearity in temperature dependence and voltage variations.

The authors [5] address the challenge of achieving low voltage and high precision by incorporating a current mode structure with resistance division. The circuit utilizes MOSFETs in the sub-threshold region and a symmetric two-stage operational transconductance amplifier (OTA). The high-order curvature compensation ensures high precision with a low-temperature coefficient of 3.65 ppm/°C across a wide temperature range. The circuit's robust performance, including a typical output reference voltage of 634.93mV and a remarkable power supply rejection ratio (PSRR) of 63.8dB@DC, makes it suitable for portable electronic products and advanced memory technologies.

Similarly, the paper [9] presents a novel curvature-compensation technique for CMOS bandgap references designed for sub-1V operation. The authors propose using parasitic vertical bipolar junction transistors in the CMOS process to generate temperature-independent currents through current mirrors. These currents compensate for high-order temperature-dependent factors, ensuring stable low-voltage operation below 1V. Simulation results demonstrate a low-temperature coefficient of approximately 7.5 ppm/°C under a supply voltage of 1V. The sub-1V curvature-compensated CMOS bandgap reference eliminates the need for post-fabrication trimming and provides a practical solution for stable and accurate voltage references in low-power electronic devices.

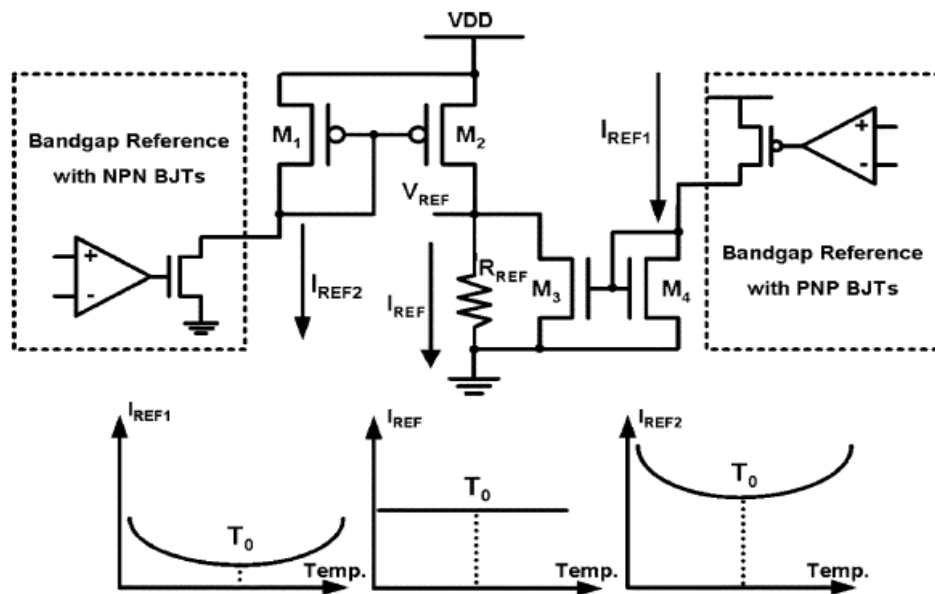


Fig. 3: New proposed Sub-1-V Curvature-Compensated Bandgap Voltage Reference Circuit[9].

III.

RESULT AND DISCUSSION

Precise analog circuits face complexities due to variations in threshold voltage (V_{TH}) and device characteristics [10]. Traditional bipolar junction transistor (BJT)-based voltage references encounter limitations in low-voltage applications. To overcome these challenges, the paper introduces the concept of a V_{TH} sensor capable of extrapolating the threshold voltage (V_{TH0}) of a single MOSFET at absolute zero temperature. However, existing V_{TH} sensor designs based on older CMOS processes struggle to maintain low-temperature coefficients (T.C.) in modern nanometer technology because the paper proposes a novel solution by presenting a new V_{TH} sensor circuit designed for sub-1-V operation in a 65-nm CMOS process. This innovative design employs a current-mode second-order temperature compensation technique to mitigate the nonlinear temperature effects of MOSFET gate-to-source voltage (V_{GS}) variations. By utilizing the different temperature characteristics of P+ diffusion and poly resistors, the circuit achieves second-order temperature compensation, effectively reducing the temperature coefficient (T.C.) of the circuit. Table 1 illustrates and compare different designs.

In practical terms, the proposed V_{TH} sensor circuit is fabricated and tested in a UMC 65-nm CMOS process. The results demonstrate its ability to generate a stable reference voltage close to the extrapolated V_{TH} for a low-threshold nMOS transistor at absolute zero temperature. The circuit exhibits a temperature coefficient (T.C.) ranging from 24.5 ppm/°C to 40 ppm/°C, over a temperature range of -40°C to 90°C, showcasing its robust

performance in various operating conditions. Furthermore, the design is scalable to different process technologies, ensuring resilience to both die-to-die (D2D) and within-die (WID) process variations.

CMOS based Band gap voltage reference circuit based on the desired specification have been designed and simulated using Cadence Virtuoso tool with the latest 65nm CMOS process, shown in Fig 4. The design simulates to validate required specifications of voltage reference. The circuit proposed is different from the state-of-the-art voltage reference circuits, as it will be generating multiple output voltages as reference which highly stable. To achieve tunability, various methods can be employed like digital to analog converter, trimming resistors, switched capacitor arrays or programmable gain amplifier, etc. The proposed output voltage references is on-chip tunable using concept of on-chip non-volatile programming of floating gate transistor. The proposed design output references will be on-chip, non-volatile programmable with the help of external voltages. The output references can be tuned from greater than 1V to sub 1V. Thus, the multiple output references can be used to provide stable power supply to several other circuits integrated in the chip. Basic features of the circuit are multiple output references, output references would be highly stable with variation in temperature and power supply. The proposed design output references can be on-chip tunable. The design will consume low power. The design will be highly integratable as based on CMOS technology. The chip area will be optimized and kept small as compared to other state of the voltage reference circuits. The circuit have been implemented before at 350nm CMOS technology using Cadence Virtuoso [13].

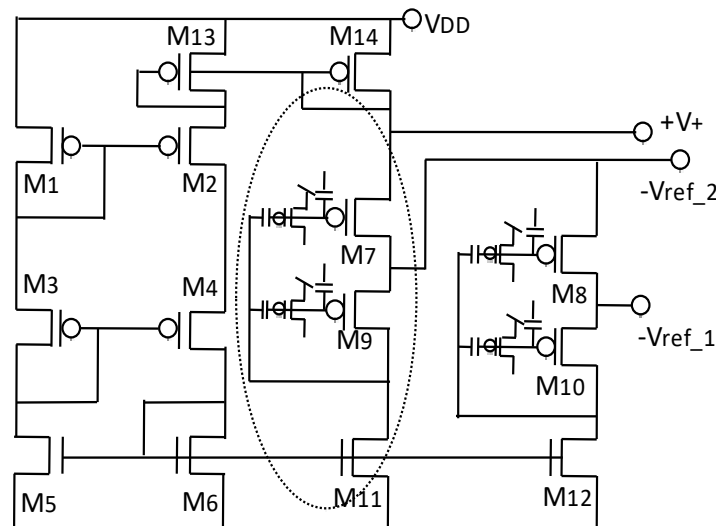


Fig. 4: Design of a Band gap Sub-1V Voltage Reference Circuit using 0.35um CMOS process [13]

In summary, this paper introduces an advanced V_{TH} sensor circuit specifically tailored for modern nanometer CMOS technology, providing stable voltage references and crucial process information while effectively addressing challenges related to temperature variations and process technology scaling. The proposed circuit's remarkable temperature stability and low-temperature coefficient make it highly suitable for a wide range of integrated circuit applications, ensuring reliable performance in diverse environments.

IV.

CONCLUSION

In summary, the research presented in this study marks a significant stride forward in the realm of CMOS bandgap voltage references operating below 1V. Through a comprehensive exploration, a spectrum of innovative circuit designs has been investigated, each contributing to the progression of low-voltage, low-power electronics. The study showcases a holistic approach to circuit design, weaving together cutting-edge features such as high-order curvature compensation, asymmetric differential pairs, and switched capacitor designs. These elements synergize to form a robust sub-1V bandgap voltage reference circuit with exceptional precision, stability, and adaptability to low-voltage environments. The performance metrics demonstrated by the proposed circuit are noteworthy, positioning it as a pioneering solution for a multitude of applications spanning portable electronics, advanced memory technologies, and low-power analog systems. Overall, this research not only pushes the boundaries of

CMOS voltage references but also lays the groundwork for further innovations in ultra-low voltage electronics. Through a thorough analysis of various circuit architectures, compensation techniques, and integration strategies, the paper underscores the significant progress made in achieving precision and efficiency at ultra-low voltage levels. The reviewed literature highlights a diverse array of innovative approaches, including advanced CMOS and FinFET technologies, novel circuit techniques, and specialized architectures tailored for Sub-1V operation. These developments have culminated in voltage reference circuits with remarkable precision, stability, and adaptability to low-voltage environments. Looking ahead, continued research efforts are poised to further refine and optimize Sub-1V voltage references, addressing remaining challenges and exploring new avenues for innovation. Moreover, the research extends beyond the fundamental circuit design, delving into specialized areas such as instrumentation amplifiers, energy harvesting applications, and curvature compensation techniques. The emphasis on practical applications, demonstrated through AFE circuits tailored for sensor interfacing and energy harvesting, highlights the real-world relevance of these innovations. The incorporation of new curvature compensation techniques further underscores the commitment to addressing challenges in precision and stability, crucial for the success of low-voltage integrated circuits. On-chip tunability with multiple output reference circuit can be designed for more advanced application where multiple supplies are required in the chip. With the tunable design high level of flexibility and integration ability can increase the yield. A tunable multiple output voltage reference circuit integrated on a single chip provides flexibility and efficiency in various applications, particularly in mixed-signal and analog circuits. This circuit typically consists of a voltage reference core and multiple output stages, each capable of generating a stable voltage reference. Multiple output stages are incorporated into the circuit, each designed to generate a specific voltage level. These stages can be individually tuned to adjust their output voltages, allowing for multiple reference voltages to be generated from a single core. To ensure accurate output voltages, feedback loops can be incorporated to monitor the output voltages and adjust the tuning parameters as needed. Applications of such circuits include data converters, power management systems, sensor interfaces, and precision analog circuits where multiple voltage references with adjustable levels are required. In essence, this comprehensive exploration not only enhances our understanding of CMOS voltage references but also lays the groundwork for future developments in sustainable, low-power electronics, and sensor interfaces. Designing such circuits involves careful consideration of factors like line regulation, load regulation, temperature coefficient, power consumption, and silicon area. Trade-offs between accuracy, power consumption, and complexity must be made to optimize the design for specific application requirements.

Table 1: Comparison Table

Parameters	[1]	[3]	[4]	[5]	[6]	[7]	[8]	[10]
T.C. (ppm/°C)	30.67 ppm/°C	34 ppm/°C	N/A	3.65 ppm/°C	N/A	7.91 ppm/°C	N/A	40 ppm/°C
Power Consumption	N/A	Around 26 μ W	2.6 μ W	29.2uW	N/A	60 μ W (at 27°C)	650 nW	290 nW (at 0.75 V)
Supply Voltage (V)	0.7V to 2V	Sub-1 V to 5 V	1-0.9	1.2V	0.7 V	Down to 0.95V	< 500 mV	0.75 - 1.2
Area (mm ²)	N/A	N/A	0.06	N/A	N/A	N/A	0.03	0.0198
Temperature Range	N/A	20°C to 120°C	N/A	-40°C to 125°C	-20 to 80°C	0°C to 150°C	N/A	-40 to 90
Technology	0.35 μ m CMOS	0.5- μ m Standard CMOS	130 nm Standard CMOS	0.13- μ m CMOS	0.18 μ m CMOS	UMC 0.18 μ m CMOS	CMOS (0.35 μ m XFAB)	65 nm
Reference Voltage	N/A	0.235 V	N/A	634.93 mV	0.483 V	620mV (at 27°C)	960 mV	N/A

Output Current (1 V Supply)	N/A	SF - 0.35mA	N/A	24.34 uA	200 μ A	N/A	30 μ A	N/A
Voltage Variation	N/A	N/A	N/A	N/A	N/A	7.91 ppm/ $^{\circ}$ C	N/A	N/A

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