[1] **Pankaj Kumar Sanda***
[2] **Anup Dey**
[3]**Rudra Sankar Dhar**

Performance assessment of monolayer Black Phosphorus DG-JLFET

Journal of Electrical Systems

Abstract: - Two-dimensional materials are very promising for ultra-short channel future devices. This paper investigates, for the first time, the viability of the junction less transistors based on 2-D materials for future state-of-the-art technology nodes. Specifically, we investigate the performance of a Junction less monolayer black phosphorus (BP) FET (JLFET) with 12nm gate length using ab initio quantum transport simulations. The electrostatic control mechanism of the device and various intrinsic static and dynamic characteristics of the device are studied. The results reveal that BP JLFET performance can fulfill the benchmark requirement of International Roadmap for Devices and Systems (IRDS 2021) for 2028 in terms of HP and HD applications. Therefore, JLFET based on 2D materials can be a promising alternative for nano scale future device applications..

Keywords: Subthreshold Swing, On/Off current, Phosphorene, Transconductance, Delay Time, Projected Local Density of State.

I. INTRODUCTION

Because of intensive downscaling, conventional silicon-based technology for metallic-oxide semiconductor field-effect transistors (MOSFETs) are gradually loosing the device application potentials due to various detrimental effects like power dissipations and short channel effect. Moreover, the scaling of advanced conventional MOSFET demands the use of advanced processing with multiple additive technology boosters, such as strain, high-k dielectrics with metal gate stacks, shallow junctions and the replacement of the silicon channel with materials having higher carrier mobility. Two-dimensional (2-D) materials have proven to be an excellent channel material. due to their dangling bond free interface and exceptional thinness, allow for nearly perfect electrostatic control while reducing the short channel effect [1-2]. However, unlike silicon-based device technology where the doping is done by the replacement of atoms in crystal lattice and essentially relying on statistical distributions of dopant atoms, in prevailing 2-D materials technology, transfer of charges from defects or molecular adsorbates in the vicinity to the 2-D layer is used for this purpose [2-4]. Hence controlling this precise 'effective doping' of these devices at this nano scale regimes pose a great difficulty in fabricating the junctions in devices. The stringent requirement of an ultra-steep doping profile at the metallurgical junctions restricts the scaling of the conventional MOSFETs. Therefore, field effect transistors having no metallurgical junctions at the source-channel and channel-drain interface were proposed to overcome the constraint of ultra-sharp doping profiles and higher thermal budgets to activate the dopants. Junction less FET (JLFET) structure attracted great attention recently as the drain, source, and channel are similarly doped, as a result, no junction is produced, resulting in ease of manufacture and cost savings. [4-6] and design simplicity, enables flexibility in the choice of materials for the gate electrode and gate oxide. Furthermore, JLFET outperforms conventional MOSFETs in terms of subthreshold swing, intrinsic speed, power dissipation, and enhanced thermal budget. [7-11]. Besides, JLFET are less sensitive in threshold voltages to variations with fabrication parameters and random dopant fluctuation effect [12]. Several studies have been published on JLFET to demonstrate these possible benefits. in the recent past for materials in their bulk state [11-12] demonstrating their merits. Thus, it is natural to anticipate that plugging the advantages of 2-D systems into the JLFET structures may produce even better device characteristics whose performance may meet the requirement set by IRDS for both HP and HD device. However, the potential for performance of junction less field-effect transistor based on 2-D materials as channel has not been investigated. so far and relatively scare in literature, because of the planar geometry of 2-D structures, which may not have a wrap-around gate shape and are frequently sought after for maximum electrostatic control in a device. In order to take advantages of well-established favorable characteristics of 2-D systems An effort is made in this paper to study the possibilities of 2-

[1] *Corresponding author: Department of Electronics and Communication Engineering, National Institute of Technology, Mizoram-796012, Aizawal, Mizoram, India, and Department of Electronics & Communication Engineering, Brainware University, Kolkata, West Bengal, India. e-mail: eternal_deny_crist@yahoo.com
[2] Department of Electronics & Communication Engineering, Jalpaiguri Government Engineering College, Jalpaiguri-735102, West Bengal, India and Government College of Engineering and Leather Technology, Kolkata, West Bengal, India
[3] Department of Electronics and Communication Engineering, National Institute of Technology, Mizoram-796012, Aizawal, Mizoram, India. e-mail: rudra.ece@nitmz.ac.in

D material-based JLFET design and evaluate important performance criteria for appraising their prospects in digital electronic applications.

In this paper, for the first time, we investigated a 2-D channel dual gated-JLFET (DG-JLFET), employing phosphorene as the device's model channel material, to evaluate the most important FET performance parameters using ab initio quantum transport simulations. [14]. The key figure of merits for static and dynamic performances is taken into account using the benchmark laid down in International Roadmap for Devices and Systems (IRDS2021) for both HD and HP technologies [15], with the primary goal of acquiring physical knowledge into the device's operations and potential performance limits. Here in, a symmetric double gate structure (DG-JLFET) is considered of p-channel JLFET with similar to assess their relative performance potentials. Among the various other 2-D materials phosphorene has been extensively researched due to their superior electronic properties like favorable band gap, high carrier mobility, and anisotropic electronic characteristics and high thermal stability [1]. Like graphene, phosphorene is a monolayer (ML) of bulk phosphorus in which individual atomic layers are stacked together by van der Waals interactions [3]. The puckered layer structure is formed by sp3 hybridization of the atomic orbital of the phosphorus atoms. Further, the band gap of multilayer phosphorene can be tuned by changing the thickness of the layer [6-7]. Li et al studied the performance of black phosphorus JFET [3] and shows its potential advantages for use in the future electronic device. As a result, various research on the performance of phosphorene-based MOSFET and TFET devices have recently been published in the literature. [4-9]. To ascertain the accuracy of our simulation we first verified our reproduced results for BP MOSFET with the results reported in the previous works before proceeding for JLFET simulations.

Black phosphorus (BP), one of the most stable phosphorus allotropes, has recently been reevaluated as an essential layered material (since 2014). When compared to 2D nanomaterials that have been extensively investigated, including graphene and transition metal dichalcogenides, 2D-BP has an advantage due to its finite, straight bandgap and strong charge-carrier mobility. Due to these qualities, 2D-BP is the best choice for near- and mid-infrared optoelectronics applications. Phosphorene's in-plane anisotropy, which is fundamental to its mechanical properties, is its most distinctive characteristic, electronic, electric, transport, thermoelectric, and optical properties and has not been widely used in device design. The puckered lattice structure, which is the source of the noticeable anisotropy in BP, becomes even more striking with decreased dimensionality. Previous research has demonstrated that bulk BP exhibits a straight band gap and excellent carrier mobility [1-2]. Additionally, it has been demonstrated that under high pressures, BP undergoes a number of phase transitions and turns superconductive [12]. In keeping with predictions, the band gap of BP will rise with fewer layers, from 0.3 eV in bulk to 2 eV for a single layer. [10-12]. In contrast to MoS2, the band gap in BP stays direct for any number of layers. [10]. Furthermore, unlike few-layer MoS2, which typically displays n-type behavior, BP can be modulated into both p-type and n-type structures thanks to its rather small band gap. [13]. The phosphorus atoms in BP create a covalent bond with three nearby atoms, however unlike graphene, BP takes the form of a puckered structure with ridges that are not in the plane. [16-17]. Weak van der Waals forces keep the phosphorus atoms in their individual layers together[2,4]. Fig. 1. shows a schematic diagram of lateral JLFET. Since each element in BP is connected to three nearby atoms, the fact that phosphorus has only three valence electrons, as in contrast to carbon, makes it semiconducting. [18-19].

II. METHODOLOGY

The Atomistix ToolKit 2020 package implements the density functional theory (DFT) and nonequilibrium green function (NEGF) formalisms for the calculation of transport properties [14]. We consider a double-gated monolayer -BP JLFET as shown in Fig. 1. The effective oxide thickness (EOT) of the dielectric material of 0.5-nm is assumed for simulations. The FET is p-type doped with doping density considered for testing are 1.66×10^{13} , 2.20×10^{13}, 2.76×10^{13} and 3.32×10^{13} cm^{-2} and is taken as uniform throughout the entire device regions. Since BP exhibits high anisotropic carrier mobility with crystal orientation, we only use the armchair direction (AC) as the transport direction (as it has an eight-orders-of-magnitude higher current than the zigzag (ZZ) direction does for ML BP). [20-22], to achieve optimum performance. The device's ballistic quantum transport properties are estimated using the NEGF formalism. The Schrodinger equation and the Poisson equation are self-consistently solved inside the NEGF formalism to take into consideration the bias and gate potentials throughout the device channel [23-24]. Using the Landauer-Buttiker formula, the drain current I_{ds}, at a given drain-bias voltage, V_{ds}, and gate voltage, V_{gs}, is determined as follows:

$$I_{ds}(V_{ds},V_{gs}) = \frac{2e}{\hbar}\int_{-\infty}^{\infty}[f_s(E-\mu_s) - f_d(E-\mu_d)]T(E,V_{ds},V_{gs})dE \quad (1)$$

where $T(E,V_{ds},V_{gs})$ being the transmission coefficient, f_s and f_d are the source and drain Fermi-Dirac distribution functions, respectively, while μ_s and μ_d are the electrochemical potentials for the source and drain, respectively.

Noting that the transmission coefficient $T(E)$ is the average of k-dependent transmission coefficients over the Brillouin zone, in NEGF approach, we may express the k -dependent transmission coefficients $T_{k_z}(E)$ at energy E as

$$T_{k_z}(E) = Tr\left[\Gamma^L_{k_z}(E)G_{k_z}(E)\Gamma^R_{k_z}(E)G^{\dagger}_{k_z}(E)\right] \quad (2)$$

in which $G_{k_z}(E)$ and $G^{\dagger}_{k_z}(E)$ are the retarded and advanced Green's function, respectively, and $\Gamma^{L/R}_{k_z}(E)$ = $i\left(\sum_{L/R} - \sum^{\dagger}_{L/R}\right)$ accounts for the left and right electrodes level spreading out in the form of self-energy $\sum_{L/R}$. The Hartwigsen-Goedecker-Hutter (HGH) type pseudo potentials with Tier 2 the basis set is used. The real-space mesh cutoff is taken as 100 Hartrees, and the temperature is set to 300 K. The k-point grids in the form of Monkhorst-Pack are set to $16\times1\times1$and $16\times1\times216$ for the central region and the electrode region, respectively [23]. The boundary conditions adopted in our analysis along the transverse, vertical, and transport directions is of periodic, Neumann, and Dirichlet type, respectively [25].

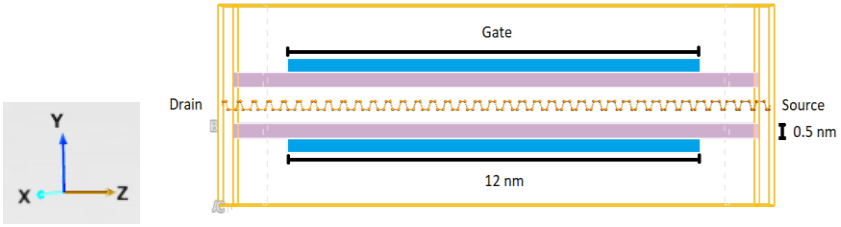


Fig. 1. The schematic diagram of lateral JLFET

The primitive cells of the ML BP are orthorhombic and hexagonal. Optimized phosphorene lattice is used to form the supercell required for our device construction. We used the generalized gradient approximation (GGA) in the form of the Perdew-Burke-Ernzerhof (PBE) functional to modify the exchange and correlation interaction. The Monkhorst-Pack of $16\times1\times1$ grid points is adopted for monolayer BP modeling. Ballistic transport properties are calculated by coupling DFT with NEGF methods. The k-point meshes for the electrodes regions and central region are sampled with $16\times1\times216$ and Tier 2 the basis set is used. The density mesh cut-off energy is set to 100 Hartee and the electron temperature is set at 300K [24].

We used the gate length (L_g) to 12 nm which is selected in accordance with the current guidelines set by the International Roadmap for Devices and Systems (IRDS 2021) for 2028 applicable for HP and HD applications, and the device performances are studied at a for varying the source-drain voltages from 30 mV to 70 mV, and the gate-to-source voltage window (V_{gs}, voltage window between the OFF and ON-states) is also taken as -0.75V to 2V for p channel JLFET The work functions are same for both the gates [25-26].

III. Results And Discussions

The optimized lattice parameters for monolayer black phosphorus (ML- BP) taken for our simulations are a = 4.62 Å and b = 3.35 Å which is in conformity with [2-5]. In Fig. 2. we have plotted the drain current (I_d) as a function of gate bias voltage (V_{gs}) for various doping concentrations ($(1.66-3.32)\times10^{13}$ cm^{-2} with a fixed drain to source voltage (V_{ds}), of 0.05 Volt. for test and the corresponding doping levels are provided in the inset. From the plot it is evident that increasing doping concentration the subthreshold slope deteriorates while the ON-state saturation current increases. However, for suitable JLFET operation high doping concentration is often desired. To meet these conflicting requirements simultaneously, the optimal doping concentrations of 2.20×10^{13} cm^{-2} for HP and 1.66×10^{13} cm^{-2} for HD applications are found from test results which meet the requirement for IRDS

2021. In Fig. 4. we have plotted the drain current (I_d) as a function of gate bias voltage (V_{gs}) taking the optimal doping concentrations to show the impact of oxide dielectric constant on drain current and control of channel electrostatics. It is clear from the plot that increasing dielectric constant, the slope of drain characteristics increases depicting improved electrostatic control by the gate. The subthreshold slope changes from 65 to 61 $mV/decs$ as relative dielectric constant is varied from 4 (SiO_2) to 25 (HfO_2) [27-30]. The drain electrode bias, however, has negligible impact on drain current as may be verified from plot in Fig. 5. Only a small ON current increase is achieved as drain bias is increased from 30mV to 70mV with similar doping. The key parameters of the device performances are tabulated in TABLE-I.

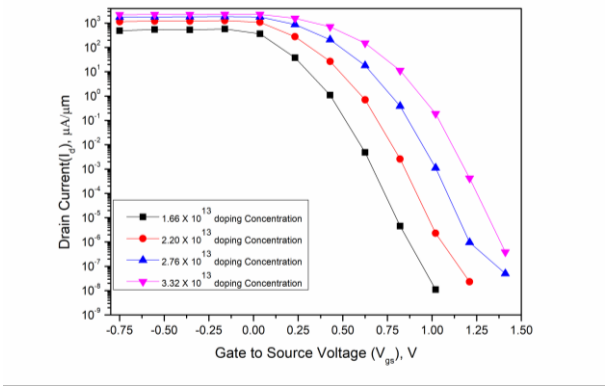


Fig. 2. Comparative drain current plot for different doping levels as a function of gate-to-source voltages ranging between $(1.66-3.32)\times10^{13}$ cm^{-2} with a drain to source voltage (V_{ds})= 0.05Volt

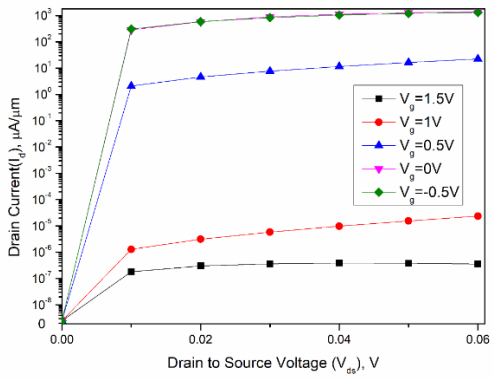


Fig. 3. Comparative drain current plot as a function of drain-to-source voltages (V_{ds}) for various doping concentrations ranging between $(1.66-3.32)\times10^{13}$ cm^{-2} with a variation of gate to source voltage (V_{gs})

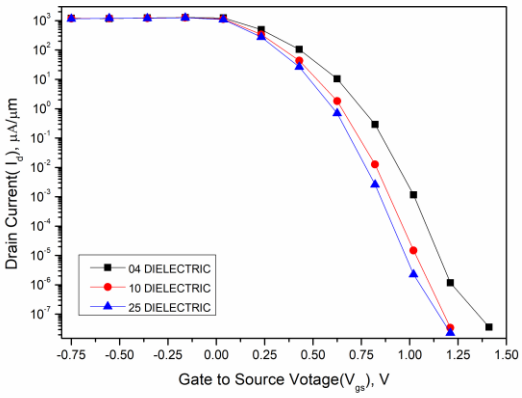


Fig. 4. Comparative drain current plot as a function of gate-to-source voltages (V_{gs}) for different dielectric materials as insulator under the gate electrodes.

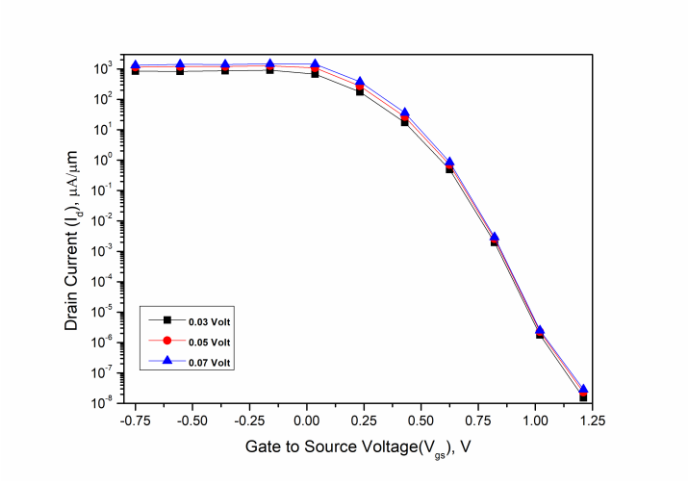


Fig. 5. Comparative drain current plot as a function of gate-to-source voltages (V_{gs}) for three different drain-to-source bias (V_{ds}).

1. Gate capacitance and Electrostatic Control

For The JLFET operation, the uniformly doped channel behaves as simple resistor when no bias is applied and also flat band (FB) condition prevails if work functions of the metal and the semiconducting materials are same. Thus, applying small drain bias will cause maximum current to flow from source to drain since the channel thickness is at maximum under these conditions. Applying appropriate gate bias will deplete the charge carriers underneath the gate regions forming barrier for the transporting carriers from source to drain. The channel thickness will be reduced causing decrease in current. As the gate voltage is further increased the depletion regions extends more towards the centre of the channel and further decrease of current and eventually the device enters into off-state. The change of depletion layer will in turn develop voltage control capacitance in the channel.

For evaluating the key device characteristics at the gate length of 12nm, we can safely assume that the device operates in the ballistic under partial depletion regimes, $C_g = C_{ins}C_d / (C_{ins} + C_d)$ where C_d is the depletion capacitances and C_{ins} is the gate insulating or oxide capacitances, respectively [30-32]. In order to determine the total charges Q_g in the channel of the device, Mulliken charge-based approach is adopted in our analysis. The extracted channel charges under the channel as a function of gate-to-source voltages for various doping concentrations are shown in the plot in Fig. 5. The impact of doping concentrations on the induced charges is clearly evident from Fig. 6., which also explains the transport mechanism of the device. Beyond saturation voltages ($V_{gs} \geq -0.016V$), doping variation has negligible effect on depleted charge variation and is significantly high in mid subthreshold regions in conformity with the results obtained from the current curves in Fig. 2. Besides the charge variation is again low near OFF-state regions. The gate capacitance is then computed by using the expression $C_g = dQ_g / dV_{gs}$ [32-33], in which V_{gs} is gate-to-source biased applied and is provided in Fig. 6. It is clear from our analysis that any stray and parasitic capacitances are also automatically captured. Gate bias dependence of the capacitance plot in Fig. 7. is provided for p-type channel only, for n-type channel the dependence will be similar with small difference in numerical values. Moreover, the influence of drain bias on capacitance in these cases is small for both type devices, as the applied drain voltage required for JLFET operation is also small, unlike conventional MOSFET, depicting superior characteristics of JLFET.

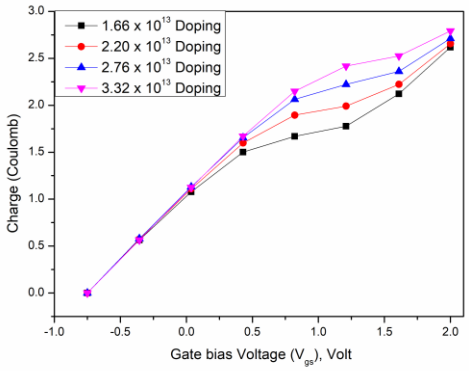


Fig. 6. Extracted charge variations under the channel as a function of gate-to-source voltages for different doping concentrations.

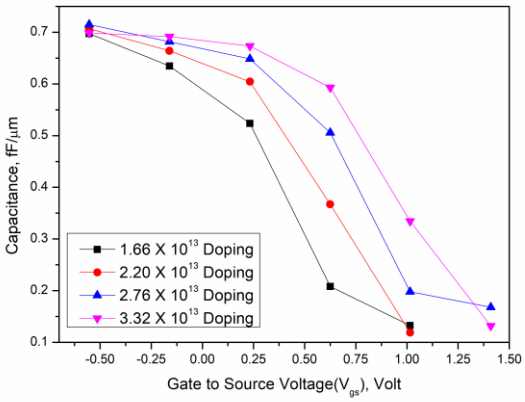
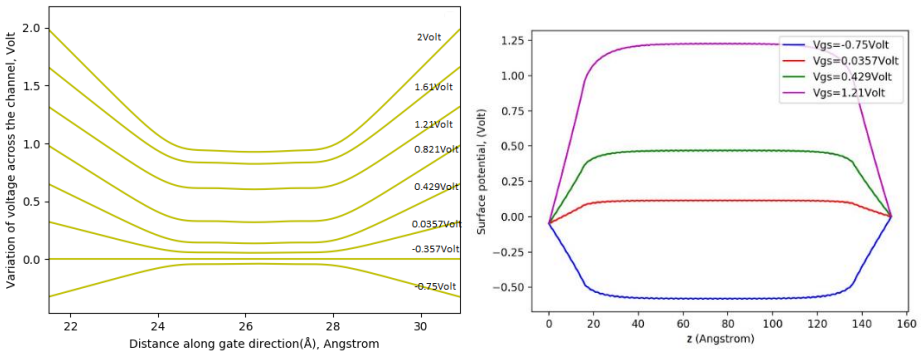


Fig. 7. Variations in capacitance for different doping concentrations in DG JLFET devices as a function of gate-to-source voltages.

In order to comprehend the impact of gate bias voltage on surface potential of the device, we plot the average electrostatic potential along the y-direction (i.e., along the gate direction) for various gate bias voltages for the p-type device in Fig. 8(a)., for the optimal doping concentration 2.20×10^{13} cm^{-2} (for HP applications from Fig. 2). The surface potential along the z-direction (i.e., along the transport direction) for various gate bias are plotted in Fig. 8(b). It is observed that as the positive gate bias is increased, the depletion layer thickness underneath the metal gate and oxide layer increases and hence the effective height of the barriers opposing the source-drain conduction, and finally leading the device to the OFF-state. It is noteworthy that the central potential (i.e., the potential at the middle of two phosphorus atoms) also shifts upward along with the depletion layer potentials upon increase of gate bias, leading to lowered leakage current in this absolutely thin device geometry. To gain more insight, corresponding carrier densities under the gates are also plotted in Fig. 9 for HP FETs, as a function of y-directions. As expected, the carrier densities decrease with increasing V_{gs} for p-type FETs, and impact is more between the BP layer and oxide surfaces, due to capacitive influence of the oxides.



(a) (b)

Fig. 8. (a) Variation of voltage (v-y) along gate direction (y) direction for different applied gate biases (b) Variation of electrostatic potentials for 2.20×10^{13} cm^{-2} p-type doping as a function of gate-to-source voltages along the channel direction (z) in DG JLFET device.

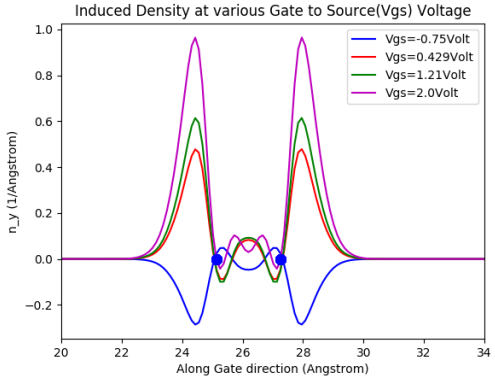


Fig. 9. Variation of depletion charge density (n_y) for 2.20×10^{13} cm^{-2} p-type doping as a function of gate-to-source voltages along gate direction (y) in DG JLFET device.

2. On-Off Characteristics and subthreshold swing

Low enough OFF-state leakage is usually desired in FET applications, which in turn, forces the standby power dissipation (P_{stanby}) to remain small in the integrated circuits. If not suitably designed, under thermal influence this may lead to thermal runway and eventually destroys the entire circuits. Leakage currents are observed to be drastically reduced when the relatively low (or optimized) doping level is provided throughout the device while keeping the saturation current at its maximum. It is noted from Fig. 2., for p-type BP-JLFET at the doping concentration of 1.66×10^{13} cm^{-2} the OFF-state leakage is $1.10\times10^{-8}\,\mu A/\mu m$, at approximately 1.02V of V_{gs}. Similarly for doping value 2.20×10^{13} cm^{-2} for the p-type BP-JLFET the OFF-state leakage is $2.31\times10^{-8}\,\mu A/\mu m$ at V_{gs} value of 1.21V as noted in Fig. 2. With similar $V_{ds}=0.05V$, and found that both of which is much smaller than the IRDS-21 requirements for HD and HP applications for 2028[15], respectively. We set the OFF-state current value for HP applications $I_{off}(HP)$ as 10 $nA/\mu m$ and OFF-state current value for HD applications $I_{off}(HD)$ as $0.1nA/\mu m$ and evaluate the corresponding OFF-state source-to-gate voltages $V_{gs,off}(HP/HD)$ as per the benchmark specified in IRDS 2021. Then the ON-state current $I_{on}(HP/HD)$ is then determined at $V_{gs,on}(HP/HD)=V_{gs,off}(HP/HD)+V'_{dd}$ [36], respectively where V'_{dd} is set to be 0.65 V as per IRDS 2021[15].

Higher possible ON-state current is usually sought at saturation since it determines the ability to provide adequate drive currents required in the circuits. Further higher ON current provides higher switching speed of the device. As noted in Fig. 2. that for BP-JLFET in the range of doping concentrations $(1.66-3.32)\times10^{13}$ cm^{-2} the ON-current obtained here is $576-2300\mu A/\mu m$ (in Fig. 2.) except for 1.66×10^{13} cm^{-2} for which the ON-current is $576\mu A/\mu m$ and all are greater than the IRDS 2021 requirements for high performance (HP) technologies. It is also noted that for the p-type doping concentrations 1.66×10^{13} cm^{-2} ON-state performance is also satisfied for HD application benchmark requirements. Further, the JLFET performance not significantly affected by the variations in V_{ds} in the ranges $0.03-0.07V$.

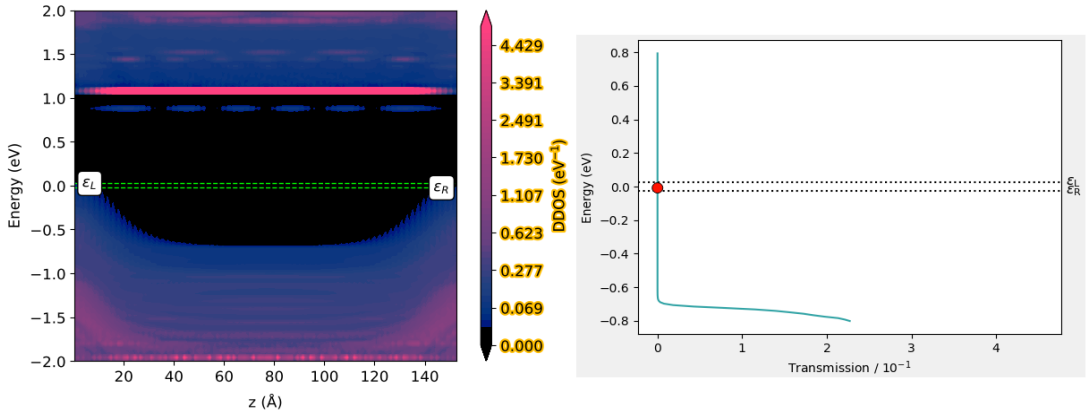
Turning next to the $I_{ON}-I_{OFF}$ ratio, another important static figure of merit, we predict the value of the ratios to be in the range of 10^{8-9} for the selective doping concentrations for HD while 10^{5-6} for HP devices, which are higher than previous results reported in [8] for BP MOSFET. We assume $I_{OFF}=100\,pA/\mu m$ as prescribed in IRDS2021 benchmark for HD technologies and $I_{OFF}=10nA/\mu m$ for HP technologies [15].

The sub-threshold swing (SS), defined as $SS=\partial V_{gs}/\partial\log I_d$ [25], is a very important indicator to illustrate the gate electrostatics control ability in the subthreshold region. In order to lower the energy consumption of a transistor, it is advantageous to have a smaller SS, which denotes improved gate control and may lower the operating switching voltage.. The SS value of the phosphorus JLFET with $L_g=12nm$ is in the ranges 61-65

mV/dec for doping of ($(1.66-3.32)\times10^{13}$ cm^{-2}. Compared with the optimal simulated SS of 82 mV/dec in 12nm-gate-length DGML(double gate monolayer) MOSFETs [7]; thus the SS of phosphorus device are much lower. This indicates the superior gate-controllability of DGML JLFET devices than the DG ML MOSFET in the subthreshold region as the SS of the JLFET device can be tuned near to the optimum value of 60 mV/dec [7].

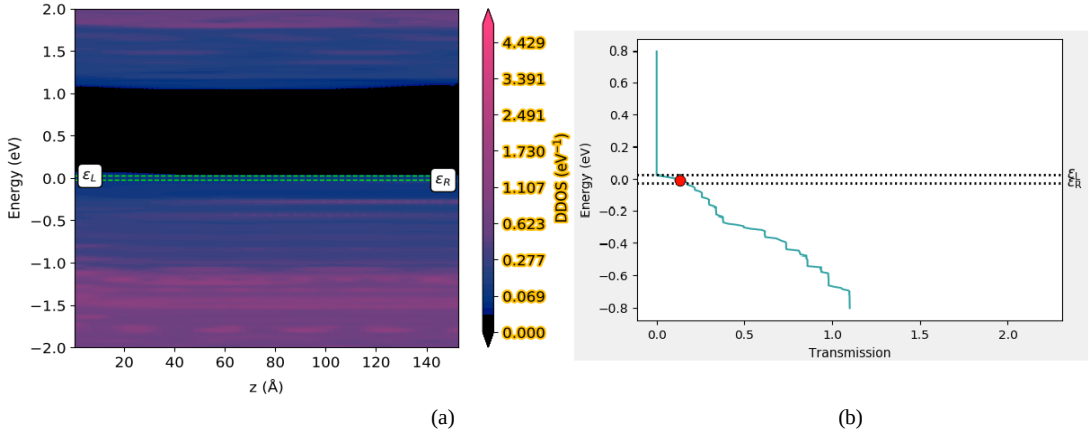
Transconductance g_m, given by $\partial I_d / \partial V_g$, is another indicator to characterize the gate control ability at the superthreshold region, as shown in Figure. 2. It is noted that the g_m values for 1.66×10^{13} cm^{-2} is 1670 $\mu S / \mu m$ and that for doping value 3.32×10^{13} cm^{-2} it is 4400 $\mu S / \mu m$.However, for doping concentration 2.76×10^{13} cm^{-2} the g_m value is maximum (4660 $\mu S / \mu m$). Hence on current is expected to be maximum in these doping ranges. Furthermore, the g_m values are considerably higher comparing to the black phosphorus DG MOSFET, leading to higher on current characteristics of the BP JLFET. The impact of doping variation on peak trans-conductance is elucidated in the plot in Fig. 12.

The operation mechanism of the JLFET device under examination here can be well understood by evaluating the local density of states. (LDOS) as shown in Fig. 10 and 11 for the OFF-state and ON-state, respectively, for p-type FETs. Additionally, corresponding transmission spectrums are offered. From Fig. 10 We observe that in the OFF-state, the effective barrier height is roughly 0.6 eV, resulting in an entire block of transmission. The device enters the ON-state by lowering the gate bias, which also lowers the barrier height to zero as shown in Fig. 11, allowing for high carrier transfer from the source to the drain electrode. The channel below the metal gate gets depleted as the gate bias increases with positive polarity, increasing barrier height. The device eventually enters the OFF-state when the gate region is completely depleted and the current transmission from source to drain terminal ends. At this bias situation, 1.21V, the effective barrier height reaches its maximum value. Similar argument may be made for n-type FETs operation.



(a) (b)

Fig. 10. Projected local density state (PLDOS) along source to drain and the corresponding transmission spectra of OFF-state for the DG-JLFET with gate length L_g =12nm. The green/black dash line indicates the source to drain tunneling window $V_{ds} = 0.05V$ corresponding to right and left Fermi levels of the electrodes.



(a) (b)

Fig. 11. Projected local density state (PLDOS) along source to drain and the corresponding transmission spectra of on-state for the DG-JLFET with gate length L_g =12nm. The green/black dash line indicates the source to drain tunneling window $V_{ds} = 0.05V$ corresponding to right and left Fermi levels of the electrodes.

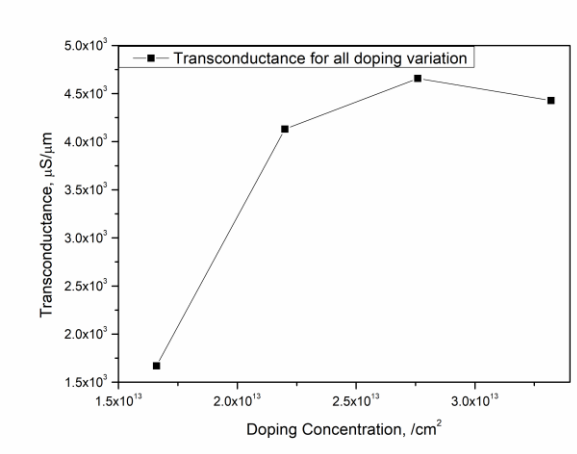


Fig. 12. Variation of transconductance as a function of different doping concentrations.

3. Intrinsic Delay time

The definition of intrinsic delay time (τ) is the duration of the response of the drain current to the applied gate voltage. This is defined as $\tau = C_g V_{ds} / I_{ON}$ .However, due to strong bias dependence of gate-capacitance C_g, we quantify as $\tau = (Q_{ON} - Q_{OFF}) / WI_{ON}$ [35] , where, Q_{ON} and Q_{OFF} are both the depleted charges in the gate regions for the on-state and off-state, respectively, W is the channel width and I_{on} is the drain current in the on-state [25]. A small τ indicates a faster switching speed of a digital circuit. The small value of gate capacitance C_g together with the high I_{on} would develop small τ. It should be noted that I_{on} can be increased by increasing the device gate length as referred in previous studies [25]. For JLFET, however, one can have additional degrees of freedom, as seen in Figs. 2 and 3. When doping concentration is increased, the ON-current substantially increases along with a slight increase in the OFF-current. The doping concentration enhances the ON-current in JLFET due to the more conducting charge carriers present in the ON-states. Additionally, the greater doping concentrations suggest a quicker reaction to gate bias for channel region depletion as depicted from subthreshold characteristics for various doping concentrations which has been clearly understood from the Fig. 2. This is also reflected in gate capacitance behavior at different gate bias conditions. The total gate capacitance of the phosphorus JLFET is in the range of $0.1325 \sim 0.6972 / 0.119 \sim 0.7067 / 0.1678 \sim 0.714 / 0.13176 \sim 0.698\, fF/\mu m$, for $(1.66 / 2.2 / 2,76 / 3.32) \times 10^{13}$ cm^{-2} which is in the range of the IRDS goals for both HP(0.37fF/μm) and HD(0.37fF/μm) requirements indicating a good gate control feature. The delay time of the device with a well-defined I_{on} (I_{off} of this device can reach IRDS standard for HP or HD in 2028) can be evaluated. The calculated (τ) of the 12 nm DG ML phosphorus JLFET are given in Fig. 13. With this small Cg, all of the intrinsic delay time (0.12 to 0.42 ps) for HP application and (0.076 to 0.423 ps) for HD application for $(1.66 - 3.32) \times 10^{13}$ cm^{-2} p-type doping is much lower than the IRDS HP/HD standards (0.78 ps) [36-37]. Most of the delay times are two times to six times lower than the IRDS HP standards, so the DG ML phosphorus JLFET offers excellent fast-switching device characteristics at the 12nm channel length. With the construction of 12 nm channel length and doping concentration of 3.32×10^{13} cm^{-2}, the delay time of the device is 0.12 ps whereas for low power application the delay time of the device reaches 0.076 ps which is ten times lower than the IRDS HD standards[38]. It is also observed that as the doping is decreased, the delay time monotonically increases. The delay time that can meet or almost near the ITRS HD goals are shown in Fig. 13.

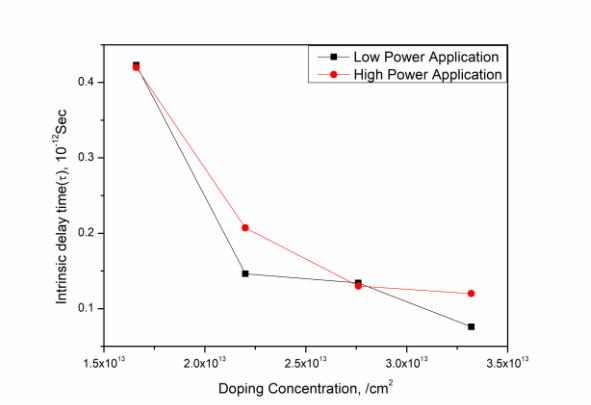


Fig. 13. Calculated Intrinsic delay time (τ) plot as a function of different doping concentrations in DG JLFET device for HP and HD applications. Red dashed lines represent the delay time for HP application and black dashed line for HD application.

4. Power Delay Product (PDP)

The power delay product (PDP) is a measure of a transistor's switching energy required for transitions from OFF-state to ON-state, which, in addition to speed, is a crucial measure in large-scale integration. The power delay product (PDP) is computed as $PDP = V_{ds} I_{ON} \tau = (Q_{ON} - Q_{OFF}).V_{ds} / W$ [25], were Q_{ON} and Q_{OFF} are as defined before. From the figure the PDPs decrease with the decreasing doping concentration for HP applications however, for HD application it does not have any obvious effect. For both cases, however, the PDPs of DG ML phosphorus JLFET are hundreds of magnitudes smaller than the IRDS HP/HD 2028 requirement of 0.24/0.28 fJ/μm. The optimal value we have got 12×10^{-3} fJ/μm for 2.76×10^{13} cm^{-2} for HP application and 2.2×10^{-3} fJ/μm for 1.66×10^{13} cm^{-2} for HD application[39-41]. Encouragingly, with the optimal I_{on} that can fulfil the IRDS HD standards in 2028, the transistors with the configuration of 12-nm-gate-length in conjunction with selection of proper doping have at least one order of magnitude less cost of switching energy and twenty times faster switching speed compared with the IRDS HP 2028 target.

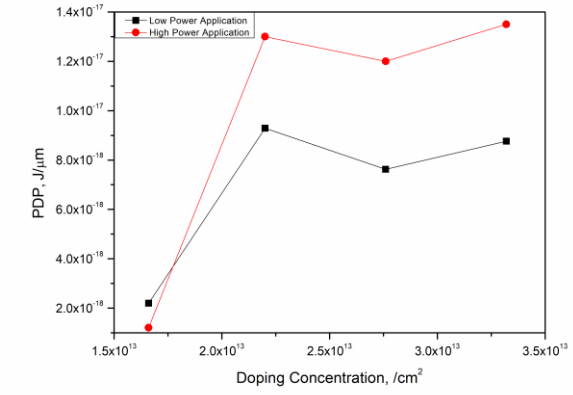


Fig. 14. Calculated Power delay product (PDP) plot as a function of different doping concentrations in DG JLFET device for HP and HD application. Red dashed lines represent the delay time for HP application and black dashed line for HD application.

5. Discussion

From previous work it was shown that ML phosphorene shows better transport characteristics in the arm chair direction compared to zigzag direction. We considered DG ML phosphorene JLFETs taking arm chair and zigzag direction as source to drain transport direction for verifying their relative merits in JLFET application. It is found that I_{on} of arm chair JLFET is higher than the corresponding zigzag JLFET for the same doping concentrations. The SS values are all lower for arm chair JLFET. Furthermore, the time delay for HP applications are lower predicting faster switching speed for arm chair JLFET in comparison with zigzag JLFET.

For JLFET operation the heavily doped p-type ML phosphorene channel is depleted by applying appropriate gate voltages. From figure 7 a and b, it is noted that applying small negative gate voltage push the channel of the device into accumulation region. To deplete it small positive gate bias is needed. As the positive gate voltage is

increased further more charges will be depleted but as noted in Fig. 7a, weak inversion may take place near the semiconductor-oxide interface. These minority charges will not participate in the conduction due to reverse source-drain biasing. Therefore, the term “depletion” used here is in broader sense [22]. However, high level doping ensures that the device will not go strong inversion regime, for operational range.

High doping apparently may increase majority carrier concentration which in turn increase saturation current but eventually limited by the increased carrier scattering owing to higher concentration. Hence an optimum concentration is obtained for suitable characteristics of the device. The optimum performance metrics are shown in TABLE II for easy reference.

TABLE. I

PERFORMANCE METRICS OF ML-BP DG-JLFETS AND THE IRDS 2021 REQUIREMENT FOR THE 2028[41].

Doping	L_g (nm)	V_{dd} (Volt)	SS (mv/Dec)	I_{on} (μA/μm)	I_{on}/I_{off}	C_g (fF/μm)	τ (ps) HP	τ (ps) HD	PDP (fJ/μm) HP	PDP (fJ/μm) HD
1.66×10^{13}	12	0.05	61	576	1.27×10^{8}	0.1325	0.42	0.42	12.12	2.2
2.20×10^{13}	12	0.05	62	1270	4.5×10^{8}	0.119	0.21	0.15	13	9.28
2.76×10^{13}	12	0.05	63	1860	1.94×10^{9}	0.1678	0.13	0.13	12	12.47
3.32×10^{13}	12	0.05	65	2300	5.95×10^{9}	0.1318	0.12	0.08	13.5	8.76

TABLE. II

PERFORMANCE METRICS OF ML-BP DG-JLFETS AND THE IRDS 2021 REQUIREMENT FOR THE 2028[41]

.

		L_g (nm)	V_{ds} (Volt)	SS (mv/Dec)	I_{ON} (μA/μm)	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)
For HP application	MOSFET(IRDS)	12	0.65	75	924	0.37	0.78	0.47
	JLFET (This Work)	12	0.05	62	1270	0.12	0.20	0.012
For HD application	MOSFET(IRDS)	12	0.65	68	521	0.37	0.78	0.47
	JLFET (This Work)	12	0.05	61	576	0.13	0.15	0.0098

IV. CONCLUTION

In summary, the key device performance metrics of the double-gated BP with a 12-nm gate length for p-channel JLFET configurations are evaluated performing a fully quantum transport simulations. The electrostatic control mechanism of the gate is also illustrated. Furthermore, the improved device characteristic for p channel DG JLFET reveals that the device may be promising in post CMOS technological era. The gate controlling parameters are also accessed, and their effects on the intrinsic switching speed of the FET and power dissipation are examined. Finally, the device's likelihood of being viable according to the IRDS21 roadmap for 2028 device structure is compared, and it is discovered that the BP-JLFET may be an excellent contender for HP and HD technologies in advanced nanoscale MOSFET.

References

[1] Liu, H. et al. Phosphorene: An Unexplored 2D Semiconductor with a High Hole Mobility. ACS Nano 8, 4033–4041 (2014).

[2] Max C. Lemme , Deji Akinwande , Cedric Huyghebaert &Christoph Stampfer, ‘2D materials for future heterogeneous electronics’,nature comm 2022

[3] Lee, Tae; Kim, Soo; Jang, Ho (2016). Black Phosphorus: Critical Review and Potential for Water Splitting Photocatalyst. Nanomaterials, 6(11), 194–.199

[4] Koenig, Steven P.; Doganov, Rostislav A.; Schmidt, Hennrik; Castro Neto, A. H.; Özyilmaz, Barbaros , Electric field effect in ultrathin black phosphorus. Applied Physics Letters, 104(10), 103106–103112,2014.

[5] Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS2 Transistors. Nat. Nanotechnol. 6(3), 147–150 (2011)

[6] F. W. Chen, H. Ilatikhameneh, T. A. Ameen, G. Klimeck, and R. Rahman, “Thickness engineered tunnel field-effect transistors based on phosphorene,” IEEE Electron Device Letters 38, 130–133 (2017).

[7] Haratipour, N., Robbins, M. C. & Koester, S. J. Black phosphorus p-MOSFETs with high transconductance and nearly ideal subthreshold slope. Condensed Matter-Mesoscale and Nanoscale Phys. 1 (arXiv:1409.8395) 2014.

[8] Y. Takao and A. Morita, Physica BþC 105, 93 (1981).

[9] R. Keyes, Phys. Rev. 92, 580 (1953).

[10] Y. Du, C. Ouyang, S. Shi, and M. Lei, J. Appl. Phys. 107, 093718 (2010).

[11] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nat. Nanotechnol. 6, 147 (2011)

[12] Talukdar, Angshumala; Raibaruah, Apurba Kumar; Deva Sarma, Kaushik Chandra (2020). Dependence of Electrical Characteristics of Junctionless FET on Body Material. Procedia Computer Science, 171, 1046–1053, 2020.

[13] Dae-Young Jeon, Jimin Park, So Jeong Park, and Gyu-Tae Kim,"Junctionless Electric-Double-Layer MoS2 Field-Effect Transistor with a Sub-5 nm Thick Electrostatically Highly Doped Channel," ACS Applied Materials & Interfaces 2023 15 (6), 8298-8304.

[14] Atomistix ToolKit version 2020.09, QuantumWise A/S (www.quantumwise.com): Copenhagen, Denmark

[15] International roadmap for Devices and Systems, IRDS 2021, https://irds.ieee.org/

[16] Duarte, J.P.; Moon-Seok Kim; Sung-Jin Choi; Yang-Kyu Choi "A Compact Model of Quantum Electron Density at the Subthreshold Region for Double-Gate Junctionless Transistors" , 59(4), 1008–1012, 2012.

[17] Chandra Deva Sarma, Kaushik; Sharma, Santanu "An approach for complete 2-D analytical potential modelling of fully depleted symmetric double gate junction less transistor" , Journal of Computational Electronics, 14(3), 717–725, 2015.

[18] Jin, Xiaoshi; Liu, Xi; Wu, Meile; Chuai, Rongyan; Lee, Jung-Hee; Lee, Jong-Ho , Modelling of the nanoscale channel length effect on the subthreshold characteristics of junctionless field-effect transistors with a symmetric double-gate structure. Journal of Physics D: Applied Physics, 45(37), 375102–375109, 2012.

[19] Schwierz, F.; Pezoldt, J.; Granzner, R. Two-dimensional materials and their prospects in transistor electronics. Nanoscale , 7, 8261–8283,2015.

[20] Chandra Deva Sarma, Kaushik; Sharma, Santanu, An approach for complete 2-D analytical potential modelling of fully depleted symmetric double gate junction less transistor. Journal of Computational Electronics, 14(3), 717–725,2015.

[21] Lee, Jeongsup; Zhang, Yiqun; Dong, Qing; Lim, Wootaek; Saligane, Mehdi; Kim, Yejoong; Jeong, Seokhyeon; Lim, Jongyup; Yasuda, Makoto; Miyoshi, Satoru; Kawaminami, Masaru; Blaauw, David; Sylvester, Dennis "A Self-Tuning IoT Processor Using Leakage-Ratio Measurement for Energy-Optimal Operation". IEEE Journal of Solid-State Circuits , 1–11 , 2019.

[22] J. Colinge, C. Lee, A. Afzalian, N. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," Nature Nano, vol. 5, no. 3, pp. 225–229, Mar. 2010

[23] S. Gundapaneni, M. Bajaj, R. K. Pandey, K. V. R. Murali, S. Ganguly, and A. Kottantharayil, "Effect of band-to-band tunneling on junctionless transistors," IEEE Trans. Electron Devices, vol. 59, no. 4, pp. 1023–1029, Apr. 2012.

[24] S. Sahay and M. J. Kumar, "Insight into lateral band-to-band-tunneling in nanowire junctionless FETs," IEEE Trans. Electron Devices, vol. 63, no. 10, pp. 4138–4142, Oct. 2016.

[25] Sun, X., Song, Z., Liu, S., Wang, Y., Li, Y., Wang, W., & Lu, J. Sub-5 nm Monolayer Arsenene and Antimonene Transistors. ACS Applied Materials & Interfaces, 10(26), 22363–22371, 2018.

[26] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, "Enhanced electrostatic integrity of short channel junctionless transistor with high-k spacers," IEEE Electron Device Lett., vol. 32, no. 10, pp. 1325–1327, Oct. 2011

[27] Hong Li, Jing Lu,"Sub-10 nm vertical tunneling transistors based on layered black phosphorene homojunction,"Applied Surface Science, Volume 465, Pages 895-901(2019)

[28] Rassekh, Amin; Sallese, Jean-Michel; Jazaeri, Farzan; Fathipour, Morteza; Ionescu, Adrian M. Negative Capacitance Double-Gate Junctionless FETs: A Charge-based Modeling Investigation of Swing, Overdrive and Short Channel Effect. IEEE Journal of the Electron Devices Society, 1–1,2020.

[29] Gnudi, A.; Reggiani, S.; Gnani, E.; Baccarani, G. Analysis of Threshold Voltage Variability Due to Random Dopant Fluctuations in Junctionless FETs. , 33(3), 336–338,2012.

[30] Agrawal, Ashutosh Kumar; Koutilya, P. N. V. R.; Jagadesh Kumar, M. A pseudo 2-D surface potential model of a dual material double gate junctionless field effect transistor. Journal of Computational Electronics, 14(3), 686–693,2015.

[31] S. Sahay and M. J. Kumar, "Symmetric operation in an extended back gate JLFET for scaling to the 5 nm regime considering quantum confinement effects," IEEE Trans. Electron Devices, vol. 64, no. 1, pp. 21–27, Jan. 2017.

[32] L. John, L. C. Castro, and D. L. Pulfrey, "Quantum capacitance in nanoscale device modeling," J. Appl. Phys., vol. 96, no. 9, pp. 5180–5184, Nov. 2004.

[33] S. Luryi, "Quantum capacitance devices," *Appl. Phys. Lett.*, vol. 52, no. 6,pp. 501–503, Feb. 1988.

[34] S. Datta, Quantum Transport: Atom to Transistor. Cambridge, U.K.:Cambridge Univ. Press, 2005.

[35] M. J. Kumar and S. Sahay, ''Controlling BTBT-induced parasitic BJT action in junctionless FETs using a hybrid channel,'' IEEE Trans. Electron Devices, vol. 63, no. 8, pp. 3350–3353, Aug. 2016.

[36] Ameen, T., Ilatikhameneh, H., Klimeck, G. et al. Few-layer Phosphorene: An Ideal 2D Material For Tunnel Transistors. Sci Rep 6, 28515 (2016).

[37] K. Singh, V. Kumar and M. Kumar, "Performance Evaluation of Phosphorene Elevated Source Tunnel FET with Strained Channel and Ferroelectric Gate Oxide," 2019 6th International Conference on Signal Processing and Integrated Networks (SPIN), Noida, India, pp. 371-375, 2019.

[38] Quhe, R., Li, Q., Zhang, Q., Wang, Y., Zhang, H., Li, J.,Lu, J." Simulations of Quantum Transport in Sub-5-nm Monolayer Phosphorene Transistors". Physical Review Applied, 10(2),2018.

[39] S. Sahay and M. J. Kumar, "Nanotube Junctionless FET: Proposal, Design, and Investigation," in IEEE Transactions on Electron Devices, vol. 64, no. 4, pp. 1851-1856, April 2017.

[40] Sahay, Shubham; Kumar, Mamidala Jagadesh. "Symmetric Operation in an Extended Back Gate JLFET for Scaling to the 5-nm Regime Considering Quantum Confinement Effects". IEEE Transactions on Electron Devices, 1–7,2016

[41] Li, H., Tie, J., Li, J. et al. High-performance sub-10-nm monolayer black phosphorene tunneling transistors. Nano Res. 11, 2658–2668 (2018).