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FPGA Implementation of Direct Torque Control for Surface Mounted Permanent Magnet Synchronous Motor using PID Controller

Abstract: - This paper presents a real time FPGA implementation of a Direct Torque Controller for Surface Mounted Permanent magnet Synchronous Motor (SPM) using PID controller. The Direct Torque algorithm with PID controller is designed and implemented using VHDL.The complete digital controller is divided into three modules. From first module position of flux vector is found based on the flux error and torque error and the sector. The torque error is obtained from PID controller. From second module the switching state of the inverter is found based on the position of the flux vector, whereas third module indicates the complete digital controller. The digital controller algorithm presented in this paper has been implemented on a Xilinx Spartan-3 FPGA board. The inverter keeps the same state till the outputs of the hysteresis controllers change states. This inverter is fed to the SPM to maintain a desired constant speed when the load varies. Experimental results on FPGA implementation of a Direct Torque Controller for SPM using PID controller are provided in this paper for two reference speeds and two load torques.

Keywords: Direct Torque Control (DTC), Permanent Magnet Synchronous Motor (PMSM), FPGA, PID controller

I. INTRODUCTION *(HEADING 1)*

The permanent magnet synchronous motor (PMSM) is a synchronous machine wherein the excitation winding is replaced with permanent magnets thus resulting in negligible rotor losses and hence an improved efficiency, outstanding power to weight ratio, offer an improved power factor relatively independent of the pole number and speed.Surface mounted permanent-magnet synchronous motor (SPM) also known as the axial flux permanent magnet motor, the permanent magnets are placed on the surface of a cylindrical iron-laminated rotor body, whereas stator possesses three phase winding [1]. The absence of rotor winding and its related losses, leads to high efficiency, high torque/weight ratio, and reduced cooling requirements [2].

Also due to high equivalent magnetic air gap results in a very low synchronous inductance by which the armature reaction effect on pole flux of SPM is low when compared with other machines of similar size [3] [4].

Due to its high efficiency, high power density and linear torque characteristics made suitable for a wide range of applications like in high performance elevator drive systems, actuators for industrial robots and wheel in motor for hybrid vehicles. The flux-weakening operation with sufficient torque capability of SPM finds applications in wind generators in attaining a wide range of speed control [1]. The control methods of AC drives depend on advanced microprocessor and DSP techniques to implement the complex, real-time control algorithms necessary for high

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dynamic performance of the AC drive. These conventional techniques have disadvantages like complexity in design, more power consumption (input is about 5v to 12v), limited computational capability.

FPGA systems allow easy implementation of digital signal processing due to its higher performances, enhanced flexibility and scalability, the lower cost and computation time attained using FPGA. Many control functions tend to migrate from microcontrollers (or DSP) platforms to SoPCs. The use of FPGAs, instead of other architectures in the field of drives, was mainly based on three factors: the acceleration of the design or parts of it, the flexibility of the reconfigurable hardware (RH), the reduction of costs [5].

The dynamic and fast change in VLSI technology has radically changed the design process. The life cycle of modem electronic products may be even shorter than its design cycle. Therefore, the need for rapid prototyping becomes a design challenge for modem electronic products. The advent of field-programmable gate array (FPGA) technology has enabled rapid prototyping of digital systems [6].

The FPGA realization of the PWM strategies provides advantages such as fast prototyping, simple hardware and software design, higher switching frequency, reuse, restructure and release the computation load of the microprocessor.

In the proposed digital DTC controller with FPGA implementation has the following special features: very fast dynamic response, less failure chances, since this controller works under 1,2v input voltage it has very less power consumption (56 mW), re programmability, low cost, high accuracy (about 99%), high speed. VHDL is a rich and versatile language that can be used for synthesis, modelling, and simulation. VHDL is supported by all major Computer Aided Engineering (CAE) platforms and synthesis tools can compile VHDL designs into a large variety of target technologies [7]. In the early 1980, Altera introduced the first family of PLDs ("Programmable Logic Devices") capable of implementing medium complexity functions [8] Those components were called EPLD, which stands for Erasable PLDs. Those components presented a much higher gate per chip count than their predecessors the PLAs and PALS devices. In 1984 Xilinx developed the first FPGA which broke the barrier of developing register-intensive programmable devices [9]. Those devices evolved to the high performance CPLDs and FFGAs that are now being commercialized in the market [8].

Also, FPGA circuits provide a suitable option for quick calculations [10]. It has the capacity to run activities in massive parallel. FPGA enables real-time control systems to quickly finish several computing tasks [11]. Unlike application-specific integrated chips like digital signal processors, which have fixed hardware functionality, FPGAs are large-scale integrated circuits (FPGAs) whose hardware configuration may be altered through programming [12].

II. FPGA IMPLEMENTATION OF DTC

By using more appropriate vectors during each sampling interval, the system's ripples can be effectively suppressed. Excellent torque and flux linkage control with fewer steady state ripples and faster rapid response performance are displayed by the suitable DTC scheme [13]. Consequently, to run the PMSM drive more effectively and produce fewer ripples in torque and flux response, the discrete voltage vector that is closest to the reference voltage vector is selected [14].

The goal of the proposed control system is to control the torque which in turn controls the speed of a SPM. Fig.1 represents the generalised components of a SPM drive. The function of the digital DTC controller realizes the optimal switching logic to select the appropriate stator voltage vector that will satisfy both the torque status output and the flux status output.

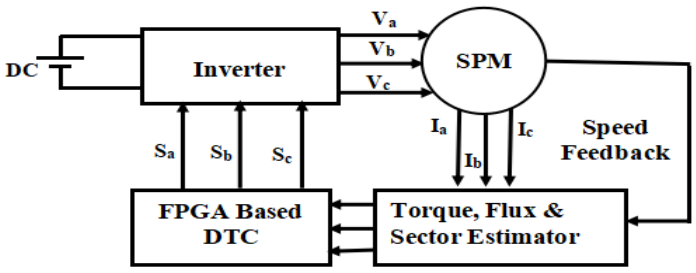

Fig.1. Block diagram of the FPGA implementation of DTC fed SPM

By choosing the right voltage phasors, which are dependent on the torque controller, flux controller, and instantaneous position of λ_s, it is possible to produce the quick torque response. Table 1 provides a general selection of DTC vectors. The look-up table in table 2 is used to calculate the switching state based on S_T, S_λ and S_θ [15]. In this work, flux states are taken as +1 and -1 and torque states are -1,0 and +1 [16].

Digital DTC algorithm using PID controller is realised with Xilinx IST 10.1 simulator and implemented in Xilinx Spartran 3 FPGA board. The flow chart of the digital DTC controller is shown in Fig.2 (Table 1). Where 'K' is the present sector number. In order to overcome the disadvantage of conventional DTC, Modofied DTC is used where the first sector is from -30^0 to $+30^0$, which is represented in Fig 3.

As already mentioned, input to the FPGA board is flux error, torque error and the position of the flux vector (sector number). The flux error represents a two-bit binary number (0 or 1 binary equivalent is 00 or 01). which are given to the pin numbers P39 and P40. The torque error represents a two-bit binary number (0 or 1 or -1 binary equivalent is 00 or 01 or 11). Which are given to the pin numbers P50, P51 and P52. The sector number represents a three-bit binary number (0 to 6)

To obtain results here, this DTC algorithm is divided into three modules. In the first module the voltage vector is obtained for a given torque error, flux error and sector number. In the second module, the switching state of the inverter is found from the voltage vector. Whereas third module is the integration of the first and second modules (from Fig.4 to Fig.6)

Table1. Voltage Vector Selection based on reference flux and torque demand

In the "K" Sector	**Increase**	**Decrease**
Stator Flux	K,K+1,K-1	K+2,K-2,K+3
Torque	K+1,K+2	K-1,K-2

The digital controller algorithm presented here is implemented on a Xilinx Spartan-3 FPGA board, Device: XC3S400, Pin package: PQ208. The Direct Torque algorithm is designed and implemented by using VHDL. Here from Fig. 7, the results are obtained when flux error is 0 and torque error is 1 and the position of the flux vector is in sector 2 (From Table 2) then the switching vector is V3 i.e. the switching states to the inverter are 011. After this switching state inverter switching state changes to V4 → V5 → V0→ V1 → V2 and so on until torque and flux commands are changes from the existing state.

Table 2. Voltage Vector Selection based on reference flux and torque demand

Sector Number θ(N)		**θ(1)**	**θ(2)**	**θ(3)**	**θ(4)**	**θ(5)**	**θ(6)**
S_λ	S_T						
1	1	V_1	V_2	V_3	V_4	V_5	V_0
1	0	V_7	V_6	V_7	V_6	V_7	V_6

1	-1	V_5	V_0	V_1	V_2	V_3	V_4
0	1	V_2	V_3	V_4	V_5	V_0	V_1
0	0	V_6	V_7	V_6	V_7	V_6	V_7
0	-1	V_4	V_5	V_0	V_1	V_2	V_3

From Module I, Module II and Module III position of flux vector is found based on the flux error and torque error w.r.t to the sector number, which are shown in Fig.7, Fig. 8, Fig. 9. Fig.10 and Fig.11. Here the torque error is obtained from PID controller. From Module II, the switching state of the inverter is found based on the position of the flux vector. The final output is taken from Module III, which represents the switching states of the inverter, which are from taken from the pin numbers P44, P46 and P48. From the X power analysis, it is found that the power consumption for the proposed controller is about 56 mW only which is shown in Fig.12.

The Synthesis Report gives the details of the device utilization summary, specifications of the target device, product version etc. From the device utilization summary is tabulated in Table 3 .

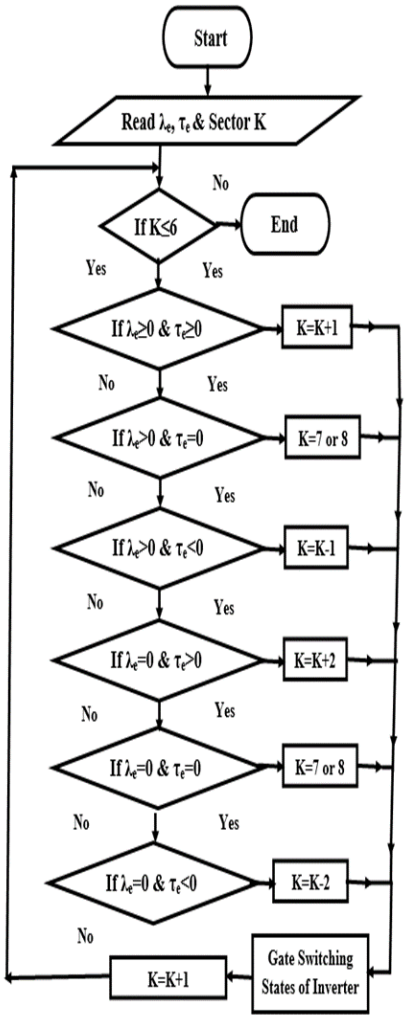

Fig.2. Flow Chart of Digital DTC Controller

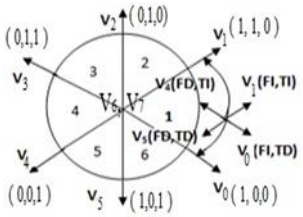

Fig.3. Sector Division

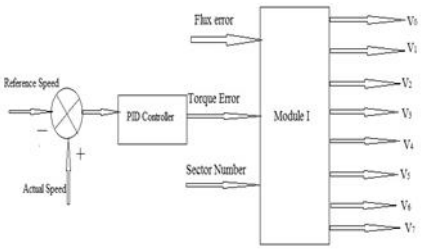

Fig.4. Voltage vector

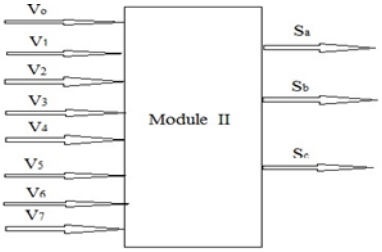

Fig.5.Switching state of the Inverter

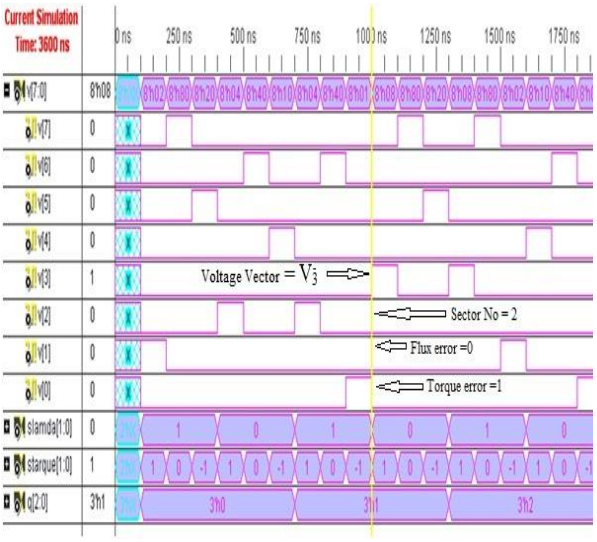

Fig.7. Output Flux vector from sectors 1 to 3 for Module I

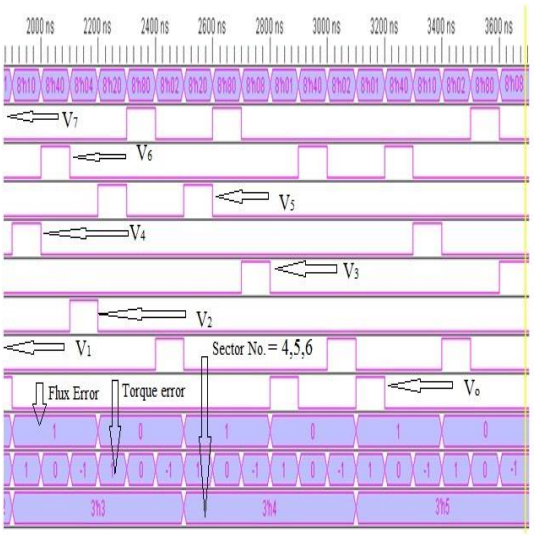

Fig 8. Output Flux vector from sectors 4 to 6 for Module I

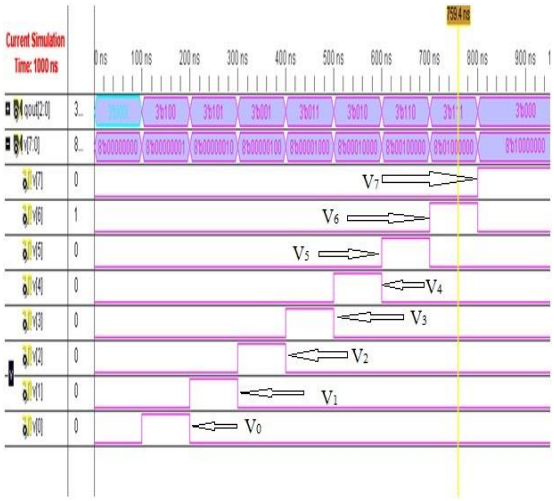

Fig 9. Output Flux vector from sectors 1 to 6 for Module II

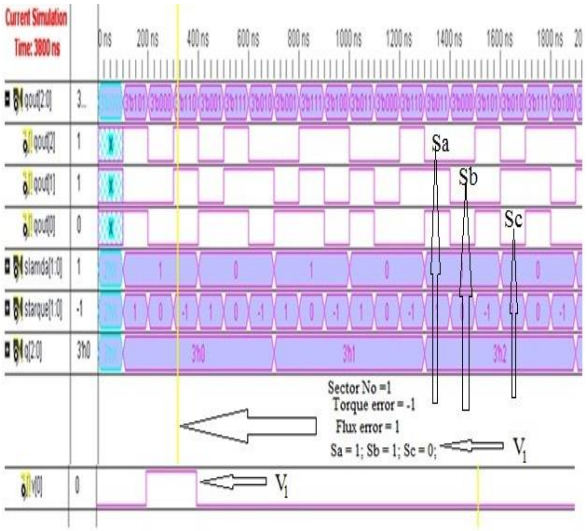

Fig. 10. Output Flux vector from sectors 1 to 3 for Module III

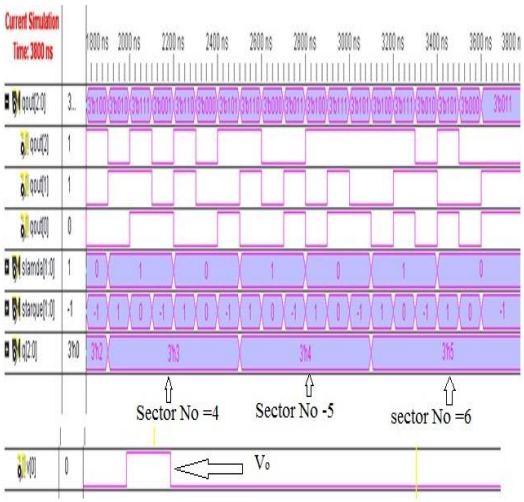

Fig 11. Output Flux vector from sectors 4 to 6 for Module III

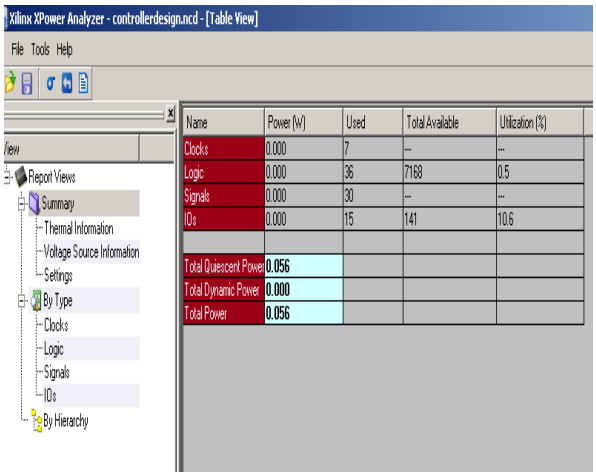

Fig 12. X Power Analysis Report

Table 3. Device utilization Summary

Device Utilization Summary (EstimatedValues)			
Logic Utilization	Used	Available	Utilization
Number of Slices	5415	16640	32%
Number of Slice Flip Flops	3104	33280	9%
Number of 4 input LUIs	8943	33280	26%
Number of IOBs	56	519	10%
Number of GCLKs	3	24	12%
Number of DSP48s	66	84	78%
Xilinx X Power Analysis- Controller Design			
Total Power (in Watts)	0.056		

III. EXPERIMENTAL RESULTS

Fig.13 shows the experimental set up of FPGA implementation of DTC for SPM using PID Controller The motor is fed two level three phase voltage source inverter. This set up consists of FPGA board, intellectual power module (IPM), Surface Permanent Magnet Motor., three phase auto transformer, Personal computer and digital oscilloscopes. In this work, the VSI is implemented by , intellectual power module including gate drivers, six insulated IGBTs and protection circuits, The actual motor phase currents are measured by current sensors (current transformer) which is fed to the control computer through 12 bit bipolar successive approximation ADC with 1µsec speed. First only two motor phase currents are measured, as the motor neutral is isolated, the third phase current can be calculated later, Hence two measure phase currents only two sensors are required. The rotor position is measured by means of 2000 pulses per revolution encoder; Spring balance load is coupled to the shaft of SPM to observe the load torque disturbances. The DTC implementation on Spartan is shown in Fig.14, Here experiment is carried out with two sets of load torques and two sets of reference speeds.

From Fig.15 and Fig.16 it is clear that the direct axis and quadrature axis flux are equal in magnitude (0.9 Wb) with 900 phase shift at TL=1.5 Nm and TL= 2Nm with reference speed of 1000 rpm with corresponding sectors. The electromagnetic torque response, stator flux response and reference speed responses are shown in Fig.17. It is revealed from the Fig.17 that, for an instantaneous change in the set point of the speed, the tracking performance is very fast and accurate.

In this work since the phase currents are sinusoidal (from Fig.18 to Fig.21), the torque ripples are also less which are proven from the THD of phase currents, they are 2.199% when T_L = 1.5 Nm and 3.190% when T_L = 2 Nm. The phase voltage wave forms are shown from Figs 22 to Figs 25. The THD of phase voltage waveforms are 27.997 % and 14.943% when T_L = 1.5 Nm and T_L = 2 Nm respectively. The rms phase voltage and rms phase currents are given in Table 4. Also, it is evident from experimental results that V_α and V_β; $I\alpha$ and I_β are 90° phase difference from each other which are shown in Fig.26 for step changes in the load torque at 1500 rpm. The specifications of SPM used in this work is given in Table 5.

Fig 13.Experimental Setup

Fig 14. Digital DTC implementation on a Xilinx Spartan-3 FPGA board

Fig. 15. Direct and Quadrature axis flux response,Stator flux response and sector numbers for reference speedof 1000 rpm and load torque =1.5 Nm

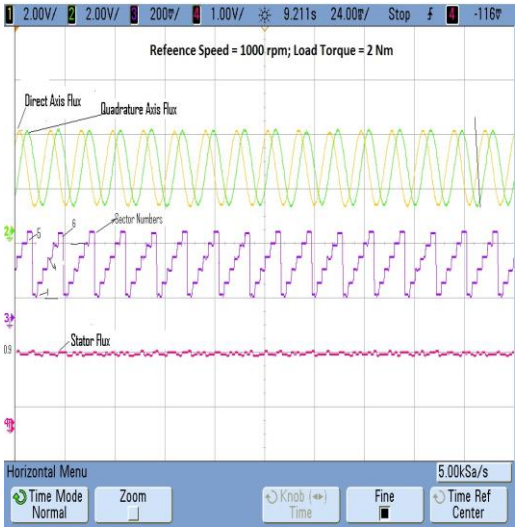

Fig.16. Direct and Quadrature axis flux response,Stator flux response and sector numbers for reference speedof 1000 rpm and load torque = 2 Nm

Fig.17. Speed and electromagnetic torque response for various reference speeds and load torques

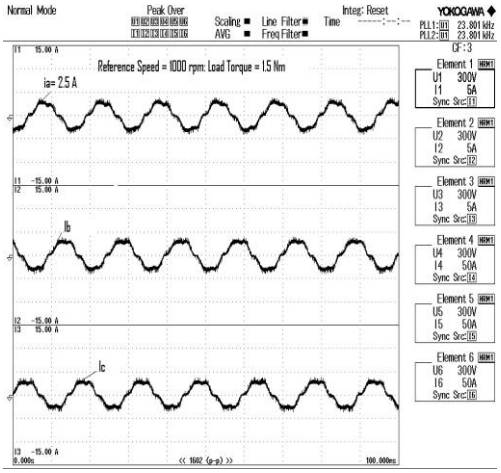

Fig.18. Phase current responses for ω_{ref} = 1000 rpm and T_L = 1.5 Nm

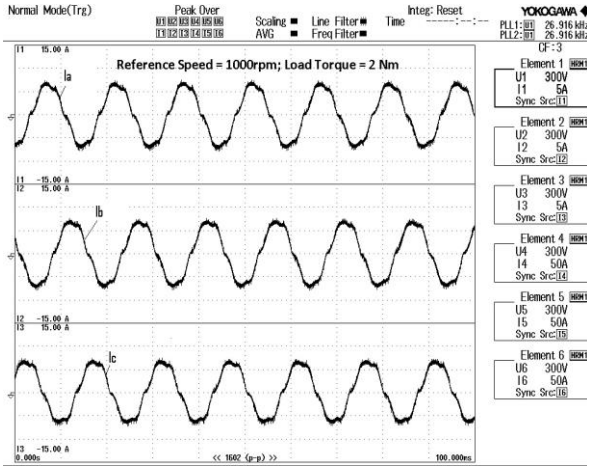

Fig.19. Phase current responses for ω_{ref} = 1000 rpm and T_L = 2 Nm

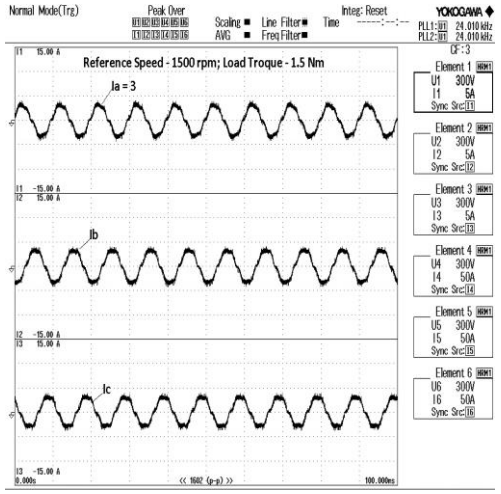

Fig.20. Phase current responses for ω_{ref} = 1500 rpm and T_L = 1.5 Nm

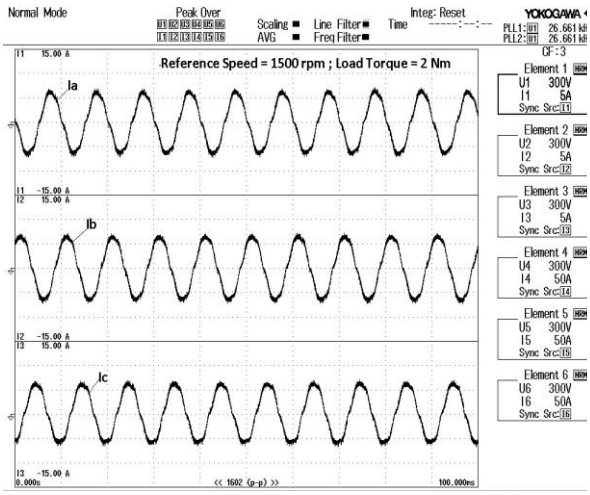

Fig.21. Phase current responses for ω_{ref} = 1500 rpm and T_L = 2 Nm

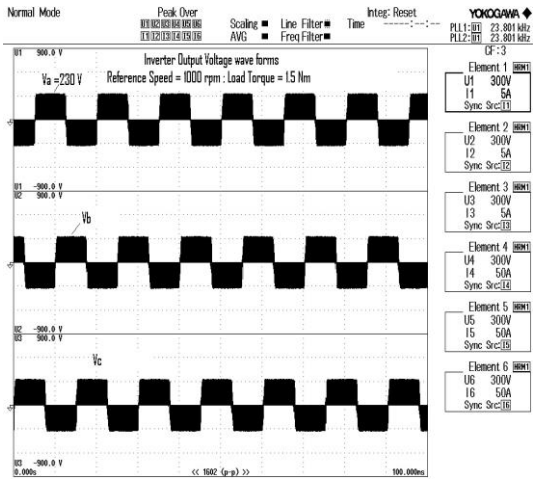

Fig.22. Phase voltage responses for ω_{ref} = 1000 rpm and T_L = 1.5 Nm

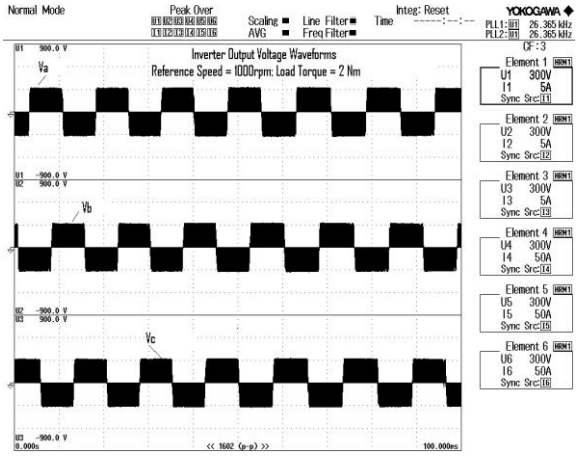

Fig.23. Phase voltage responses for ω_{ref} = 1000 rpm and T_L = 2 Nm

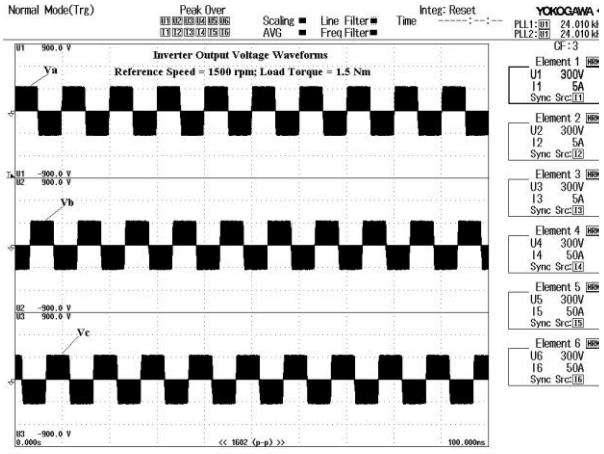

Fig.24. Phase voltage responses for ω_{ref} = 1500 rpm and T_L = 1.5 Nm

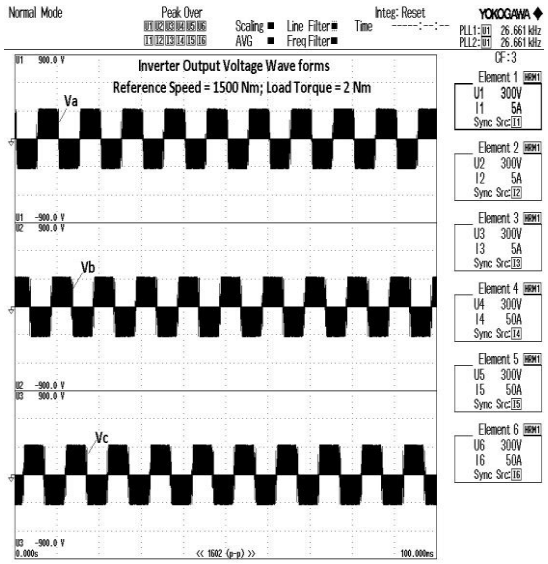

Fig.25.. Phase voltage responses for ω_{ref} = 1500 rpm and T_L = 2Nm

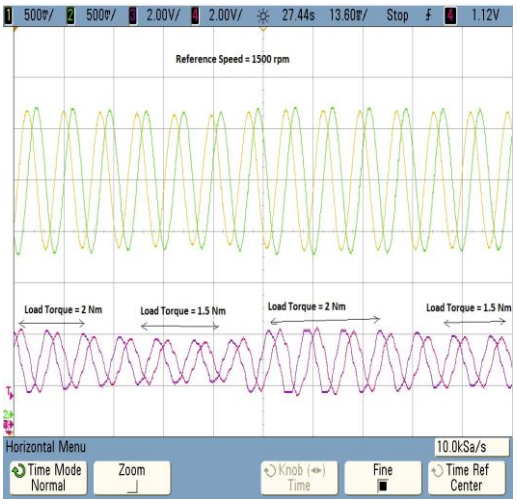

Fig.26. Two Phase current responses and two phase voltage responses for reference speed of 1500rpm and different load torques

Table 4. THD of RMS Phase Voltage and Phase Current

T_L (N.m)	ω_{ref} (rpm)	RMS Phase Voltage (V)	RMS Phase Current (A)	RMS Phase Voltage THD (%)	RMS Phase Current THD (%)
1.5	1000	103.8	2.6817	27.997	7.199
	1500	123.99	2.6210	15.238	3.910
2	1000	110.02	5.1126	22.679	4.744
	1500	130.27	5.1653	14.943	4.609

Table 5. Specifications of SPM

Parameter Description	Value
Rated Output Power	800W
Stall Current	5.5A
Rated Speed	3000rpm
Rated Voltage	230V
Torque Constant	0.526 N.m/A
Voltage Constant	31.8 V/rpm
Phase Resistance	0.85Ω
Phase Inductance	3.82mH
Electrical Time Constant	5.6ms
Mechanical Time Constant	0.65ms
Rotor Inertia	1.16Kg.cm^2

IV. CONCLUSION

In this paper, Hardware implementation of Direct Torque Control using PID controller for SPM with FPGA by VHDL is carried out. The high-performance sensor less AC drives requires a fast digital realization of many mathematical operations concerning control, estimators and algorithms, which are time consuming. The modelling of the algorithm using FPGA need to be done only once so a lot of time is saved. Also control algorithm, when implemented in an FPGA, can have a very short execution time due to the high degree of parallelism of its architecture. The proposed digital controller with simple design approach using FPGA can provide better performance compared with existing controllers. Nowadays FPGAs are available at low – cost and hence a hardware configured controller using FPGA is effective in the reduction of torque and flux ripples. In particular, by virtue of the FPGA's rep-programmability, designers can keep changing and planning devices to cater to user's needs.

Future scope of this work can be carried out to further reduction in torque ripple and flux ripple and THD of voltage and current waveforms by using Fuzzy Logic Controller and Genetic Algorithm. Also by incorporating three level SVM of DTC algorithm with PID Controller, Fuzzy Logic Controller and Genetic Algorithm.

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