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Comparative Analysis of PMOS and NMOS based Linear Regulators with Similar Power Profiles

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Abstract: - In his article, a comparative analysis of PMOS and NMOS based linear voltage regulators is presented. An output power of 18 mW is considered in the both cases. In PMOS based regulator, the output voltage is 1.6 V and output current is 11.25 mA, whereas in NMOS, they are 1 V and 18 mA respectively. Firstly, a conventional linear regulator is designed with PMOS as pass element and its stability and various performance parameters are analyzed. SPICE simulation is carried out to measure parameters and they are tabulated for the comparison. Similarly, another linear regulator is designed where pass element is a NMOS transistor. After the analysis of stability and performance parameters, SPICE simulation is conducted. The performance parameters of both regulators are compared and it is found that NMOS regulator exhibits better performance but low dropout feature of PMOS regulator makes it suitable for low power applications..

Keywords: Linear voltage regulator, LDO, low power, PMIC.

I. INTRODUCTION

Power management integrated circuits deal with efficient and reliable power delivery to a electronic system. Voltage conversion from one domain to another like AC to AC, AC to DC, DC to DC, DC to AC converters form major part of power management system. Typically, DC to DC voltage converters are called voltage regulators. Voltage regulators provide a stable output voltage irrespective of fluctuations in supply and load demands. This control action can be linear or discrete in time domain. Hence, there are two types namely, linear and switching voltage regulators [1]–[4].

Fig. 1 shows basic block diagram of a linear voltage regulator. It is basically a negative feedback system in which current from pass element is adjusted such that output voltage remains constant. Based on type of transistor used in pass element, linear voltage regulators are classified into PMOS and NMOS based regulators.

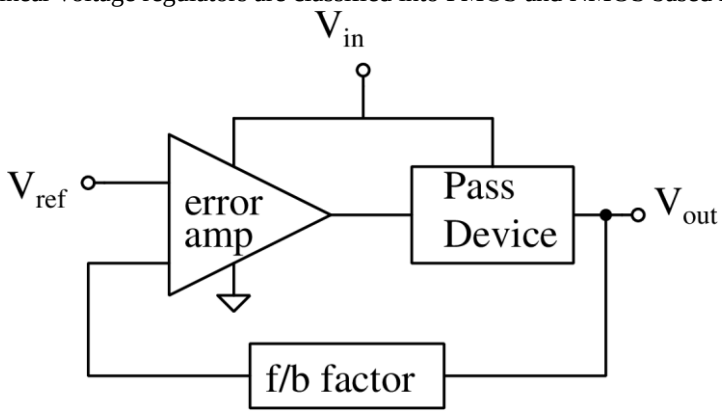

Fig. 1. Basic block diagram of linear voltage regulator

In PMOS based regulator, PMOS transistor is configured as common source amplifier. The voltage difference between input and output terminals is the minimum voltage required to keep MOSFET in saturation region, which is typically around 50 mV to 200 mV [5]–[8]. Hence, PMOS based voltage regulators are called Low Drop Out (LDO) voltage regulators and their power efficiency is comparable with switching regulators [9]–[11]. The dominant pole can be at input of pass transistor or at the output terminal. If it lies at output, LDO requires a large output capacitor, which can be an on-chip or off-chip. On-chip capacitor occupies large area on chip and off-chip does not allow complete system integration on a chip. Hence, recently often dominant pole is chosen at the input of pass transistor. The Miller capacitor is employed to reduce the value of on-chip capacitance. However, the

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transient response of PMOS based regulator is limited by the large parasitic capacitance present at the input of pass transistor and quiescent current of the system [12]–[14].

In NMOS based regulator, pass transistor is a NMOS device and it acts like a common drain amplifier. This makes the difference between input and output voltage larger than the previous type [15], [16]. However, the mobility of charge carrier is higher which significantly reduces the size of pass transistor and its ill [17], [18]effects. Also, due to the nature of common drain configuration, output impedance is less and hence regulation will be better. Typically, the dominant pole lies at the output of error amplifier [19], [20]. In this article, the analysis of both types of regulators are presented and designed for a common power specification. Both regulators are simulated in SPICE tool and performance parameters are compared. Section 2 and 3 give the analysis part of the both regulators. The simulation results and associated discussions are explained the forth section. Last section briefs about conclusion.

II. DESIGN OF PMOS BASED REGULATOR

PMOS based regulator is shown in Fig. 2. 180 nm CMOS technology is considered for the design. Supply voltage is assumed to be 1.8 V. From the literature it is found that the typical dropout voltage is 200 mV. For better common mode range, reference voltage is taken as 0.9 V. The values of feedback resistors are 56.25 kΩ and 43.75 kΩ. To achieve 18 mW output power, maximum load is kept at 11.25 mA for an output voltage of 1.6 V.

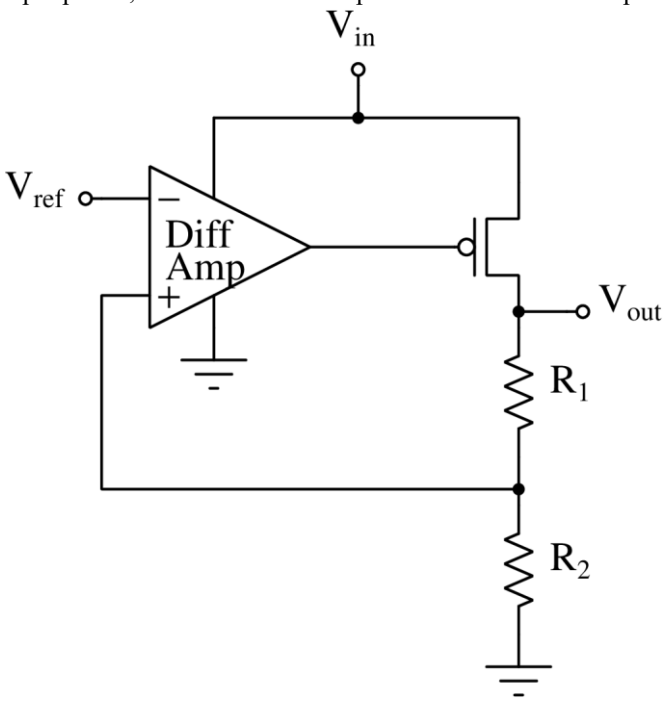

Fig. 2. Basic block diagram of PMOS regulator

The design begins with determining the size of pass transistor. The maximum load capability and dropout voltage decide the W/L ratio of the transistor. The specifications of differential amplifier needs to be derived based on regulator requirements. Table II shows the specifications of the differential amplifier. The complete circuit diagram of the regulator is shown in Fig. 3. The transistors from M_1 to M_6 form differential amplifier and M_p is the pass element. Before looking into the performance parameters, the stability of the regulator must be investigated. The small signal model of the regulator is depicted in Fig. 4.

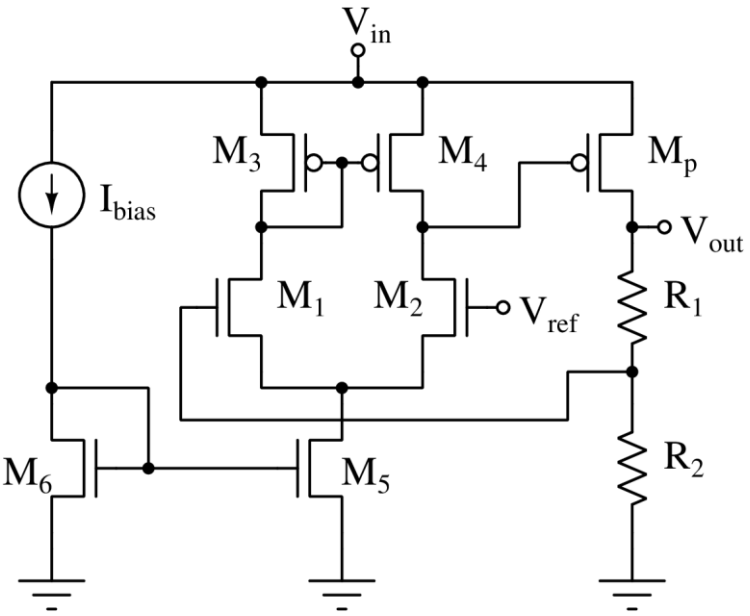

Fig. 3. Circuit diagram of PMOS regulator

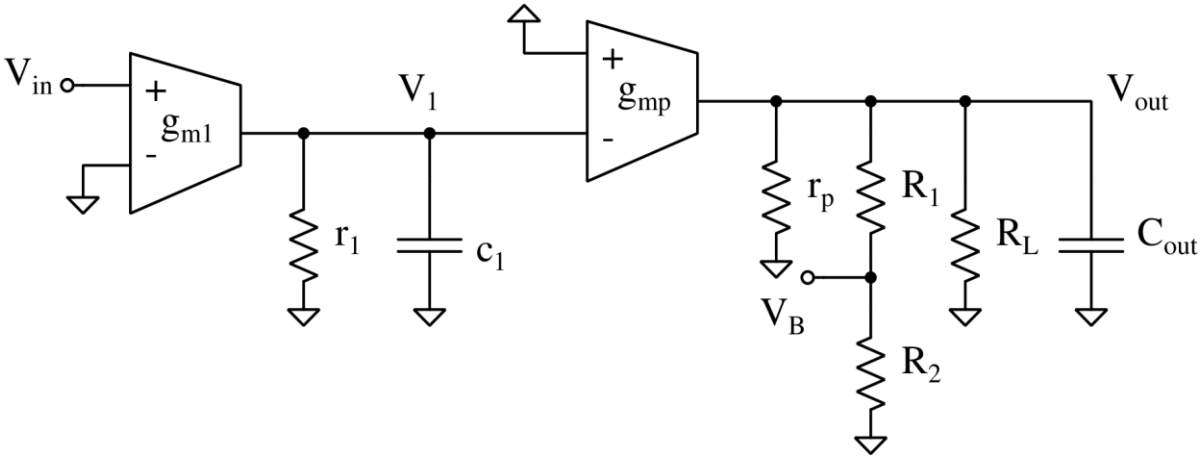

Fig. 4. Small signal diagram of PMOS regulator

Convention of notations are as follows

g_{m1} , g_{mp} → trans-conductance of M_1 and M_p .

c_1 → parasitic capacitance at input of pass transistor.

r_1 , r_p → output resistance of M_1 and M_p .

C_{out} → effective parasitic capacitance at the output terminal.

R_L → output load resistance.

From Fig. 4,

$$V_1 = \frac{g_{m1} r_1}{1 + j\omega c_1 r_1} V_{in}$$

$$V_{out} = \frac{-g_{mp} R_{out}}{1 + \omega C_{out} R_{out}} V_1$$

$$V_{out} = \frac{-g_{mp} R_{out}}{1 + \omega C_{out} R_{out}} X \frac{g_{m1} r_1}{1 + j\omega c_1 r_1} V_{in}$$

$$V_B = \beta V_{out}$$

where $R_{out} = r_p \parallel (R_1 + R_2) \parallel R_L$

$$\frac{V_B}{V_{in}} = -\beta \frac{g_{mp} R_{out}}{1+\omega C_{out} R_{out}} X \frac{g_{m1} r_1}{1+j\omega c_1 r_1} \qquad (1)$$

Table 1

Specifications of Differential Amplifier

Parameter	**Value**
Voltage gain	40 dB
Load capacitance	45 pF
Slew rate	1 V/µs
Input common mode range	0.7 V to 1.1 V
Input common mode range	1 MHz
Phase Margin	90°

From equation (4), it can be seen that the system has two poles, one at the input of pass transistor and other at the output of regulator. To analyze the stability, SPICE simulations are carried out and it is found that that phase margin is only 12°. This is due to the absence of a dominant pole. To make pole at the input of pass transistor as dominant, the output pole must be at a frequency which is square root of 3 times the unity gain bandwidth frequency. This can be achieved by using a Miller capacitor of 15 pF value [10]. Fig. 5 shows the loop gain response of the regulator. It exhibits a phase margin greater than 60° for high and low loads.

Line regulation of PMOS based regulator is given by equation (2). Fig. 6 shows line response of the regulator and measured line regulation is 21.1 mV/V.

$$Lineregulation = \frac{1}{\beta g_{m1} r_1} \quad (2)$$

Equation (3) explains the load regulation of the regulator, where A_v denotes the feed forward gain of the regulator. Load response of the regulator is drawn in Fig. 7 and 311.6 µV/mA is the observed load regulation.

$$Loadregulation = \frac{R_{out}}{1+\beta A_v} \quad (3)$$

To investigate the load transient response, a pulse load as shown in Fig. 8 is applied and obtained result is shown in the same plot. The undershoot and overshoot voltages are 31.2 mV and 35.4 mV respectively. Fig. 9 shows the power supply rejection ratio [PSRR] of the regulator at full load. It exhibits 33.08 dB of PSRR at 10 kHz.

III. DESIGN OF NMOS BASED REGULATOR

In a NMOS based liner regulator, pass device is n channel MOSFET and hence has higher trans-conductance compared to PMOS based regulators. Basically, the final stage is a common drain amplifier and output resistance is low [21], [22]. Fig. 10 shows circuit diagram of NMOS based voltage regulator. Transistors from M_1 to M_5 form error amplifier, M_7 and M_8 constitute a level shifter. Since the output node is having a low resistance, it is not convenient to make it as a dominant pole. This forces the pole at the input of pass transistor to be a dominant one [23]–[25]. Resistor R_3 and capacitor C_c are used for this purpose. Fig. 11 shows the small signal equivalent of NMOS based linear regulator. Notation convention used in stability analysis is as follows

g_{mn} → trans-conductance of nth transistor.
r_{on} → output resistance of nth transistor.
C_n → parasitic capacitance present at node V_n .

$R_1 = r_{o2} \parallel r_{o4}$ $R_2 = (R_3 + r_{o8}) \parallel r_{o7}$ $R_{out} = (R_4 + R_5) \parallel r_{09}$

$$V_1 = \frac{-g_{m2} R_1}{1 + j\omega R_1 C_1} V_{in}$$

$$V_2 = \frac{g_{m7}(1 + j\omega R_2 C_2)}{1 + g_{m7} R_2 + j\omega R_2 C_2} V_1$$

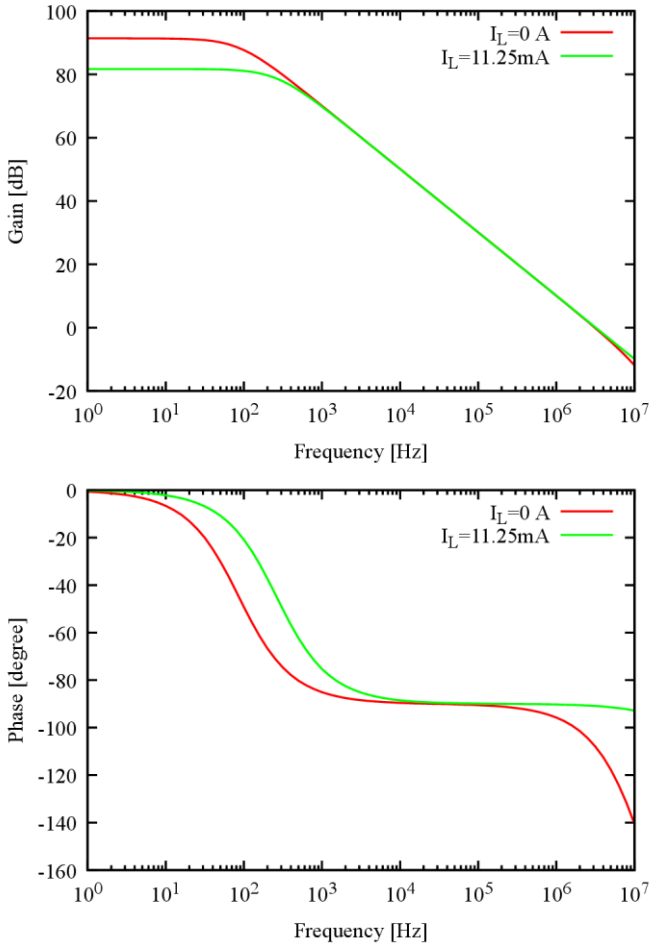

Fig. 5. Open loop frequency response of the regulator

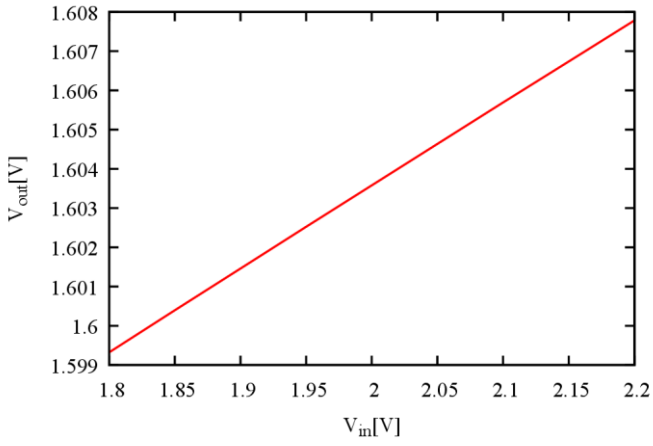

Fig. 6. Line response of the regulator

$$V_{out} = \frac{g_{m9}(1 + j\omega C_{out} R_{out})}{1 + g_{m9} R_{out} + j\omega R_{out} C_{out}} V_2$$

$$V_B = \beta V_{out}$$

$$\frac{V_B}{V_{in}} = \frac{-g_{m2} g_{m7} g_{m9} R_1 (1 + j\omega C_2 R_2)(1 + j\omega C_{out} R_{out})}{(1 + j\omega C_1 R_1)(1 + g_{m7} R_2 + j\omega C_1 R_1)(1 + g_{m9} R_{out} + j\omega R_{out} C_{out})} \quad (4)$$

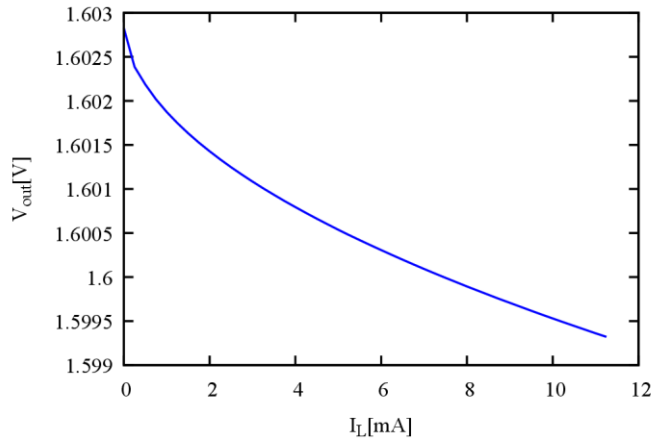

Fig. 7. Load response of the regulator

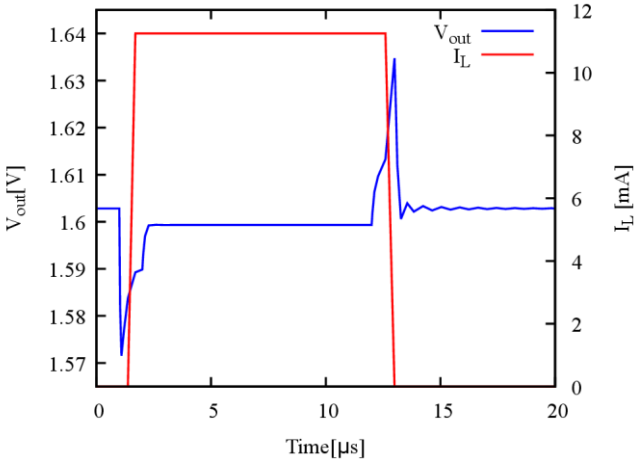

Fig. 8. Load transient response of the regulator

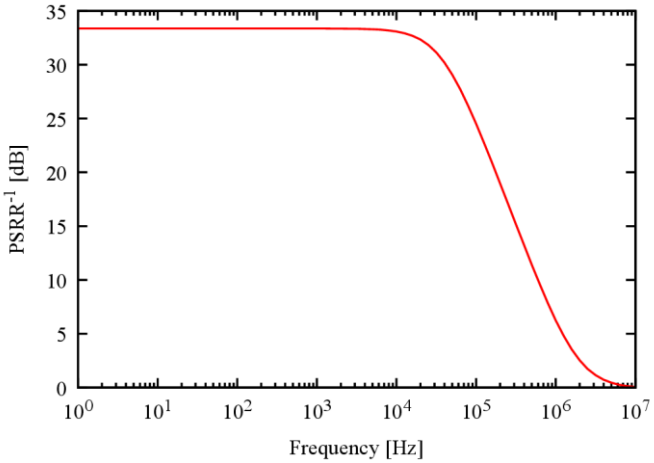

Fig. 9. PSRR of the regulator

Equation (4) indicates that system has three poles and two zeros. However, the pole at the input of pass device is dominant and system is stable with phase margin ≥ 60°. The loop gain response for low and high loads are shown in Fig. 12.

The input voltage is varied from 1.8 V to 2.2 V to determine the line regulation of the regulator as shown in Fig. 13. Line regulation is found to be 0.0022 mV/V. Similarly, load is varied from 0 to 18 mA and response of the regulator is plotted in Fig. 14. The recorded load regulation is 190.5 µV/mA. To investigate the transient response of the regulator, a step load pulse with 1 µs rise and fall time is applied and the response is shown in Fig. 15. The

undershoot and overshoot voltages are 23.3 mV and 15.7 mV respectively. The behavior of the regulator in the presence of ripples in the supply voltage is shown in Fig. 16. At 10 kHz, the PSRR is 63.6 dB.

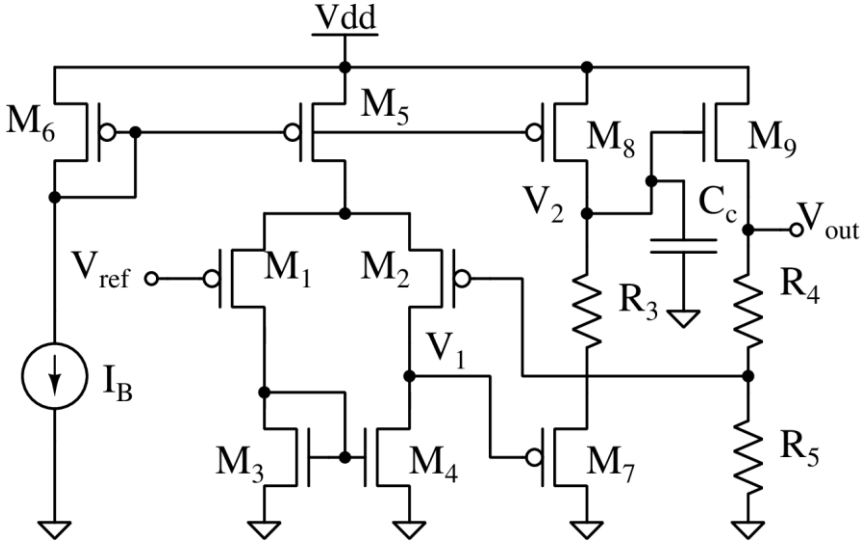

Fig. 10. The circuit diagram of NMOS based regulator

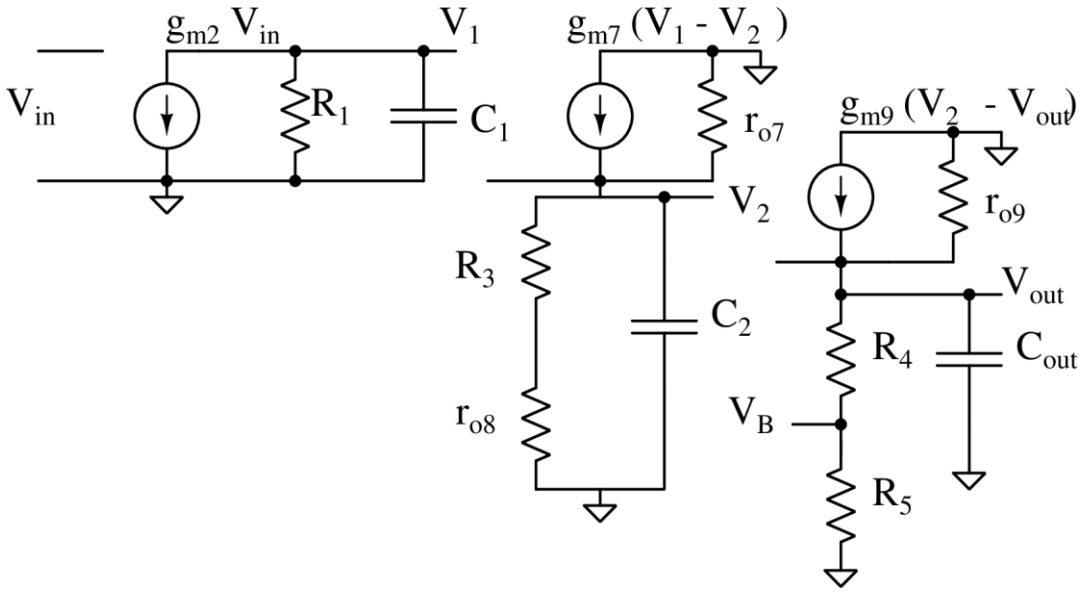

Fig. 11. Small signal equivalent circuit of NMOS based regulator

IV. RESULTS AND DISCUSSION

The simulation results obtained from PMOS based and NMOS based regulators can be compared and many inferences can be drawn. The open loop transfer function of PMOS based regulator, has two poles and one zero and pole at the input of pass transistor is made dominant with the help of Miller capacitor. Whereas in the NMOS based, the transfer function has three poles and two zeros and pole at the input of pass transistor is made dominant with help of level shifter, additional resistor and capacitor [Refer equations (1) and (4)]. Here, forcing the output pole to be a dominant one is complicated since output stage has low output impedance.

The main distinguishing feature is the configuration of pass element. The NMOS based regulator inherently has the highest immune to variations in supply voltage. It can be seen clearly in the line response and PSRR response,the NMOS based regulator is far superior than PMOS based regulator as shown in Fig. 6, Fig. 9 and Fig. 13, Fig. 16. In PMOS based regulator, the pass transistor acts as common gate amplifier for the variations in the supply and this leads to larger variation in output voltage.

Another difference is the size of pass transistor. Since, NMOS has greater drift mobility, the size of the transistor is lesser for the given current specification. Because of this, resulting parasitic gate capacitance of NMOS transistor

is smaller. Hence, NMOS regulator is faster and takes lesser time to respond to the changes in the output voltage than PMOS regulator. This can be observed in Fig. 8 and Fig. 15.

If load regulation of the both regulators are compared, it can be noticed that NMOS regulator performs better than the PMOS regulator. This is due to the difference in output resistances of both regulators. Since, NMOS regulator has lesser output resistance, the change in output voltage for the corresponding change in the load current is minimum.

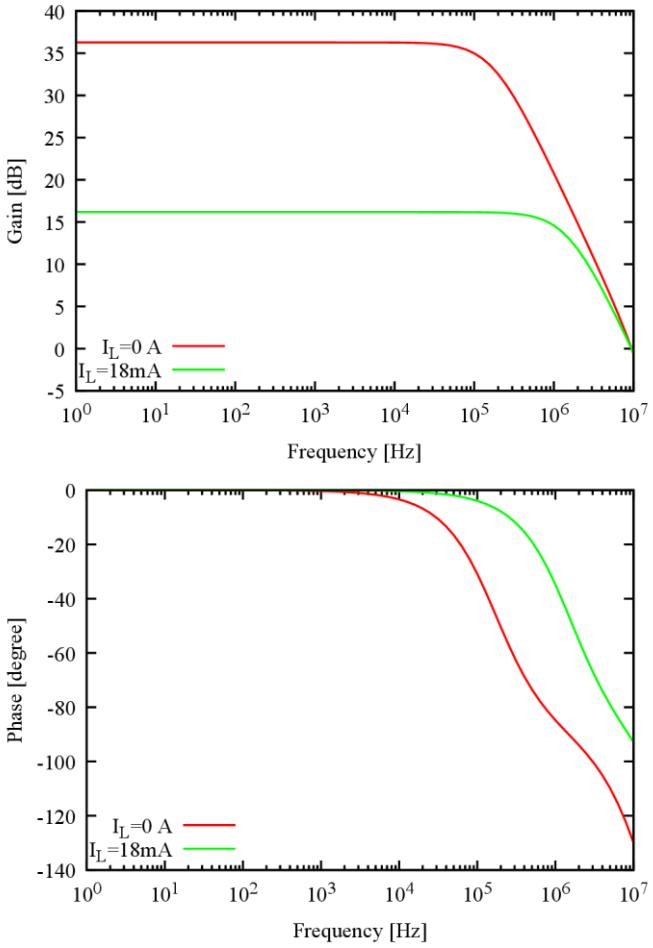

Fig. 12. loop gain response of NMOS based regulator

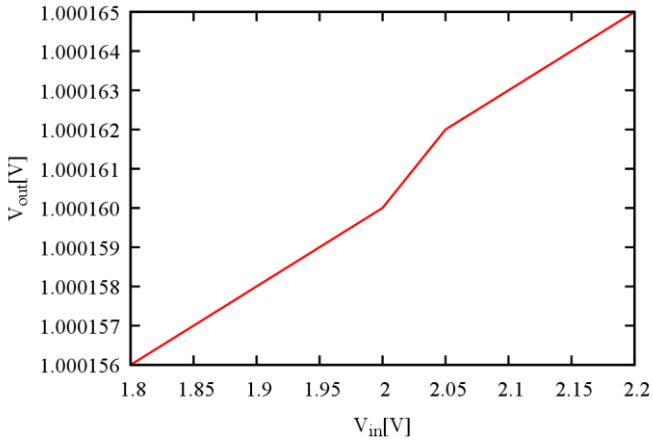

Fig. 13. line response of NMOS based regulator

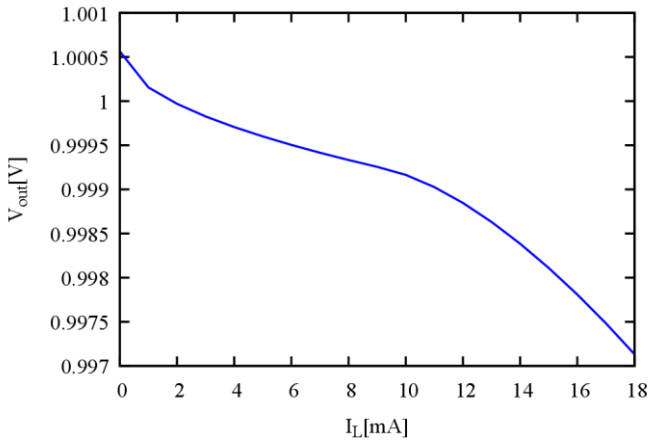

Fig. 14. load response of NMOS based regulator

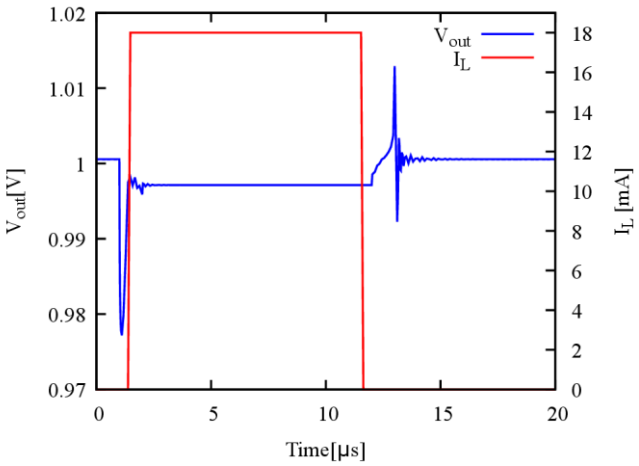

Fig. 15. load transient response of NMOS based regulator

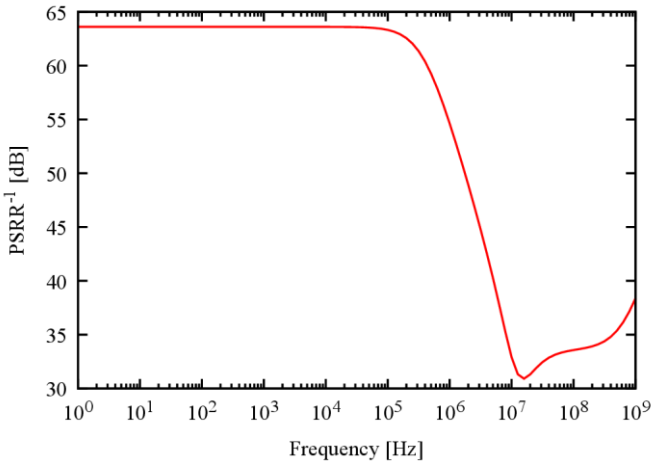

Fig. 16. PSRR response of NMOS based regulator

Open loop gain of PMOS based regulator is more since amplification is obtained from both stages namely error amplifier and pass transistor. Whereas in NMOS regulator, voltage gain is not obtained from pass transistor stage since it is in common drain configuration. Hence, open loop gain is less.

Though NMOS based regulator performs well in many of the parameters, the dropout voltage is more when compared to PMOS regulators. The voltage difference between gate of the pass transistor and output terminal must be higher than the sum of threshold and overdrive voltages. To match the dropout voltage with PMOS based

regulators,it requires a power supply greater than input voltage. Though this could be achieved with help of charge pump,but the resulting chip area and complexity will be more. Hence power efficiency of NMOS regulators is poor and not suitable for low power applications. Table 2 summarizes differences between NMOS and PMOS based regulators.

Table 2
Comparison between NMOS and PMOS regulators

Parameter	**PMOS Regulator**	**NMOS Regulator**
Dropout voltage [mV]	200	800
No. of poles and zeros	2 & 1	3 & 2
Full load loop gain [dB]	81.7	36
No load loop gain [dB]	91	16.1
Line regulation [mV/V]	21.1	0.0022
Load regulation [μV/mA]	311.6	190.5
PSRR at 10 kHz [dB]	33.08	63.6
Undershoot [mV]	31.2	23.3
Overshoot [mV]	35.4	15.7

V. CONCLUSION

In this paper, linear regulators using PMOS and NMOS as pass transistor are analyzed and designed for a common power specification. The stability of both regulator are investigated and performance parameters like line regulation, load regulation, load transient and PSRR response are measured and compared with each other. It is found that NMOS based linear regulators performs well in all above mentioned parameters. However, lower dropout voltage and better power efficiency of PMOS based regulator make it suitable power constraint applications.

REFERENCE

[1] Basso, Christophe P. “Switch-mode power supplies” McGraw-Hill Ed- ucation, 2014.
[2] Chen, Ke-Horng. “Power Management Techniques for Integrated Circuit Design” John Wiley & Sons, 2016.
[3] Rincón-Mora, Gabriel Alfonso.“ Analog IC design with low-dropout regulators (LDOs)”. McGraw-Hill Education, 2009.
[4] Erickson, Robert W., and Dragan Maksimovic. “Fundamentals of power electronics” Springer Science & Business Media, 2007.
[5] N. B. Mustafa, S. Amin, M. B. I. Reaz, F. H. Hashim, and N. Kamal, “Evolution of low drop out voltage regulator in cmos technologies,” Przeglad Elektrotechniczny, vol. 91, no. 12, pp. 26–33, 2015.
[6] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, “Area-efficient linear regulator with ultra-fast load regulation,” IEEE Journal of solid-state circuits, vol. 40, no. 4, pp. 933–940, 2005.
[7] Y. Lu, Y. Wang, Q. Pan, W.-H. Ki, and C. P. Yue, “A fully-integrated low-dropout regulator with full-spectrum power supply rejection,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 3, pp. 707–716, 2015.
[8] S. K. Lau, P. K. Mok, and K. N. Leung, “A low-dropout regulator for soc with q-reduction,” IEEE Journal of Solid-State Circuits, vol. 42, no. 3.
[9] J. Hinojo, C. Luján-Martínez, A. Torralba, and J. Ramírez-Angulo, “Internally compensated ldo regulator based on the cascoded fvf,” Microelectronics Journal, vol. 45, no. 10, pp. 1268–1274, 2014.
[10] A. Maity and A. Patra, “Tradeoffs aware design procedure for an adaptively biased capacitorless low dropout regulator using nested miller compensation,” IEEE Transactions on power electronics, vol. 31, no. 1, pp. 369–380, 2015.
[11] Y. Yosef-Hay, P. L. Muntal, D. Ø. Larsen, and I. H. Jørgensen, “Capacitor-free, low drop-out linear regulator in a 180 nm cmos for hearing aids,” in 2016 IEEE Nordic Circuits and Systems Conference (NORCAS), pp. 1–5, IEEE, 2016.
[12] M. M. Boanloo and M. Yavari, “A low-power high-gain low-dropout regulator for implantable biomedical applications,” Circuits, Systems, and Signal Processing, vol. 40, no. 3, pp. 1041–1060, 2021.
[13] J. Esteves, J. Pereira, J. Paisana, and M. Santos, “Ultra low power capless ldo with dynamic biasing of derivative feedback,” Microelectronics Journal, vol. 44, no. 2, pp. 94–102, 2013.
[14] P. C. Crepaldi, L. H. d. C. Ferreira, T. C. Pimenta, R. L. Moreno, L. B. Zoccal, and E. C. Rodriguez, “Structural design of a cmos voltage regulator for an implanted device,” Current trends and challenges in RFID, 2011.
[15] Mandal, Debashis, et al. “Adaptively biased output cap-less NMOS LDO with 19 ns settling time.” IEEE Transactions on Circuits and Systems II: Express Briefs 66.2 (2018): 167-171.
[16] Li, Kan, et al. “A multi-loop slew-rate-enhanced NMOS LDO handling 1-A-load-current step with fast transient for 5G applications.” IEEE Journal of Solid-State Circuits 55.11 (2020): 3076-3086.

[17] Lu, Yan, Wing-Hung Ki, and C. Patrick Yue."An NMOS-LDO regulated switched-capacitor DC–DC converter with fast-response adaptive-phase digital control." IEEE Transactions on Power Electronics 31.2 (2015): 1294-1303.
[18] Cao, Haixiao, et al. "An Impedance Adapting Compensation Scheme for High Current NMOS LDO Design." IEEE Transactions on Circuits and Systems II: Express Briefs 68.7 (2021): 2287-2291.
[19] Luo, Ping, et al. "A fast-response NMOS-LDO voltage regulator without on-chip compensated capacitor." 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS). IEEE, 2018.
[20] Kilani, Dima, et al. "LDO regulator versus switched inductor DC-DC converter." 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS). IEEE, 2014.
[21] M. H. Kamel, Z. K. Mahmoud, S. W. Elshaeer, R. Mohamed, A. Hassan and A. I. A. Galal, "Comparative Design of NMOS and PMOS Capacitor-less Low Dropout Voltage Regulators (LDOs) Suited for SoC Applications," 2019 36th National Radio Science Conference (NRSC), 2019, pp. 305-314.
[22] Giustolisi, Gianluca, et al. "NMOS low drop-out regulator with dynamic biasing." 2006 13th IEEE International Conference on Electronics, Circuits and Systems. IEEE, 2006.
[23] Desai, Chirag, et al. "A 1.66 mV FOM output cap-less LDO with current-reused dynamic biasing and 20 ns settling time." IEEE Solid-State Circuits Letters 1.2 (2018): 50-53.
[24] Bansal, Nitin, and Rahul Gupta. "An NMOS low drop-out voltage regulator with-17dB wide-band power supply rejection for SerDes in 22FDX." 2018 31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID). IEEE, 2018.
[25] Coulot, Thomas, et al. "Fully integrated power management unit (PMU) using NMOS Low Dropout regulators." Eurocon 2013. IEEE, 2013.