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Regular paper

Design and implementation of an efficient PWM technique for multilevel inverters with power quality monitoring

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Multilevel inverters are one of the important components of modern smart grids and the grid integration of renewable energy sources is not possible without them. In this paper, an asymmetrical switch ladder multilevel inverter (ASLMLI) topology is used to develop a 17-level inverter. The switching pulses for the proposed inverter are developed efficiently using a binary search algorithm based on the grid voltage as a reference. A graphical user interface (GUI) based power quality monitoring system is also developed that senses the grid signals accurately to serve them as a reference for grid integration purposes. The loss and efficiency analysis of the ASLMLI is carried out in the form of generic design equations. A comparative study shows the effectiveness of the proposed system in terms of the accuracy of power quality monitoring. The simulation of the ASLMLI is carried out in MATLAB/Simulink, and the power quality monitoring system is developed using a data acquisition card (DAC) and National Instruments (NI) LABVIEW GUI.

Keywords:Multilevel; Inverter; LabVIEW; Power Quality Monitoring; 17-Level; Smart Grids.

1. Notation

V_{DC}	lowest DC voltage in the circuit
$P_{C,S}$	conduction loss of the switch
$P_{C,D}$	conduction loss of the diode
P_C	average conduction loss
P_O	output power
R_S	switch resistance
R_D	diode resistance
$N_{S,ON}$	number of switches in ON-state at a given time
$N_{D,ON}$	number of diodes in ON-state at a given time
V_{SW}	voltage across the switch
V_D	diode forward voltage
N_L	number of voltage levels
N_S	number of switches
N_D	number of diodes

2. Introduction

Multilevel inverter technology is a very suitable replacement for conventional inverters in high-voltage applications. The output voltage of a power inverter should be a pure sinusoid for grid integration. However, in general, the practical inverters available in the market are either square-wave or modified square-wave inverters with high switching frequencies. The main drawback associated with conventional H-bridge inverters including

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PWM inverters is that they produce a non-sinusoidal output voltage waveform along with electromagnetic interference (EMI) because of high-frequency operation. Therefore, conventional inverters require a large-sized filter to remove the harmonics and generate a sinusoidal output voltage. Multilevel inverters (MLIs) are low-switching frequency inverters that generate a stepped voltage waveform approaching a sinusoidal waveform of the desired frequency. They have many applications ranging from industrial drives to energy harnessing from renewable energy sources [1]. Using small steps of voltage makes the switches of multilevel inverters withstand higher voltages and have reduced voltage ratings. The conventional multilevel inverters existing in the literature are of different types such as diode-clamped, capacitor-clamped, cascaded H-bridge, and some other asymmetrical topologies [2-7].

In the modern multilevel inverters topologies, various switching configurations have been proposed in the literature to generate the maximum possible number of voltage levels at the output. Some topologies are comprised of a basic unitcell (with few switches) being repeated in a certain manner to generate a high number of voltage levels [8-10]. Those topologies can be used to get as many levels as required by just repeating the structure. However, increasing the switches makes the overall size of the inverter very large along with a complex control mechanism. Some other topologies of MLIs have an asymmetrical structure of the switches to generate a specific number of voltage levels [11-14]. There are some switching PWM techniques such as 180 degrees conduction, 120 degrees conduction, sinusoidal PWM, and space vector modulation (SVPWM) available for conventional inverters in the literature. However, the field of generic PWM patterns for multilevel inverters is yet to be explored in detail by researchers.

In [15], a 7-level inverter is presented with nine switches reducing some switches from the conventional cascaded multilevel inverters. A new square T-type MLI configuration is proposed in [12] that utilizes twelve switches and four DC power sources to generate a seventeen-level output voltage. An upgraded configuration of the topology in [12] is presented in [16] as K-type. The K-type topology utilizes fourteen power switches and two DC power sources along with two capacitors generating thirteen output voltage levels. This configuration is superior to its former configuration as the two DC voltage sources are replaced with two capacitors. In all the above-discussed inverter topologies, there is no generic switching pattern for MLIs presented that can be used for grid integration of renewable energy sources through MLIs in a feedback fashion. An MLI topology havingtwelve bidirectional switches is presented in [17] to generate a 6-level output voltage.Owing to a 6-level output voltage, an output filter of a relatively larger size is required for grid integration.

This paper presents the improvements in the topology presented in [18] in terms of the design of an efficient pulse width modulation (PWM) scheme using a binary search algorithm (BSA) along with the power quality monitoring system. The designed PWM scheme for the switches can be used to interface the MLI with the electric power grid using the simplest control. This paper is organized as follows. Section 3 discusses the 17-level ASLMLI topology in detail along with the switching pattern. Section 4 discusses the binary search algorithm for the generation of switching PWM using the grid voltage as a reference. Section 5 discusses the simulation and experimental results including harmonic analysis. Section 6 discusses the general equations for losses and efficiency calculation. Section 7

discusses the power quality monitoring system. Finally, section 8 summarizes the results obtained from the simulation and hardware.

3. Topology of ASLMLI

The schematic diagram of the ASLMLI is shown in Figure.1. The ratio of the DC voltage sources V_1:V_2 is taken as 1:3. The DC power source V_2 is the inverted version of V_1. The switches S_1 and T_1 are bidirectional whereas the switches K_1-K_4, S_x and S_y are unidirectional. The ASLMLI configuration operates as follows:

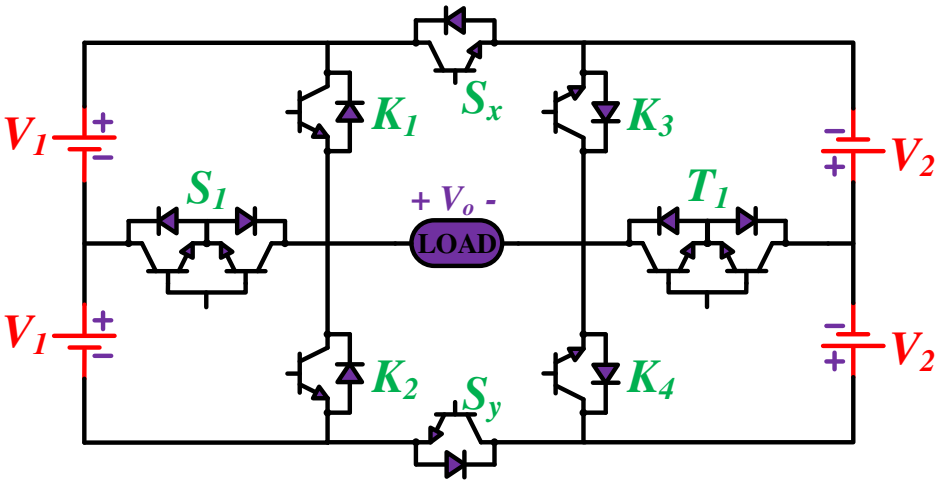

Figure 1: Proposed 17-level ASLMLI configuration

The switches K_1, K_3, and S_x can be turned ON to get the zero level. Alternatively, the switches K_2, K_4, and S_y can also be turned ON to generate the zero level. The path of current for zero voltage level is shown in Figure.2.

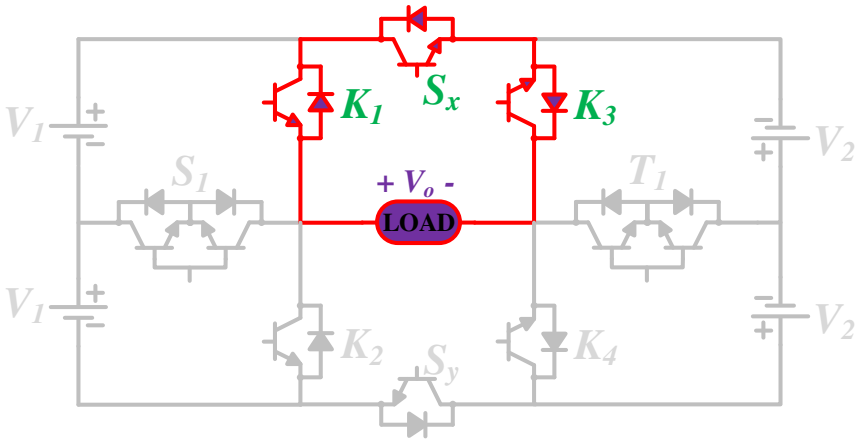

Figure.2: Path of current for state-0 of the ASLMLI

The switches S_1, T_1, and S_x can be turned ON to get the zero level. The path of current for the -(V_1+V_2) voltage level is shown in Figure.3.

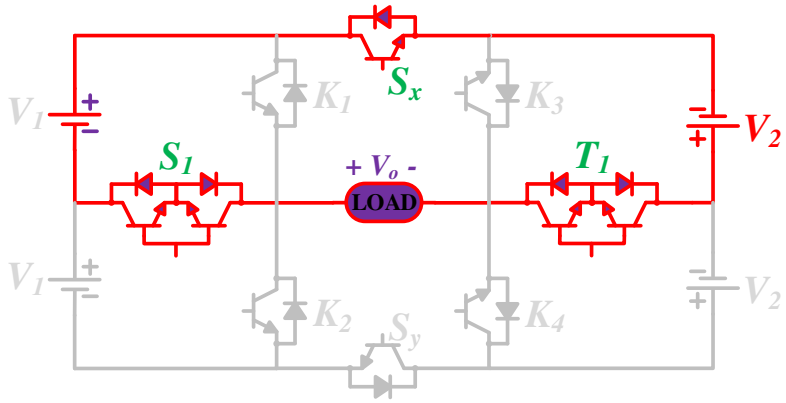

Figure.3: Path of current for the state -(V_1+V_2) of the ASLMLI

Table 1: Switching states of 17-level ASLMLI configuration

Sr. No.	Switching States								V_o
	K_1	K_2	K_3	K_4	S_x	S_y	S_1	T_1	
1	1	0	1	0	0	1	0	0	2(V_1+V_2)
2	0	0	1	0	0	1	0	0	V_1+2V_2
3	0	1	1	0	0	1	0	0	2V_2
4	1	0	0	0	0	1	1	1	2V_1+V_2
5	0	0	0	0	0	1	1	1	V_1+V_2
6	0	1	0	0	0	1	0	1	V_2
7	1	0	0	1	0	1	0	0	2V_1
8	0	0	0	1	0	1	1	0	V_1
9	1	0	1	0	1	0	0	0	0
10	0	0	1	0	1	0	1	0	-V_1
11	0	1	1	0	1	0	0	0	-2V_1
12	1	0	0	0	1	0	0	1	-V_2
13	0	0	0	0	1	0	1	1	-(V_1+V_2)
14	0	1	0	0	1	0	1	1	-(2V_1+V_2)
15	1	0	0	1	1	0	0	0	-2V_2
16	0	0	0	1	1	0	0	0	-(V_1+2V_2)
17	0	1	0	1	1	0	0	0	-2(V_1+V_2)

4. Binary Search Algorithm for PWM

The binary search algorithm (BSA) is used to generate the switching PWM based on the reference voltage signal. The reference voltage signal acts as the grid voltage signal in a practical grid integration system. A look-up table (LUT) is used with the data of Table I as seventeen rows in a sorted fashion from the minimum output voltage (most negative voltage of ASLMLI) to the maximum output voltage (most positive voltage of ASLMLI). The output voltage column acts as the indices of the LUT. At each sampling instant, the BSA compares the amplitude of the reference voltage with the LUT indices and decides the nearest level PWM for the switches. The BSA flow chart is shown in Figure.4.

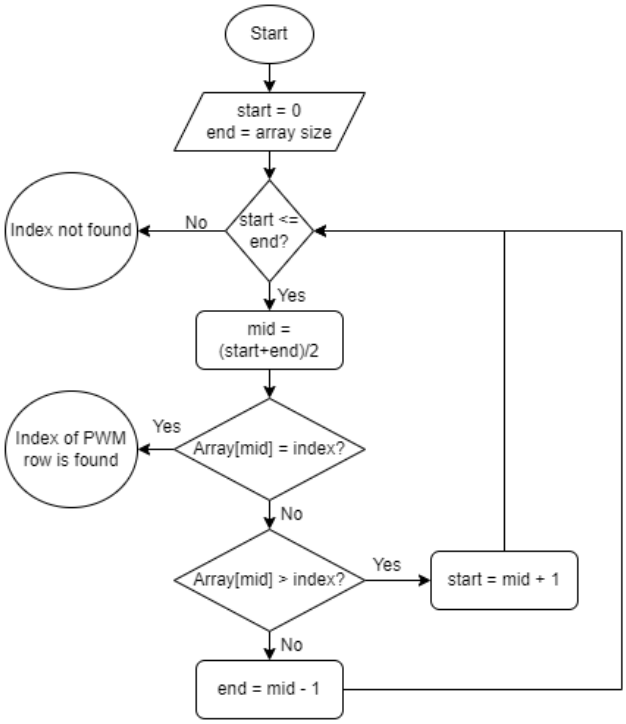

Figure.4: Flow chart of BSA algorithm

5. Simulation and experimental results

The circuit of Figure.1 is simulated in MATLAB/Simulink for various loading conditions. The resulting output voltage and current waveforms for resistive and inductive load are shown in Figure.5 and Figure.6 respectively and the PWM switching sequence is shown in Figure.7. A three-phase 17-level ASLMLI can be obtained by cascading the three units of ASLMLI presented in Figure.1. The resulting three-phase 17-level ASLMLI is simulated in MATLAB/Simulink and the output voltage waveform is shown in Figure.8.

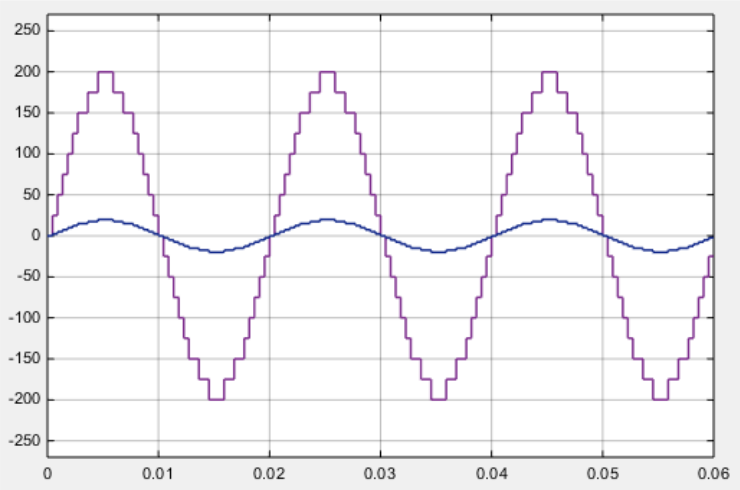

Figure.5: Output voltage and current waveform of 17-level ASLMLI for resistive load

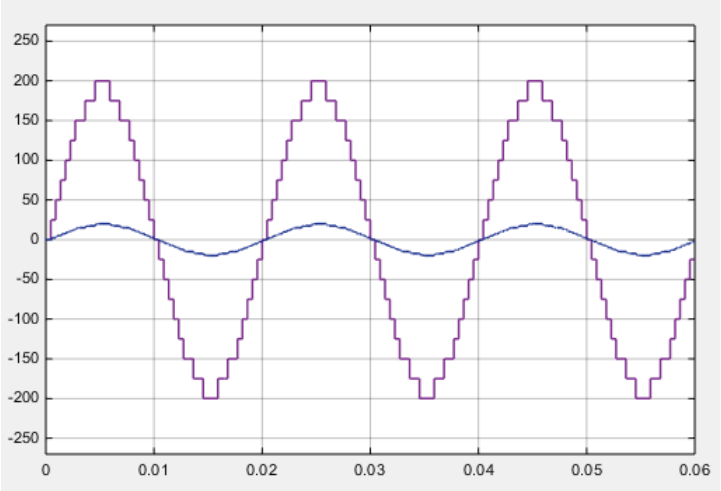

Figure.6:Output voltage and current waveform of 17-level ASLMLI for inductive load

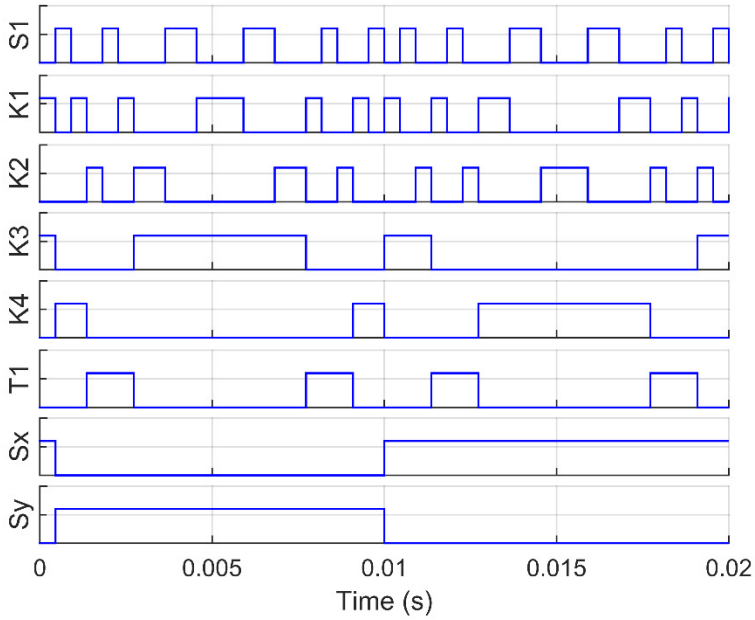

Figure.7: PWM switching sequence for 17-level ASLMLI

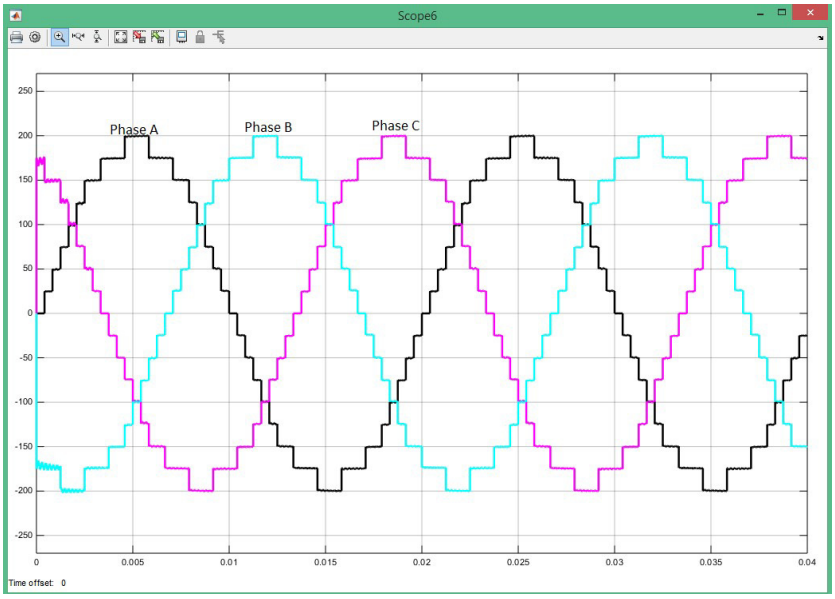

Figure.8: Output voltage waveform of three-phase 17-level ASLMLI for inductive load

The harmonic analysis of the inverter output voltage is carried out and it is observed that the total harmonic distortion (THD) of the output voltage waveform is found to be 6.19%. The harmonic analysis is carried out in MATLAB and shown in Figure.9. As seen from the harmonics plot, the peak magnitude of the fundamental component of the output voltage is 190.6 V when the peak value of the output voltage is 200 V. As per IEEE 519 standard, the THD of the proposed 17-level ASLMLI is slightly higher than the requirement for grid integration purposes. However, a small filter can be designed to attenuate the harmonics further for grid-connected operation.

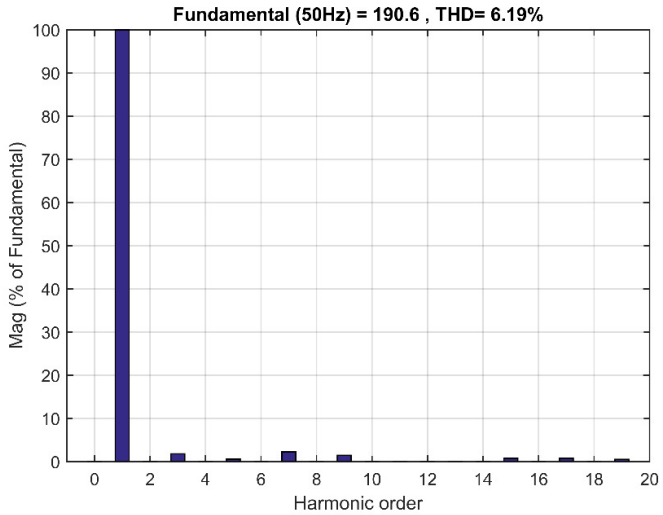

Figure.9: Harmonic analysis of the 17-level ASLMLI

The three units of the 17-level ASLMLI configuration are cascaded to obtain a three-phase 17-level ASLMLI and the experimental three-phase voltage waveform is shown in Figure.10.

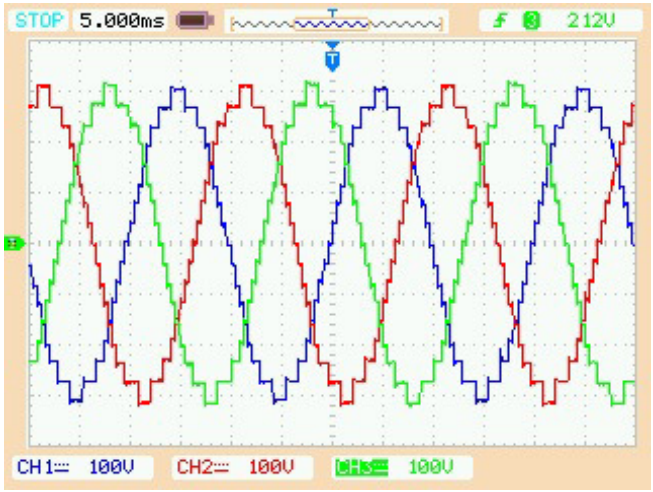

Figure.10: The experimental three-phase output voltage waveform of 17-level ASLMLI

6. Loss and Efficiency Analysis

The two significant types of losses in an MLI are conduction and switching losses. The switching loss takes place at the instant when a switch changes its state. The significant part of conduction loss is the ON-resistance 'R_S' of the switch and the resistance of the antiparallel body diode 'R_D'. The conduction and switching losses for a switch and its body diode are given in [13] as:

$$P_{C,S}($$ (1)

(2)

where, and are the conduction losses of a switch and its body diode respectively. β is the constant that depends on the characteristics of a particular switch.

The average conduction loss assuming that there are '$N_{D,ON}$' number of diodes and '$N_{S,ON}$' number of switches are ON for a given time is as follows:

$$P_C = \frac{1}{\pi}\int_0^{\pi}[N_{S,ON}P_C.$$ (3)

Assuming the linear variation in the voltage and current during the switching instant, the switching loss during the turn-ON time is,

(4)

That finally becomes,

(5)

Similarly, the switching loss during the turn-OFF time is given as

(6)

The efficiency of the ASLMLI configuration is therefore given as,

$$\eta = \frac{P_o}{P_i} = \frac{}{P_o +} \quad (7)$$

7. Power quality monitoring system

The power quality monitoring system is developed that can be used along with the ASLMLI for grid integration purposes. The power quality monitoring system measures various power quality parameters such as power factor, crest factor, RMS voltage and current, different types of powers, and harmonics. A three-phase data acquisition card (DAC) based on L18P01015 current sensors is developed for the grid voltage and current measurements and is shown in Figure.11.

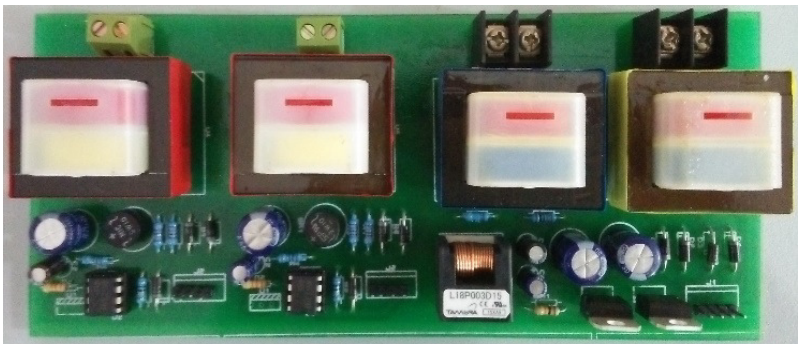

Figure.11: Data acquisition card for grid voltage and current sensing

A LabVIEW-based GUI is also developed for displaying the measured data on a display and is shown in Figure.12.

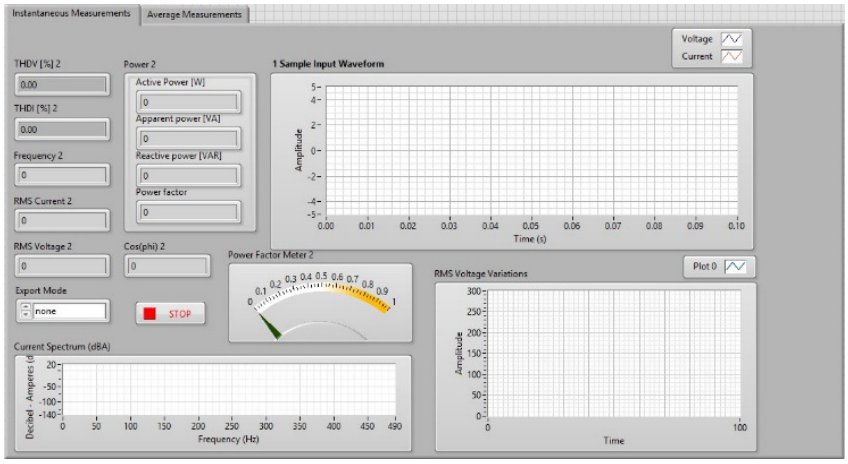

Figure.12: A LabVIEW GUI-based power quality monitoring system

The effectiveness and accuracy of the power quality monitoring system are tested by comparing the measurements with the FLUKE 435 power analyzer and the resulting comparison is shown in Figure.13.

Figure.13: A comparison between the power quality monitoring system and the FLUKE-435 power analyzer

8. Conclusion

This paper proposes an efficient technique for the implementation of PWM for an asymmetrical switch ladder multilevel inverter. The PWM for switches is generated using a binary search algorithm. A power quality monitoring system is also developed using a data acquisition card and a LabVIEW-based GUI. The output voltage waveform of 17-level ASLMLI shows the effectiveness of the proposed PWM switching technique. This technique can generate the switching pattern for almost any MLI and is very useful for grid integration purposes as it simplifies the control scheme.

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