[1]Dr. Mohammad Ahmar Khan

[2]Yatin Chopra

[3]Saurabh Gangola

[4]Dr. Vuda Sreenivasa Rao

[5]Parul Chaudhary

[6]Dr. Mohammed Yousoof Ismail

Advances in Traditional Electrical Validation of High-Speed Serial Connections Using Innovative Debugging Methods and Machine Learning Models.

Abstract: - As technology continues to shrink and more heterogeneous blocks are combined into single System on a chip (SOCs), the design of high-performance integrated circuits is getting more and more difficult. In the course of silicon validation, which includes testing (Wafer Testing, Automatic Test Equipment), digital validation (Functional Data route, FSM), analogue bench validation (Electrical, Interoperability), and system validation, a number of challenges that arise from the complicated design are uncovered. The process, methods, and constraints of each domain are unique. Electrical problems that have already passed through earlier stages of design are the primary focus of analogue validation. The analogue signal or mix signal nature of IPs makes it impossible for digital validation or any of the other post-silicon domains to discover electrical flaws on its own. As a result, studies focusing on analogue bench validation have grown in prominence. Recent developments in analogue bench validation, focusing on high-speed serial interface in particular, are highlighted in the proposed study. In addition, this article summarises recent technological developments that provide avenues for further study regarding analogue bench validation.

Keywords: System on chip, Wafer Testing, Automatic Test Equipment, Electrical, Interoperability, Digital validation

Introduction

As technology continues to shrink and heterogeneous blocks are combined into single systems on chips (SOCs), the design process and silicon validation are both impacted, making high performance integrated circuits more complicated with each passing day. During silicon validation, a wide variety of problems with silicon are found, most of which are the result of complicated system integration and can only be resolved by using improved methodology and methods that are tailored for debugging. The last step in the very large scale integration (VLSI) design flow before silicon is used in practical applications is post silicon validation. Logic and electrical

[1] Dept. of MIS, CCBA, Dhofar University, Salalah, Sultanate of Oman

mkhan@du.edu.om

[2]Assistant Professor SAITM, Gurugram

chopra.yatin3123@gmail.com

[3]Assistant Professor, School of Agriculture, Graphic Era Hill University, Dehradun; Adjunct Professor, Graphic Era Deemed to be University, Dehradun, Uttarakhand-248002, India

Mail id- sgangola@gehu.ac.in

[4]Associate Professor, Department of Computer Science and Engineering, Koneru Lakshmaiah Education Foundation, Green Fileds, Vaddeswaram, A.P., 522302.

vsreenivasarao@kluniversity.in

[5]Assistant Professor, School of Agriculture, Graphic Era Hill University, Dehradun; Adjunct Professor, Graphic Era Deemed to be University, Dehradun, Uttarakhand-248002, India.

Mail id- parulchaudhary@gehu.ac.in

[6]Dept. of MIS, CCBA, Dhofar University, Salalah, Sultanate of Oman"

validations, software debugs, and ensuring the usefulness of design functions are all part of silicon validation. The goal is to find any issues that are preventing silicon from working according to specification, identify the root cause of the problem, and fix it either through design changes, on-board modifications, or software settings. Manufacturing (Wafer Testing, Automatic Test Equipment), digital (Functional Data Path, FSM), analogue bench (Electrical, interoperability), and system validation are all concurrent areas that make up silicon validation. The process, methods, and constraints of each validation domain are unique. The presentation of application software on the customer board or the actual application board usually serves as a gatekeeper for product releases. When doing analogue bench validation, it is important to evaluate all electrical components of the design. This includes the interface between analogue circuitry and the requirements, coupling between the power and ground planes, cross talk, and reflections. Any problem found in the Post Silicon Validation domains makes it difficult to troubleshoot electrically, which is a continual challenge for analogue bench validation. Analogue bench debug is likely to follow any problem detected throughout the validation stage. Because of this, analogue bench validation becomes quite difficult. Because it makes up for the shortcomings of the other silicon validation zones, it is an essential component of the whole. Consequently, postsilicon analogue bench validation is still a vibrant and promising field of study. The communication system makes advantage of the high speed interface controller and physical hardware, such as DDR, SATA, PCIe, USB, Ethernet, MIPI, HDMI, and so on, to transport data at very high speeds to and from external devices. Because of their completely analogue behaviour, any kind of silicon validation would have a hard time catching their defect. Moreover, outside of the analogue bench validation setting, it is challenging to analyse the signal integrity and mixed signal behaviour of these signals. Overshoot, undershoot, hum noise, and reflection are all examples of reflection-related noise; false trigger timing errors are caused by crosstalk between many networks; and noise margins are reduced due to rail collapse, which causes bounce of the ground. Signal integrity concerns might be hard to detect without HSSI certification. When testing and analysing high-speed serial interfaces, jitter measurement is crucial due to the extreme sensitivity of serial link performance to clock quality. In order to verify that a component satisfies a specified jitter parameter (such as jitter tolerance) and to validate anticipated jitter properties during development and debug, precise measurements are essential.

Problems with USB mass storage device (MSD) recognition on PCs and laptops are common in the real world. The message "USB device not recognised" is shown, which is usual. Data transmission speeds can be slower when USB3 MSD is connected as USB2. Connecting an MSD to a host allows it to direct hardware-based state changes and dialogues. Since these delays are not specified in the USB 2.0/3.x standards, they are often determined by firmware drivers or developers based on experience or experimentation. Device identification problems (as mentioned above) with consumer USB MSDs from different manufacturers are caused by this standard gap. Article [3] discusses time-out failures and process hangs that occur during repetitive enumeration. But they don't touch on how to troubleshoot problems with consumer USB MSD enumeration or detection.

The first stage of the investigation involves a thorough examination of the silicon validation ecosystem as a whole, as it is usually found inside a semiconductor business. The focus here is on the development of analogue bench validation. The development model for post-silicon validation is laid out. So, the paper explains how the silicon validation flow works and why it's important within the larger context of the silicon validation flow. As has been said, the reasons for the expansion of analogue bench validation will persist in other validation methods, new industry standards, and holes in the current validation framework. All of these things point to the fact that there are a lot of issues in the newly formed area of study known as analogue bench validation. Possible research topics in validation and related areas include resolving a number of pressing obstacles. In order to show where we are now and where we need to go, we also go over certain validation approaches for high-speed serial interfaces. For high-speed serial interfaces, the difficulties of analogue bench validation are highlighted. Factors discovered in our analysis are anticipated to form the basis of future validation approaches. A phase-locked loop (PLL) is a crucial building component for fast serial interfaces. Thus, it is crucial for analogue bench validation and characterisation to debug and overcome the recognised difficulty of PLL with regard to diverse serial links. All high-speed serial interfaces (PCIe, SATA, USB3 etc.), on-chip Phase-Locked Loops (PLLs), and on-board devices (Ethernet PHY) get the clock without additional on-board clock sources using on-chip single source clocking, lowering the silicon bill of materials (BOM).This work go over the problems and difficulties found during debugging and validation (such as the high jitter values seen when characterising the PCIe, SATA, and

SerDes transmitter clocks), compare various configurations, and provide a workaround for USB-PLL and an on-board solution. Although this study was conducted on a real-life system-on-chip (SoC), the resulting design and suggested resolution are applicable to a wide variety of SoCs. Designing new clocking with these sorts of possible concerns in mind requires designers to understand the design's sensitivity to clocking changes and the influence it may have at various locations, which is one of the main conclusions from this study. It is beneficial for validation engineers to anticipate clocking changes, do thorough characterization, and debug accordingly. We have seen several device identification difficulties in various serial interfaces.

Therefore, designers and validation researchers always face the difficulty of device startup and data transfer failure difficulties with high-speed hosts and devices. We have identified two primary specification limitations during host controller initialization as the root cause of these failures (timeout error, enumeration failure, etc.): the first is the time it takes for the xHCI controller to poll for changes in the Connect Change Status, and the second is the lack of a discharge timing specification for VBUS during power down. For the purpose of analytically estimating the USB power discharge process, we have presented a model based on dual resistors. Additionally, experimental evidence and modelling results from a 16 nm USB host validate this concept. Additional research and testing of the model reveals its inadequacy in accurately forecasting the discharge timing. This is because not all gadgets have a resistive component.

Representing the device as a two-valued resistor does not accurately depict the discharge profile of the USB power, but it provides a decent approximation. We have therefore shown a dual current based model that is an enhanced representation of the USB power discharge (VBUS) process. We enhance the discharge profile accuracy and lower the model versus silicon inaccuracy by up to 75% using this model.

Signal Integrity (SI) measures, such as peak-to-peak voltage and jitter, are affected by board traces/channel for high speed serial lines with data rates above 1 Gbps, causing the test to fail the target specification. Hence, de-embedding is done to remove channel effect deterioration and isolate the DUT (transmitter) performance. The time and money spent on the VNA/TDR and SDLA needed for de-embedding is going towards the same SI assessment, which is basically being done twice: once on the non-embedded signal and again on the de-embedded signal. In order to address these shortcomings, we have put up a set of machine learning models. Without actually running the traditional de-embedding procedure (using s-parameter files), users may utilise these models to get the de-embedded SI values (jitters, amplitude, etc.).

A Perspective on the Evolution of Analog Bench Validation and Characterization

Designers of SOCs are cognizant of the fact that, upon receipt of the initial silicon, there will be unforeseen mistakes that must be corrected. Sophisticated and intricate subsystems of interdependent systems are blamed for the mistakes. The power supply or the clock might also be a cause of inaccuracy. Process, voltage, and temperature (PVT) issues, crosstalk noise, and synchronisation faults are other potential causes. They may even cause software and hardware to interact in ways you wouldn't anticipate. Testing the interplay of the embedded software components is an integral part of silicon validation for contemporary CPU designs. Software debugging and electrical and logic validation make up the bulk of the post-silicon validation process. In silicon validation [7], testing the chip's efficiency at a set speed under varying operating circumstances is of utmost importance. Neglecting to consider the efficiency of the chip might result in disastrous failure in real-time applications. In cases when the design is not performing as expected, debugging silicon failure involves identifying the source of the fault. Initial silicon validation debugging calls for months of dedicated technical work. As the technology length decreases (below 28 nm), the silicon certification procedure becomes more challenging. Making sure design functionalities operate as intended, finding problems that are preventing silicon from performing as expected, getting to the bottom of what's causing the problem, and fixing it either by design or software settings are all goals of post-silicon validation. Before silicon is used in real-world applications, it must first undergo silicon validation as part of the system-on-chip design pipeline. Automation in testing (manufacturing testing, wafer probe), system validation (for application level testing), and digital validation (for digital portions of integrated circuits) make up the bulk of it. Analogue bench validation is used for digital signals with an analogue nature, as well as mixed and pure analogue signals of integrated circuits [8]. Members

of the digital, analogue, system, and ATE teams make up the semiconductor industry's post-silicon validation teams. This is why analogue bench validation is used by a lot of organisations. [9]

Fig. 1: Post Silicon Validation

There has been and will be a great deal of study on silicon validation. The digital validation part of the silicon flow has been the primary focus of these studies, with an emphasis on logic validation of silicon. In contrast to the earlier practice of producing digital and analogue integrated circuits independently, mixed signal systems on a chip (SoC/IP) are quickly reaching maturity. A mixed signal system on a chip (SoC) or integrated circuit (IP) hosts both digital and analogue components. Validation on an analogue bench is therefore as important in silicon flow. Digital validation [10] for functional bug hunting, automatic test equipment (ATE) for manufacture bugs, full volume testing, analogue bench validation for characterization of the analogue nature of digital signal, analogue IP validation, and system validation for application level testing are the main divisions of SoC validation (PostSilicon Validation), as shown in Fig. 1. Completely finding and addressing defects via verifications, automated test equipment (ATE), and digital validation becomes a tough undertaking for systems on chip (SoC) technologies that include high speed, high integration levels, and scaled technologies. There are electrical validation processes for every mixed-design circuit. To make sure this complicated design works as expected in all the defined scenarios, the digital validation engineer checks it. It is rather challenging to embed an analogue design into a digital system and then validate it. Thus, a fresh avenue for investigation becomes available. Due to the inadequacy of digital validation alone, analogue bench validation is vital. Pure analogue signal IPs are immune to digital validation's ability to find analog/electrical defects. Analogue bench validation is further complicated by the fact that sophisticated System-on-Chips (SoCs) have several digital CPU cores, co-processors/accelerators, mixed signal IPs, and a high-speed serial interface [11]. To evaluate expected behaviours under defined operating circumstances, analogue bench validation uses produced chips with digital and analogue IPs in actual application contexts. The goal is to eliminate bugs completely. Analogue bench validation and characterisation are very challenging and costly, according to many semiconductor firms. The problem originates from the fact that current methods are unable to handle the upcoming systems' enormous complexity..

Automatic Test Engineering

ATE is a well-liked technique for finding production errors. Although ATE may only execute pattern-based stimuli, among its many restrictions, these bugs may nonetheless exhibit analogue behaviour. As a result, even little interactions between silicon components may cause silicon flaws. The interaction between the silicon components might be caused by physical factors or by design faults, namely logic or functional defects. This is because analogue IPs are parametric. It is well known that in order to conduct ATE testing, patterns are loaded into the DUT. These patterns are unable to exercise or shake hands with the DUT subblocks at the software level. Application level testing is always superior than ATE testing. Because of its intrinsic constraints, it requires a degree of validation and design that is comparable to but higher than wafer level testing, but lower than analogue bench validation and application level testing. The effectiveness of the ATE testing is due to the test measures, which include single-stuck-at coverage, transition fault coverage, and N-detect coverage (pattern based). The experimental proof by Ma et al. [15] may help us grasp the efficacy of measures for real chips better. Such statistics enable automated test pattern development and defect simulation using stimuli drawn from design verification. Similar to pre-silicon verification, the main goal of ATE testing is to find mistakes that follow certain patterns. However, as shown in the chapter's section on the flow of analogue bench validation, the primary objectives of this process are to identify and fix the design defects at their source. Design effort and expenditures are often dominated by this [16]. A defect's location may be determined using diagnostic tools. The sequential circuit, which is similar to a combinational circuit in test mode, is enabled by these methods' reliance on scan design for testability (DFT). Analogue bench validations cannot be solved using ATE based bug localization methods. This offers a fresh chance to validate analogue circuits on a bench. It is much more cost-effective to utilise a bench setup in an analogue configuration to locate the issue, identify it, and correct it than to use ATE-based testing, which is used to discover analogue defects. While digital validation requires less

initial investment, it misses problems caused by analogue or mixed signal designs. Due to scaling technologies allowing for new levels of device integration, the number of undetected analog/mixed-signal design defects in silicon is growing. These are only some of the functional concerns with high performance integrated circuits; there are more yield related concerns, including operating frequency limits. These mistakes manifest in the unique environment of system on chip operations. Predicting their impact is challenging. An active area of study in the field of stochastic test stimulation generating algorithms is the identification and correction of errors in conventional manufacturing test generation. Since the design defects' characteristics are very unexpected, this opens up new avenues for investigation [17]. In expose/standalone mode, ATE primarily monitors the static parameters.

All of this testing takes place on silicon after packaging. Analogue bench validation is still needed for several performance measures, such as ADC ENOB, phase noise of the clock signal, and the measurement of the eye diagram. Compared to application level setup, ATE test circuit board configuration and instrumentation setup have inherent constraints. Setting up an ATE test circuit board differs from setting up an application board for a client. In addition, the configurations of the end user applications may vary from the ATE configurations. The success of the ATE in the postsilicon validation cycle serves as an inspiration for the research conducted on the analogue bench. The gadget is repeatedly stimulated by the test engineer. A vector loop is the method most often used. The test engineer must connect the optical probe to the imaging equipment in order to carry out the same task. Maintaining tight synchronisation between the two systems is crucial for ensuring accurate and repeatable outcomes [18]. Various assessment methodologies will be used to examine the internal device behaviour of the DUTs. Validation on an analogue bench might benefit from several different ATE test methodologies. Fault simulation, coverage estimate, mixed-signal ATE technology, and power supply impedance emulation are only a few examples of ATE approaches. A power supply's impedance emulation may eliminate overkills and underkills caused by an impedance mismatch between the client board and the ATE [14]. The environment for Automatic Test Equipment and Validation has been the focus of further efforts [19]. Analogue bench validation may greatly benefit from some of these advancements in ATE research.

One way to examine the connections between different parts of an integrated circuit is via boundary scan testing. One test approach that helps characterise I/O and is also useful for troubleshooting is the boundary scan analysis. In order to analyse the sub-blocks of an integrated circuit or measure the voltage, it watches the states of the pins on the circuit. Although boundary scan tests stand alone for I/O, they do not validate IO features or compatibility, among other implementations. Analogue bench validation research is driven by the utility of boundary scan tests in the post-silicon validation flow stage, despite the constraints of these tests. In the past, device testers may have had difficulties while testing I/Os at high speeds. On the other hand, I/O testing is still limited by price and quality. Several DFT approaches are described in literatures as potential solutions to these problems. The loopback idea is at the heart of the most prominent and widely used method for testing serial transceivers (more on this in section IV). This way, we may verify the transceiver's operation without using the pricey high-speed, high-pincount device. Traditional scan testing methods face even more difficult and daunting obstacles. The nondeterminism and speed of the serializer and de-serializer (SerDes) are the causes of this. As part of the system-on-chip design, During an Emulation Test, a different model of hardware is used to simulate the DUT hardware's actions. By compiling source code in a format that the emulation system supports, the emulation model is able to take use of hardware description languages like Verilog. The typical objective is to do a functional evaluation of the system and develop debugging [24]. The benefits of a hardware model, like as performance and system integration, are combined with the programming freedom of simulators in hardware emulation. The ability to execute ASIC designs in a fully functional system environment at decreased frequencies is made available via hardware emulation. This allows us to begin developing the system's software at an earlier stage in the development cycle and debug the design prior to its deployment on silicon [25]. As mentioned earlier, the validation flow's emulation testing stage only verifies the operation of digital logic, excluding any usage of analogue logic or blocks. The hardware imports Verilog and VHDL, which include just the digital portion of the system on a chip. It is only possible to verify the accuracy of digital connection and the operation of the analogue digital interface at lower frequencies in order to verify the software initialization and configuration of the analogue logic section. Because creating an IP in complicated SoC may be a time-consuming job, this is a huge aid when setting up the analogue bench for validation. The digital validation

process checks the logic's functioning using the RM (Reference Manual document) Register Information. When it comes to registration information, RM is considered the top standard. Various tests, including as the register reset, read/write, and functional tests, are conducted to ensure the accuracy of the register memory map. Logic analyzer and field-programmable gate array (FPGA) testing are the norm in digital level testing. It also does read/write operations on the contents of the register. When testing the electrical properties or operation of a system on a chip (SoC), it is common practice to examine the pin status. In order to simulate an actual user experience, digital functional validation is carried out on a dedicated design test board. This board is capable of executing scripting environments like Python and TCL on hardware, simulating an application-type situation.

Research on analogue bench validation originates from digital validation, which has its own set of restrictions. Digital validation ideas, including as bug identification, localization, and root cause analysis, have become increasingly comprehensive as they have progressed from theory to industry practice. Additional progress towards failure reproduction and methods to replicate failures may be found in [12]. In [10], we see more work on error detection. The most effective method for handling processor core defects is the IFRA (Instruction Footprint Recording and Analysis) methodology, which has a 90% success rate. For effective failure intimation and root cause investigation, real-time response data may be used. With this, digital validation may be made more observable. One typical method of debugging in digital validation is using on-chip trace buffers. It is even possible to employ the formal claims from the simulation traces in a scalable way. This is a great tool for finding problems that caused failures at module borders. A prominent method known as latch divergence analysis is used to filter out state variation from post-silicon digital validation. A modified back tracing approach may be used to analyse information from these filtered out states in order to identify the underlying cause. For efficient digital validation before and after silicon fabrication, a number of improvements have been included to speed up error detection and runtime. You may try to fix the design flaw without re-spin when you've located, analysed, and determined the source of an issue. Common methods for designing microprocessors include microcode patches and field repairable control logic. For post-silicon metal repairs made possible via ECO routing or spare cell insertion, there is another method known as FogClear. For electrical testing of hardware faults, the semiconductor industry has traditionally relied on automated test environments (ATEs) and digital validation. Unfortunately, owing to setup limitations, this validation cannot catch high performance analogue faults. This is supplemented with analogue bench validation, which offers a better means to face these analogue difficulties.

Device Detection Issues and their Resolution at High-speed Serial Interface

The U.S. Serial Bus interface has greatly improved our quality of life. You won't have to fiddle with the device's settings every time you connect it in thanks to its self-configurable interface. The ability to power tiny devices straight from the USB [86] interface is what makes the USB system so useful in embedded environments; it's known as hotpluggability. It also gets rid of the necessity to restart the peripherals after replacing them. Since its launch in 2010, Superspeed USB, also known as USB3.x [87], has developed with new and exciting capabilities. The development's high points include data flows, effective power management, dependable control over time, and data speeds of up to 20 Gbps. The USB host controller's data structures, operating paradigm, and registers are described in the Extensible Host Controller Interface (xHCI). It is crucial to the deployment of these features since it guarantees compatibility with earlier versions. When using a desktop or laptop computer, end users often encounter problems with USB mass storage device (MSD) identification. The message "USB device not recognised" appears as an error. Take note that sometimes USB3 MSD may connect as USB2, which will cause data transmission rates to be slower. An MSD's role in facilitating hardware-based state transitions and discussions begins upon host connection. Negotiations may also benefit from the state machine's time delays. Even though these delays aren't specified in the USB 2.0/3.x specifications, firmware drivers and developers implement them experimentally. Therefore, consumer USB MSDs from different manufacturers have device identification problems due to the standard difference.

This study delves into the topic of device identification and the LTSSM backdrop, specifically focusing on 16nm networking system on a chip (SoC) that has complete embedded setup and supports an embedded operating system (OS), often referred to as uboot-OS. The eXtensible Host Controller Interface (xHCI) based USB controller revolves on LTSSM, which stands for Link Training and Status State Machine (Fig. 2). The xHCI standard describes the USB host controller at the register level and serves as a specification for the

computer interface.
It specifies how a host and a consumer USB device should interact during negotiations and hardware-based state changes. Link is considered trained and prepared for the enumeration sequence once the LTSSM reaches a state called U0 after following the stated sequence. When the host detects an MSD, it updates its port status and control register (PORTSC) to reflect the new state of the Connect Change Status (CCS) bit. When the CCS bit is "set," it means that the port configuration exchange is complete; this is called device (MSD) detection from the perspective of design implementation..

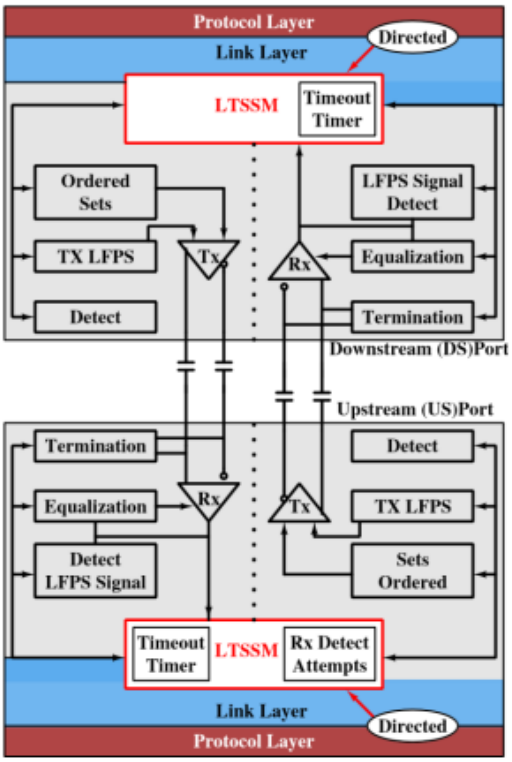

Fig. 2: The link training and status state machine (LTSSM) in USB3.x Devices

In a software driver, the timing delays are configured. These timings are developer-specified and not stated in the USB 2.0/3.x standards; as a consequence, consumer USB devices from different manufacturers sometimes fail to recognise one other. There have been mentions and conversations about USB device identification concerns in system on chips, and they have offered various analyses of the same problem. While testing enumeration and data transfer at an embedded setup with a 16nm SoC and uboot-OS in the lab, the problem was noticed during connection training between the xHCI host and consumer device. Setting the CCS bit in the PORTSC register allows the host controller to notify the driver of the device's connection, as shown before. In embedded system testing [100], it was discovered that the driver could not identify the connection of a couple of super-speed devices when confirming the host-device connection between the host controller and a USB mass storage device.

Prediction of De-embedded Signal Integrity Parameters using Machine Learning Based Models in High Speed Serial Link Characterization

The use of machine learning is gradually expanding in the very large scale integration (VLSI) sector. There are two main parts to the chip design flow: the steps taken before silicon is used and the steps taken after silicon is used. The steps taken before to the chip's tape-out, known as "pre-silicon," include things like design, verification, integration, emulation, and so on. After fabrication, the chip proceeds to the lab for testing, validation, characterization, and other post-silicon processes. Engineers and academics are using various machine learning methods during the presilicon process to discuss channel design and high speed SERDES (Serializer-De-serializer).

Regarding the use of ML for post-silicon analogue validation and characterisation, we were unable to locate any substantial study. It should be mentioned that the purpose of validation and characterization is to check the chip for any possible errors or flaws. As a result, reliable and accurate test methodologies are required.

Conclusion

The integration of innovative debugging methods and machine learning models has significantly advanced traditional electrical validation processes for high-speed serial connections Overall, the combination of traditional electrical validation techniques with innovative debugging methods and machine learning models represents a significant leap forward in ensuring the reliability, performance, and efficiency of high-speed serial connections in various applications. As technology continues to evolve, further advancements in this field hold the promise of even greater improvements in validation processes and product quality.

References

1. Lu, S., Zhong, L., Wu, X., Li, Y., & Wu, S. (2020). A Novel Machine Learning-Based Approach for High-Speed Signal Integrity Analysis in Multi-Gbps SerDes Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 67(6), 1993-2006
2. Cai, J., Huang, M., Xu, S., & Shao, Z. (2020). An Integrated Machine Learning Approach for High-Speed Serial Link Design. IEEE Access, 8, 183678-183689.
3. Kim, J., Seok, M., Kim, S., & Kim, H. (2019). Signal Integrity Analysis using Machine Learning: A Review and a New Perspective. *Electronics, 8*(9), 1073.
4. Dai, X., & Jiang, J. (2018). A Machine Learning Approach for High-Speed Signal Integrity Analysis in Multi-Gbps SerDes Design. *IEEE Access, 6*, 28687-28697.
5. Chen, T., Zhang, L., Huang, T., & Cao, Y. (2018). Deep learning for signal processing: from traditional neural networks to deep learning. *IEEE Signal Processing Magazine, 35*(6), 117-121.
6. R. Medico, D. Spina, D. V. Ginste, D. Deschrijver, and T. Dhaene, "Machine-learning-based error detection and design optimization in signal integrity applications," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 9, no. 9, pp. 1712-1720, 2019
7. Ichiyama, K.; Kusaka, T.; Ishida, M. A jitter injection module for production test of 52-Gbps PAM4 signal interfaces. In Proceedings of the International Test Conference, Washington, DC, USA, 9–15 November 2019.
8. Ergenc, D.; Onur, E. Poster Abstract: ISDR: SDR-in-the-loop Simulation. In Proceedings of the INFOCOM 2019-IEEE Conference on Computer Communications Workshops, INFOCOM WKSHPS 2019, Paris, France, 29 April–2 May 2019
9. Gabauer, J. Test and Validation of the Integrity and Performance of High Speed Interfaces; Course: ENGG7290; The University of Queensland: St Lucia, Australia, 27 June 2019.
10. Ahn, S.U.; Seo, B.K.; Kim, H.W.; Shin, Y.S.; Kim, H.T.; Oh, G.G.; Kim, Y.D. Cost-Effective Test Method for screening out Unexpected Failure in High Speed Serial Interface IPs. In Proceedings of the International Test Conference, Washington, DC, USA, 26–28 October 2020.
11. Ahn, S.U.; Seo, B.K.; Kim, H.W.; Shin, Y.S.; Kim, H.T.; Oh, G.G.; Kim, Y.D. Cost-Effective Test Method for screening out Unexpected Failure in High Speed Serial Interface IPs. In Proceedings of the International Test Conference, Washington, DC, USA, 26–28 October 2020
12. Hoefflinger, B. ITRS: The International Technology Roadmap for Semiconductors. In Chips 2020; Springer: Berlin/Heidelberg, Germany, 2011; pp. 161–174.
13. Abdennadher, S.; Meixner, A. Why defect based testing works for high-speed I/O interfaces. In Proceedings of the DTS 2020-IEEE International Conference on Design and Test of Integrated Micro and Nano-Systems, Hammamet, Tunisia, 7–10 June 2020
14. Masood, S.; Khan, S.A.; Hassan, A. Simulating Synchronization Issues on a Multiprocessor Embedded System for Testing. In Proceedings of the 2021 IEEE International Conference on Information Communication and Software Engineering, Chengdu, China, 19–21 March 2021