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Ultra-Low Power 9T FinFET Based SRAM Cell for IoT Applications

Abstract: - The rapid proliferation of Internet of Things (IoT) devices has escalated the demand for energy-efficient memory solutions. The development of SRAM (Static Random-Access Memory) has gathered significant attention, particularly for low-power applications and portable devices. This research introduces a novel approach to ensure robust performance and operational integrity, all while adhering to stringent power constraints amidst process and temperature fluctuations. This quest for alternative nano-devices has been ignited by the scaling and channel control challenges intrinsic to CMOS technology. Among the array of alternatives, including FinFETs, TFETs, and CNTFETs, FinFETs have emerged as strong contenders. FinFET SRAMs contribute to the ongoing drive for electronic devices to become more compact and energy-efficient. They offer a distinct advantage as a promising CMOS substitute, attributed to their high performance, stability, with low power consumption characteristics at the nanoscale. The study proposes an ultra-low power 9T FinFET based SRAM cell meticulously designed for IoT applications. Leveraging the unique attributes of FinFET based 9T cell, the proposed SRAM cell is tailored to achieving minimal power consumption while maintaining inherent stability. The study assesses the performance of the proposed SRAM cells for power dissipation, stability, speed, and energy efficiency, and compares them with existing SRAM structures. The results are obtained through the Monte Carlo simulation technique, which evaluates circuit performance under specified conditions. The study achieves remarkable efficiency gains with 9T SRAM cells compared to other configurations. Additionally, the reduced read and write access times facilitate expedited data retrieval and storage operations.

Keywords: FinFET, SRAM, CMOS, Energy-Efficient, Performance, Power.

I.Introduction

According to ITRS 2009 [1] glossary, More than Moore (MTM) is the incorporation of functions into services that don't necessarily adhere to Moore's law scaling, yet offer additional value through various means. Memory components constitute a significant portion of a semiconductor die, with memory circuits occupying approximately 60 to 70 per cent of chip space. Miniaturization has become a prominent design principle in contemporary electronic devices, aligned with the market trend towards compact and portable devices. The scaling of CMOS (complementary metal oxide semiconductor technology) has made the pursuit of miniaturization achievable, a characteristic pervasive in nearly all electronic devices [2]. Today, intelligent devices are characterized by their remarkably compact form factors.

CMOS scaling has reached its limit at this point, and alternative options for silicon or CMOS devices, such as TFETs, FinFETs, and CNTs, have emerged as potential solutions. It would appear that the FinFET device is a promising technology, and it has the potential to be a very promising alternative for low-power developing electronics circuits [3]. Also, FinFETs can work at lower voltages and lower medium frequencies for operations. Because it is resistant to the CMOS short-channel effect and has higher threshold voltages, it is a viable alternative for SRAM memory [4]. FinFET has also been shown to be a viable alternative for DRAM memories. FinFET-based memories have been proposed and approved, mostly as a result of their advantages over CMOS in terms of reduced size and lower levels of leakage. Because the FinFET is a multi-gate transistor, it possesses exceptional electrostatic characteristics as a result of the multiple gates operating on the channel [5]. FinFET devices also feature "Scaling" in addition to the aesthetic appeal of MOSFET devices.

SRAM (Static random access memory) constitutes a considerable portion of the real estate on contemporary VLSI chips, thereby wielding significant influence over chip performance [6] and power consumption [7]. Thus, the imperative to diminish SRAM power usage while adhering to specified criteria becomes paramount. A potential avenue for accomplishing this objective involves supply voltage variations translating into energy savings and exerting an exponential decline in static power dissipation [8].

Similarly, Utilizing SRAM for high-speed caches results in a deceleration of SRAM functionality. For portable applications, SRAMs must possess attributes of ultra-low power consumption, great performance, with exceptional stability in read/write operations. While SRAM cells designed for 20 nm FinFET technologies can significantly reduce power usage to minimal levels, achieving remarkable power efficiency, they contend with substantial data stability issues during write and read operations. Consequently, conventional SRAM cells and their predecessors

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face challenges in operating at ultra-low voltages. This study is committed to addressing and overcoming this predicament.

II.Related work

The evolution of multi-gate devices from their single-gate counterparts stems from continuous endeavours to enhance current flow and exert superior control on Short Channel Effects (SCE). Referred to as "DELTA" in contemporary terms, the original self-aligned vertical multi-gate MOSFET features channels on the body's sidewall, with naturally self-aligned front and rear gates [5]. This compatibility led to the emergence of FinFET and other multi-gate topologies alongside traditional CMOS. The shortening of gate length has triggered Short Channel Effects (SCE), encompassing sub-threshold elevation, threshold voltage fluctuations, and punch-through occurrences between drain and source [9]. The primary aim of the FinFET structure is to minimize body size, preventing leakage channels and facilitating effective gate control. FinFETs are fabricated using silicon on Insulator or bulk silicon, with their 3D structure composed of thin, vertically oriented bodies known as Fins. The three-sided gate configuration enveloping the channel augments its performance. Since the FinFET channel is oriented vertically, the device's width is determined by the Fin's height, offering the potential to amplify current by increasing the width or the number of fins [10].

According to the author of [11], 8T SRAM improves both work reliability and power consumption drop. The study has provided various suggestions for enhancing leakage control and stability in FinFET SRAMs. In [12], the author introduces a feedback method using Schmitt trigger-based dual-port SRAMs for enhanced stability, while other research focuses on reducing variations and improving stability in FinFET SRAMs. The recent announcement by Intel [13], has propelled the development of nanoscale FinFETs, with the company adopting At the 22 nm technology node, FinFET emerges as the fundamental CMOS device of choice. Within the domain of FinFET technology, configurations with two to three gates are common, presenting a quasi-planar architecture that entails distinct fabrication techniques, which can be effectively balanced. Fabrication of FinFETs utilizes wafers composed of bulk silicon and silicon on insulators (SOI).

To enhance the read performance in addition to write and read margin of the 6T SRAM cell, a standard back-gate bias technique was employed. This approach employs a reverse bias to address leakage issues [14]. Conversely, in an 8T cell configuration, the stability during read operations aligns with a hold stability, since the read operation current doesn't considerably distress the cell nodes. During read mode, drain current is augmented with increasing the voltage of back-gate, thereby improving read performance. During standby leakage current is minimized with this voltage at zero or negative value. A study [15] suggests that read operations at higher supply voltage helps maintain noise margins, while write operations performed with a lower voltage simplifies writing, ultimately optimizing the read/write margins for stability in SRAM.

A FinFET 8T-Decoupled SRAM [16] effectively eliminates stability issues linked with half-selects due to persistent ON word lines in unselected cells. While enhancing cell stability, the authors maintained the design's functionality. Various studies have encouraged 8T SRAM due to its low power and improved stability [17] integrated with dynamic gate voltage adjustment [18], pass gate feedback [19], and p-type pass transistor [20]. The 8T FinFET based SRAM cell in a study [21] enhanced read and write margins, and another study [22] presented the application of sub-threshold FinFET in SRAM cells to achieve power reduction. The robustness of FinFET-based 6T SRAM cells is explored and recommended by another study [23]. In conventional 6T employing FinFET in SRAM, as presented in the Figure, the challenges posed by process variations and fluctuating supply voltages significantly impede the simultaneous maintenance of both operations, primarily leading to read failures [24].

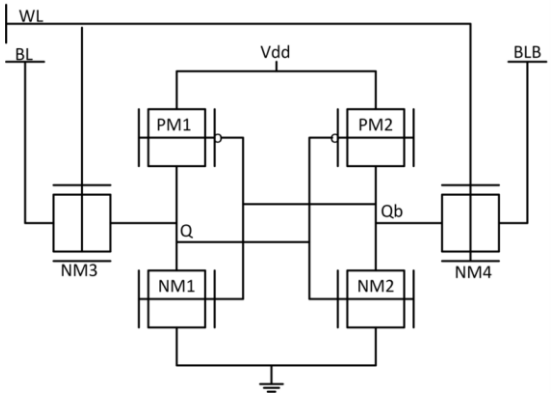

Fig. 1. Conventional 6T SRAM at 18nm [24]

The researcher [25] implemented an innovative approach using a differential SRAM cell with a feedback reduction technique to enhance read stability. They used larger access transistors to improve cell writing capability, albeit at the expense of additional area. Another study [26] reported the development of a 9T SRAM cell using a Schmitt trigger. To increase stability in read operation, inverters with Schmitt trigger were included in the main latch circuitry. Furthermore, the write margin was increased by combining selected power gating and a write assistance

approach. Various methods to reduce the supply voltage were also employed to enhance write margins in SRAM cells [27] [28]. Lowering the supply power disrupts the pull-up network, facilitating easier data writing at the storage node. Furthermore, increasing the virtual ground voltage within the pull-down network [29] enhances SRAM cell write capability [30]. 11T SRAM cell [31] has exhibited a significant improvement in write noise margin. This enhancement was achieved by substituting the ground signal with increased negative voltage at bit-line.

A study on an 11T SRAM cell [32] demonstrates notable stability and moderate performance, coupled with a significant decline in read power dissipation. The investigation involved a comprehensive analysis of key design metrics, including read current, read power, and signal-to-noise margin, for their proposed 11T cell, in comparison with several other considered topologies. However, the challenges of data stability amid persistent process variations besides leakage power were addressed in previous research [33], resulting in a remarkable enhancement in static power management and robust writing performance compared to process deviations. A specialized 11T SRAM cell was intricately designed to offer extended read and write stability, catering specifically to applications in the realm of the Internet of Things.

An innovative approach is presented with the introduction of a differential 8T SRAM-NEW to achieve more stable read data and improved write performance [34]. Furthermore, the 10T SRAM cell [35] addresses the read-disturbance issue identified [36] by incorporating distinct read and write ports that effectively isolate the storage nodes from the bit lines through read operations. The utilization of additional signal VGND in the 10T P-PN bit-cell serves to mitigate leakage at bit line in the read track as well as enhances stability. Additionally, another 10T SRAM configuration has been proposed [37] for near-threshold operations, boasting strong read and write margins. Despite its higher active power consumption, this cell exhibits effective performance at both super- and near-threshold levels.

In response to various challenges faced by SRAM, this research introduces a novel solution in the form of a 9T SRAM design, employing nine transistors instead of the conventional 6T or 8T configurations. The incorporation of FinFET technology into the 9T SRAM yields several beneficial results, driven by its enhanced electrostatic control, which leads to reduced leakage current and increased overall power efficiency.

III.Proposed Ultra Low Power 9T SRAM Cell

The proposed SRAM cell is made up of a 9T-FinFET design. The cell incorporates nine transistors, rather than the conventional SRAM's six-transistor structure, intended to significantly improve the stability and efficiency of the SRAM cell. The Figure represents the proposed 9T SRAM cell, featuring three pass gate (PM) transistors and six access (NM) transistors, interconnected with the supply voltage Vdd.

The SRAM cell is explained in two segments- upper and lower circuits. In the upper circuit, PM1 functions as the pass gate transistor, linking the storage node with bit line (BL) in addition to managing data flow during read and write operations. Acting as a switch, PM2 establishes a connection among the word line (WL), and the storage node, facilitating data transfer between the storage node and the bit line. In write operations, PM3, linked between the storage node and the ground (GND), aids in voltage reduction to store a logic 0.

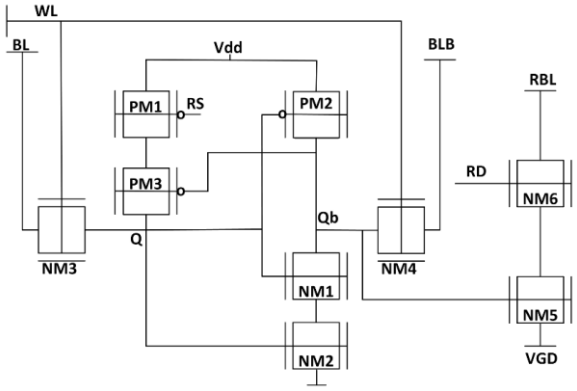

Fig. 2. Proposed FinFET based 9T SRAM cell

Transitioning to the lower circuit, NM3, tied to the bit line (BL), bolsters the SRAM cell's stability in read and write operations. NM1, serving as the access transistor, connects the storage and ground (VGD) nodes, governing data access from the storage nodule to the bit line in read operations. NM2, linked to the ground (VGD), further amplifies the SRAM cell's stability. NM4, affiliated with the power supply (VDD), elevates the storage node's voltage during write operations to store a logic 1. Additionally, NM6, connected to the RBL (read bit line), enables enhanced access and stability in read and write operations. NM5, tied to the virtual ground (VGD), contributes to augmented SRAM cell access and stability.

These specific transistor interconnections in 9T optimize the performance, culminating in heightened stability, diminished leakage current, with enhanced power efficiency in comparison to the conventional 6T SRAM cell.

Working of the Proposed 9T SRAM Cell

3.1 Read Operation

The proposed 9T SRAM cell scheme executes a read operation that eliminates the need for a pre-charge operation. Moreover, it has the capability to write both '0' and '1' on the bit line (BL), which amplifiers may distinguish. At the beginning of a read operation, the write signal (WR) and control signal (CTRL) are both maintained at a low voltage (logic level 0), while the read signal (RD) is raised to a higher voltage (logic level 1), as depicted in Figure. Upon application of the RD signal, the access transistors NM5 and NM6 are activated. NM5, linked to BL, and NM6, connected to the complementary BL (BLB), enable the retrieval of data stored within the cell. In the process of retrieving stored data, the voltage on BL is detected and amplified. If the stored value corresponds to logic 1, a voltage disparity between BL and the ground emerges, leading to a higher voltage on the bit line. Conversely, if the stored value represents a logic 0, the voltage difference is minimal, resulting in a relatively low bit line voltage. Subsequently, the sensed voltage on the bit line (BL) is scrutinized and interpreted by sense amplifiers to ascertain the logic level of the stored data.

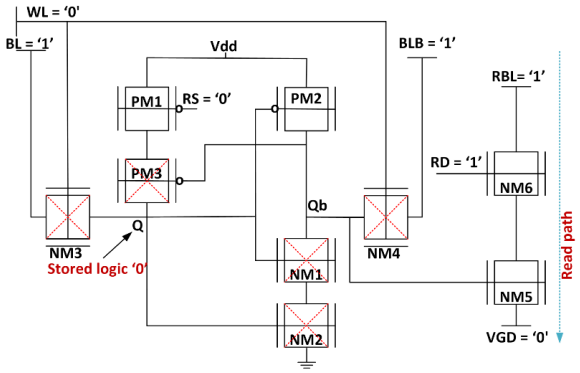

Fig. 3. a) Read Mode

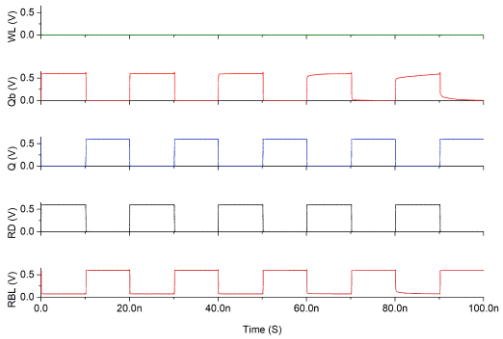

Fig. 3. b) Read Waveform

3.2 Write Operation

In the Write operation, 9T SRAM cell involves the process of storing data, either a logic '0' or '1', into the memory cell. It entails changing the voltage levels of nodes within the cell to represent the desired data value. The write operation in the cell confirms retention of the intended data until it is explicitly overwritten during a subsequent read or write operation. The cell employs a specific configuration to optimize power consumption and data stability during write operation. The access transistor NM4 is positioned in the feedback path, and NM3 is in contact with the bit line (BL) for storing the data, allowing the charging or discharging of only one capacitance (BL). This leads to a substantial decrease in dynamic power dissipation, accompanied by enhanced data as depicted in Figures 5a and 5b. Furthermore, both write access transistors of the 9T SRAM are controlled by a write signal (WL) connected to the bit line beside its complement (BLB). Specifically, one write access transistor (NM3) is linked to BL and controlled by the WL signal, while one read and hold access transistor (NM4) is managed through a control signal. The lower sub-circuit encompasses the BL access transistor (NM5) and the BLB access transistor (NM6), both governed by the read signal (RD). During a write operation, the WR signal is maintained at a high voltage (logic level 1), whereas the RD and CTRL signals are kept at a low voltage (logic level 0). Consequently, the access transistors NM2 and NM6 are deactivated, and the write access transistor NM3 is activated. To write logic 1 to Node 1, the BL is charged, forcing logic 1 into the node through NM3. This action activates transistor NM2, driving logic 0 into Node 2. As a result, transistor PM1 turns on, causing the discharge of BL. Thus, the write operation involves bit line charging as well as discharging, resulting in efficient power utilization.

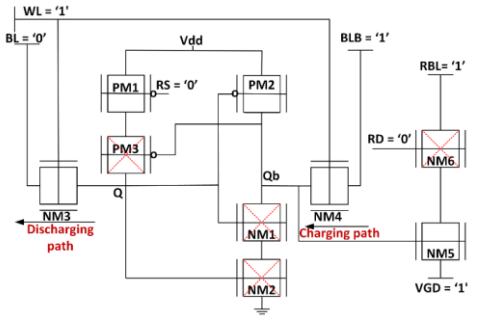

Fig. 4. a) Write '0' mode

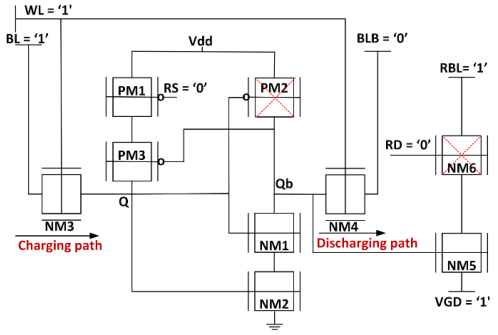

Fig. 4. b) Write '1' mode

The Figure shows a write waveform with signals integrated into the write operation of SRAM cells. Initially, WL is activated to a high voltage level allowing data transfer. The Qb and Q signals serve as the complement and actual data bits, delivering the input values for the write operation. The Bit Line Complement (BLB) signal acts in a cycle with the bit line (BL) signal to carry the data for writing in the SRAM cell, and the voltage level of BL resembles the targeted logic value. To write data, logic 1, the BL signal is charged to a higher voltage (VDD), while for logic 0, it discharges to a lower voltage level (GND). The synchronization of these signals ensures the accurate execution of the write operation.

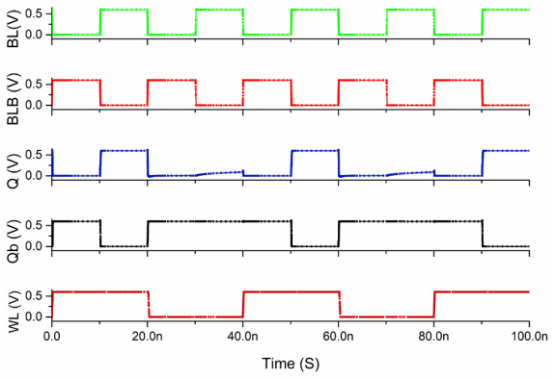

Fig. 4. c) Write Waveform

3.3 Hold Operation

The proposed 9T SRAM cell operates in hold mode like a 6T cell allowing WL and RWL signals at logic '0' and disconnecting the storage nodes from the BL. At storage node Qb, logic '0' is a presumption, which activates the PM3 transistor and keeps logic '1' at node Q. Then transistor PM3 is turned on at node QB to cut off the storage node power supply at Q, node Qb is presumed at logic '1'. The ground is connected to bit-line BL. Enhancing the NM1 transistor responsible for discharging the remaining voltage will enable you to attain the smallest effective off-state resistance between VGD and node Q.

TABLE I. 9T SRAM CONTROL SIGNALS

Mode	**Control signals**						
	RS	***BL***	***BLB***	***WL***	***RBL***	***RWL***	***VGD***
Read	0	0	1	0	1	1	0
Write 0	0	0	1	1	1	0	1
Write 1	0	1	0	1	1	0	1
Hold	0	0	1	0	1	0	1

IV.Simulation Results and Discussion

The results obtained from the proposed 9T SRAM cells include different parameters like power, Stability, speed and energy. Comparing the performance of the 9T SRAM cells with the performance of conventional 6T, TA8T, 11T, and D2p11T, gives insights into proposed SRAM benefits over other SRAM cells.

4.1 Read/Write Power Dissipation

In FinFET SRAM cells for IoT applications, power dissipation becomes a significant concern. In high-performance circuitry, the significance of dynamic power consumption becomes evident, mainly due to its correlation with the elongated interconnects that impose a substantial capacitive load on the signal path within the SRAM cell. The differential activity involved in reading and writing within the SRAM cell magnifies the capacitance of the bit-lines, resulting in notable power dissipation during these operations. The mean power dissipation in read activities is noticeable in the proposed 9T cell as well as other SRAM FinFET cells, where the Q and QB hold logic '0' and logic '1' states. Additionally, write power dissipation is observable across a voltage from 0.3 V to 0.6 V. Figures illustrate the computed values for dissipation of power in both write and read operations.

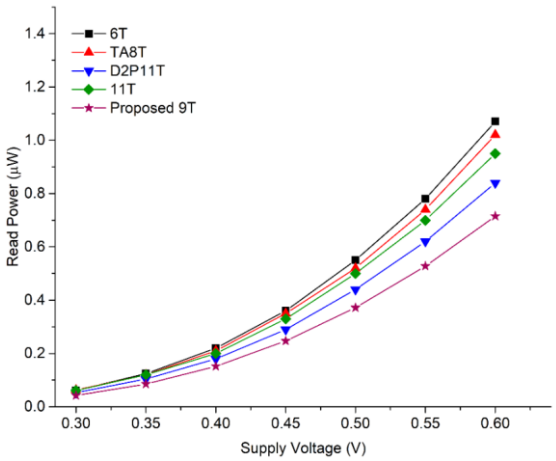

Fig. 5. a) Read Power

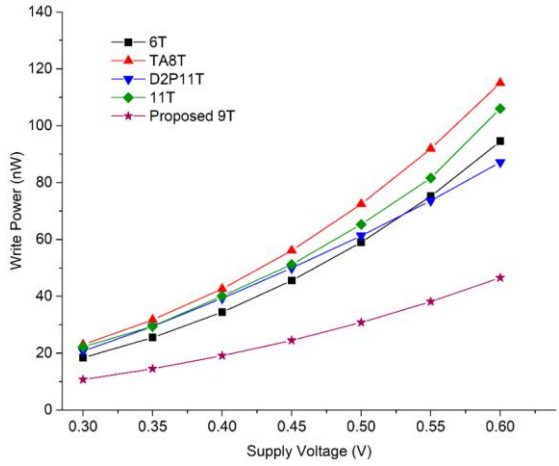

Fig. 5. b) Write Power

The power dissipation of the cell increases as the supply voltage is raised. Simulation results for various types of SRAM cells indicate read power dissipation in µW and write power dissipation in nW. The results reveal that the highest read power dissipation (1.07 µW) is observed in the 6T cell, while the highest write power dissipation (115 nW) is observed in the TA8T cell. Models with lower read power dissipation, such as the 11T and D2P11T cells, perform better than the TA8T, which outperforms the 6T in terms of power dissipation during read operations. However, during write operations, the 6T cell, which has lower power dissipation, outperforms the TA8T and 11T cells.

Because of the quadratic link of supply voltage with power dissipation, there is a rise in read power dissipation while the supply voltage of 9T SRAM rises from 0.3 to 0.6 V. Because of its single-ended read structure, the read power of 9T decreases than that of the 6T, TA8T, 11T, and D2P11T cells. Similarly, write power dissipation decreases in 9T relative to the 6T, TA8T, 11T, and D2P11T SRAM cells because it takes a greater resistive route, which decreases the current in the cell and minimizes write power dissipation.

Notably, the proposed 9T exhibits the top performance among the considered cells with the lowest power dissipation in both read (0.715 µW) and write (46.5 nW) operations.

4.2 Read Current

Read current is accountable for a fast read operation in FinFET SRAM cell. As voltage rises from 0.3V to 0.6V read current also increases. Read current eliminates the capacitive distortion caused by bit-lines without passing through storage nodes. Thus, it is an imperative factor in the stability of SRAM cells. In the read operation, read current passes through the access transistors to connect bit lines. A comparison of read currents in MC simulation displays that the suggested 9T SRAM cell gives the highest current (9.32 µA) than current in 6T, TA8T, 11T, and D2P11T SRAM cells as shown in the Figure. However, there is a slight difference in their performance with increasing supply voltage from 0.3-0.6V.

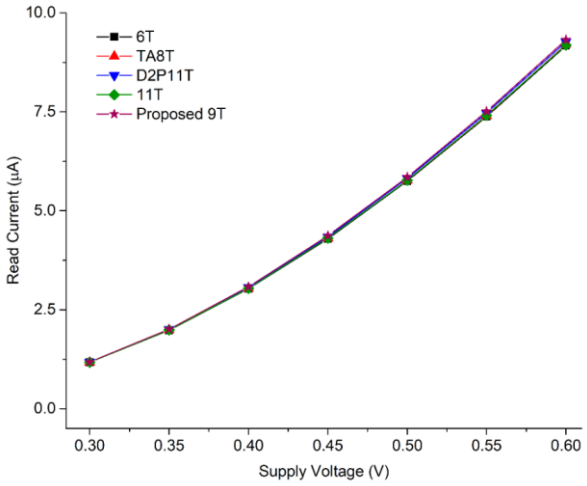

Fig. 6. Read Current

4.3 Variability Analysis

Variability in the read current of a 9T FinFET SRAM cell refers to the extent of uncertainty in read current values during read operations [38]. This variability arises from multiple sources, including process variations, fluctuations in temperature or voltage variations. Variability is important to ensure that the SRAM cell performs consistently under different conditions.

4.3.1 Read Current Variability Analysis

The variability in current for the proposed 9T SRAM is observed at a temperature of 27°C, considering supply voltage variations with a sigma value of 3. Specifically, supply voltages of 0.3V, 0.4V, and 0.6V are applied to the circuit. The Figure illustrates a Monte Carlo simulation comprising 4000 instances for varying supply voltage (Vdd). The circuit demonstrates moderate read current variability (σ/mean) at 0.4V and the highest variability at a supply voltage of 0.3V. However, at 0.6V, the circuit exhibits the lowest variability of 0.025, indicating enhanced stability at this voltage.

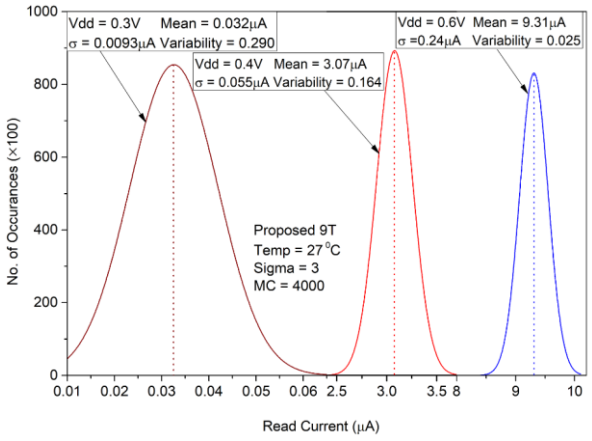

Fig. 7. Read Current Variability for Supply Voltage Variation

The results reveal that lower supply voltage leads to reduced current but higher variability. When the supply voltage rises, the variability in read current diminishes. Specifically, at 0.4V, the variability decreases to 0.164, and at 0.6V, it drops significantly to 0.025. Consequently, lower variability in the proposed SRAM cells signifies consistency and predictability in reading current behavior. It shows superior stability as well as reliability of proposed 9T SRAM cells, especially at the higher supply voltage of 0.6V.

However, at 0.3V of Vdd, the 9T SRAM cell reveals a higher variability of 0.290 in the read current than conventional 6T. This is due to the existence of added transistors in the 9T SRAM cell design, which introduces certain challenges that can impact read current variability and power static noise margin (SNM). The Figure

illustrates simulation results, showing the difference between the performance of 6T and the proposed 9T SRAM cells. Consequently, the 9T requires a higher supply voltage for achieving better stability.

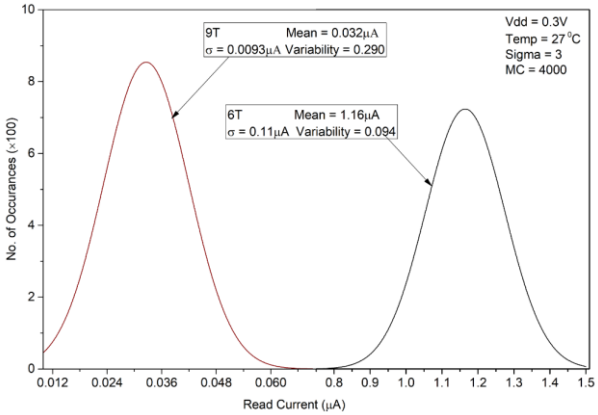

Fig. 8. Comparison of Read Current Variability in proposed 9T and conventional 6T

4.3.2 Read Power Variability Analysis

The read power variability of SRAM cells is estimated in read operation as logic '0' and logic '1' are retained at the SRAM cell's storage nodes Q and QB, respectively. To achieve greater stability, the read power dissipation across different SRAM cells is measured at 0.6V. The figure shows the variability in MC simulation results for the designed 9T SRAM cell in contrast to the 6T, TA8T, 11T, and D2P11T cells. Among these options, the 9T SRAM cell with the lowest power dissipation demonstrates a variability of 0.077, which is similar to the variability of the 6T SRAM. The variability of the other SRAM cells is also relatively close to that of the proposed 9T SRAM, although with slight differences. However, the advantage of lower power dissipation increases the reliability of the 9T SRAM over the other types.

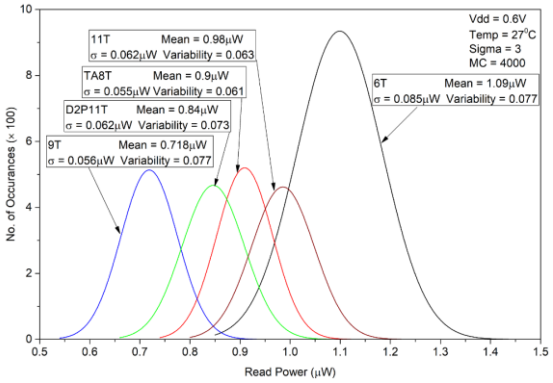

Fig. 9. Comparison of Read Power Variability for SRAM cells

Furthermore, the performance of the 9T SRAM at 0.6V is superior, exhibiting lower variability compared to the lower supply voltage of 0.4V. Both the mean read power and the σ value increase with the supply voltage, contributing to the decrease in the variability of the 9T SRAM. As a result, it exhibits enhanced performance at 0.6V.

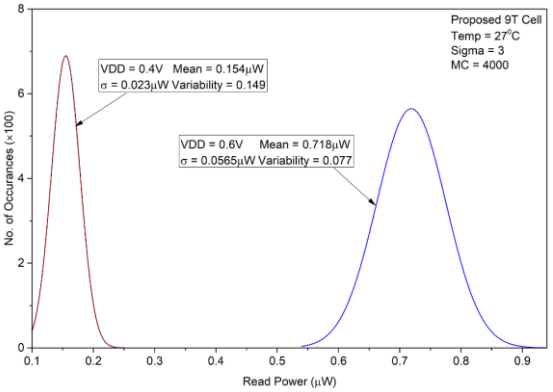

Fig. 10. Comparison of Read Power Variability for Supply Voltage Deviation

4.4 Read/ Write Stability

The stability of SRAM cells during read and write operations hinges on SNM (static noise margin), which represents the least DC noise voltage essential to alter the bit value under processing. The estimation of SNM in

SRAM cells is accomplished by employing the butterfly curve technique, wherein the size of the largest square enclosed within the smaller lobe of the butterfly curve is utilized. [17].

4.4.1 RSNM

Read stability, write stability, and hold stability are assessed by the static noise margin values RSNM, WSNM, and HSNM. With the rising supply voltage from 0.3V to 0.6V, the RSNM in the SRAM cell also rises. The read stability of proposed 9T cell (206 mV) is prominent owing to its read decoupled structure, which effectively divides the BL from the storage node during read operations. The Figure highlights the increased RSNM in the proposed 9T SRAM cell associated to the 6T (117 mV), 11T (143 mV), TA8T (142 mV), and D2P11T (154 mV) SRAM cells. Additionally, the butterfly curve is considered for assessing the stability of SRAM cells at a 0.6V supply voltage.

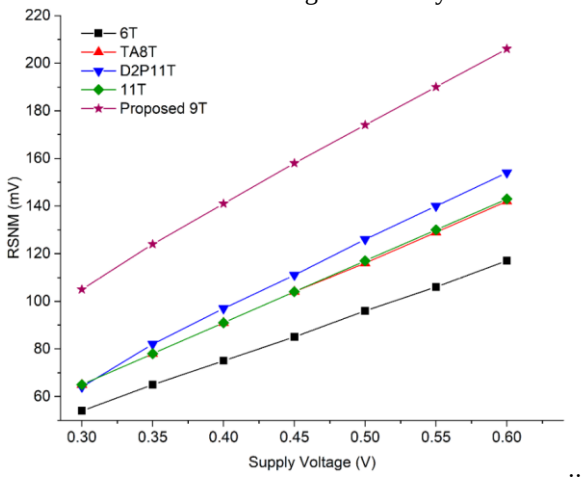

Fig. 11. a) RSNM for different SRAM cells

RSNM effectively demonstrates the impact of process variations on read stability, as illustrated by MC simulations in the Figure. The RSNM variability is minimized because of its read decoupling design produced by the transistors in the 9T SRAM eliminates the development of a voltage divider as well as prevents a positive voltage at the node storing logic '0'. The 9T SRAM cell exhibits the highest RSNM value using an inverter with a Schmitt trigger.

4.4.2 WSNM

The write stability, WSNM, is evaluated using the bit-line sweep technique [39]. The proposed 9T SRAM outperforms in write stability due to separate write and read operations. Meanwhile, the stability of 6T depends on the pull and cell ratio of access transistors.

Write stability of the proposed 9T SRAM cells demonstrates superiority over TA8T, as depicted in the Figure. Furthermore, its performance is enhanced compared to 6T and D2P11T at higher voltages. Thus, better stability is observed for the 9T SRAM than TA8T during write operations.

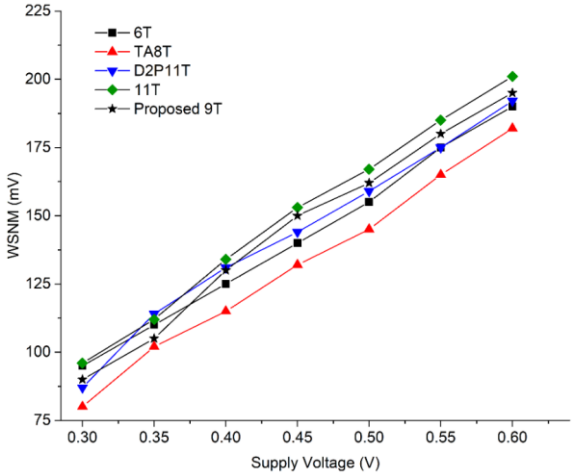

Fig. 11. b) WSNM for different SRAM cells

4.4.3 HSNM

HSNM measures the stability of the hold operation, showcasing the capacity to reliably retain stored data [40]. During this phase, the SRAM cell shows minimized leakage current through voltage scaling. To achieve better performance, the data retention voltage is set lower than the supply voltage [41]. This nominal voltage at the storage node, referred to as HSNM, is the threshold required to disrupt stored data in a hold state. The 9T SRAM achieves nearly equal HSNM compared to other SRAM cells, enhancing data retention. It ensures robust hold stability, thereby maintaining data integrity.

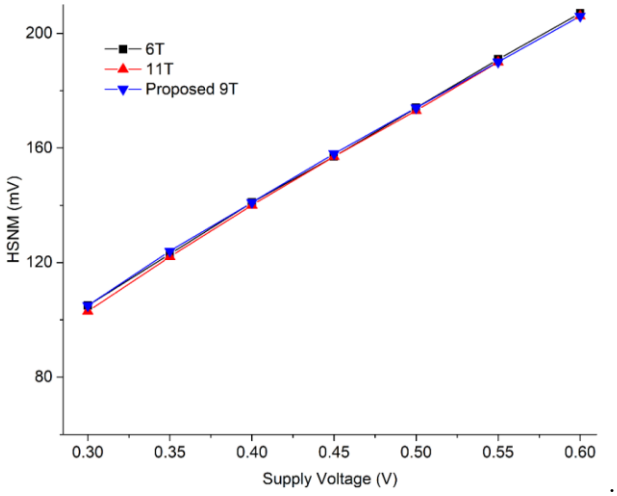

Fig. 11. c) HSNM for different SRAM cells

Variability of HSNM

Comparing SRAM cells at Vdd of 0.6V, a temperature of 27°C, and a sigma of 3 over 2000 samples, Monte Carlo simulations provide the variability of HSNM. The SRAM cells exhibit enhanced HSNM with cross-coupled inverter pairs forming a positive feedback loop during the hold state [42]. Consequently, the proposed 9T SRAM cells, with optimized feedback strength, enhance HSNM and effectively utilize both low and high-voltage transistors in the bit cell structure.

The figure shows the variability of HSNM in the 9T SRAM (0.0017) is lower than that of the D2P11T (0.0300) and 6T (0.0018) SRAM cells, showcasing superior hold stability.

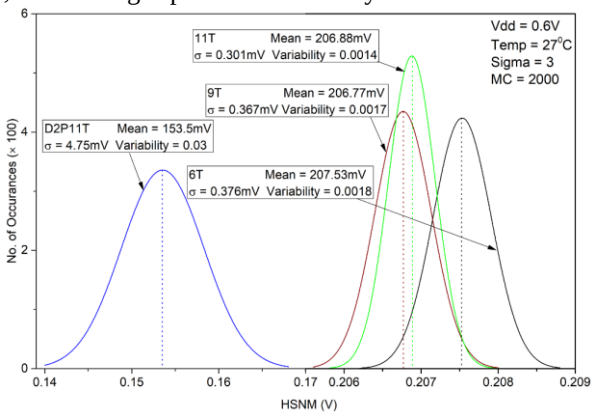

Fig. 12. Variability in HSNM for different SRAM cells

4.5 Speed

4.5.1 Read/Write Access Time

The speed of SRAM cells is referred to as read and write access time. High-speed SRAM consumes low access time denoted by the time required to acquire 50% above the supply voltage at the signal to create a difference in voltage across two bit-lines [17]. The higher read current across the read bit-line signifies a reduced time for read operations.

The read access time at different supply voltages is obtained with MC simulation as shown in the Figure. The results show the lowest read access time (25.97 pS) in the proposed 9T SRAM while D2p11T takes slightly more (28.57 pS) read access time. The speed of the proposed 9T is thus enhanced during a read operation as compared to 6T, TA8T, 11 T, and D2P11T SRAM. Furthermore, the proposed 9T SRAM cell obtains the lowest access time value of 49.98 pS for write operation. However, 6T performs better in write operations with less access time (60.64 pS) as compared to D2P11T which consumes the highest time (84.55 pS). Other SRAM cells perform moderately including TA8T and 11T cells. The write access transistors taking lower charging and discharging time plays an important role in reducing access time in the read and write operation of 9T SRAM cells.

The simulation results present enhanced speed of the proposed 9T SRAM cells in both write and read operations consuming less access time.

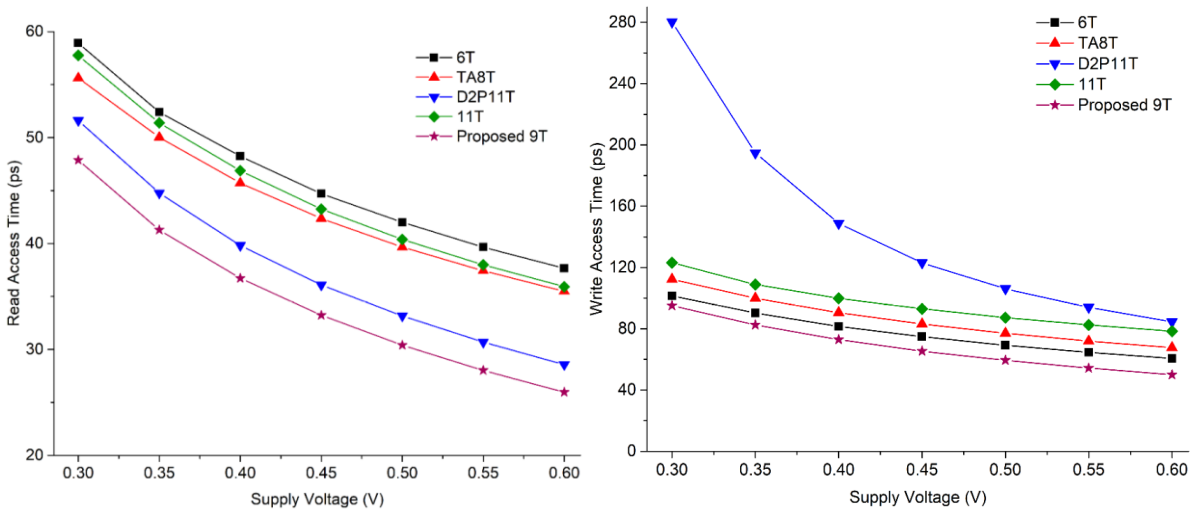

Fig. 13. a) Read Access Time for different SRAM cells b) Write Access Time for different SRAM cells

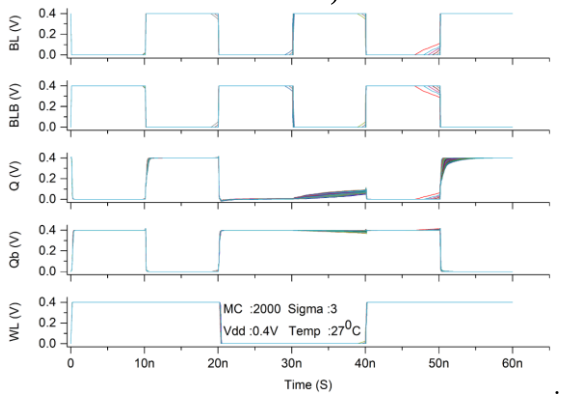

Fig. 13. c) Signal Voltage Vs Access Time

4.5.2 Power-Delay Product

PDP or Power-Delay Product is indicated as the product of the power dissipation and the delay that evaluates the energy efficiency of the SRAM cell of the circuit. In the SRAM cell, the read and write power dissipation of the cell is evaluated and the time taken for these operations is considered as the delay. A lower PDP value in energy-efficient circuits indicates less energy consumption during a given time in IoT applications. PDP is measured in aJ (attojoules), which is a very small unit of energy. While optimizing SRAM cells, the PDP value needs to achieve better energy efficiency without forfeiting its performance.

Read PDP of various SRAM cells is evaluated at different voltages as presented in the Figure. The MC simulation results of read PDP show conventional 6T with the highest PDP (40.29 aJ) while proposed 9T with significantly low PDP (18.56 aJ) is the best performing among 6T, 11T (34.12 aJ), TA8T (36.18 aJ) and D2P11T (23.99 aJ) SRAM during read operation. However, in a write operation, 11T shows higher PDP as compared to TA8T and D2P11T. 6T is better performing in write operation (5.7 aJ PDP), but 9T SRAM shows the lowest PDP of 2.3 aJ as compared to all other SRAM cells. Thus, 9T proves greater energy-efficient performance. The lowest read PDP and write PDP values of proposed 9T enhance the energy efficiency of SRAM cells in read/ write operations.

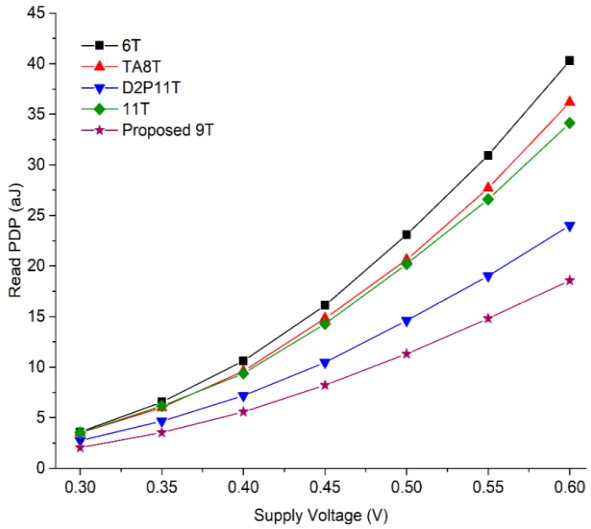

Fig. 14. a) Read PDP

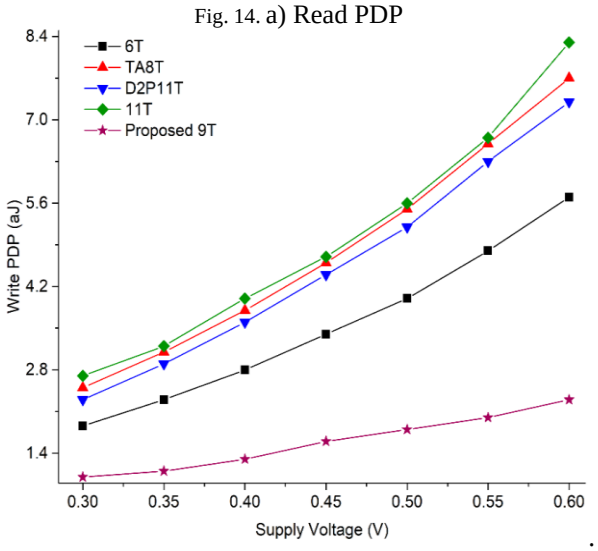

Fig. 14. b) Write PDP

4.6 Monte Carlo Simulation

A computational Monte Carlo simulation technique is employed to model and analyze the behavior of complex systems under uncertain or variable conditions. It entails the execution of multiple simulations with randomly sampled input parameters to accommodate factors like variability, noise, and other sources of uncertainty. This methodology facilitates a more comprehensive grasp of the system's performance and conduct across a spectrum of potential scenarios. In the scope of the study, the evaluation of a 9T FinFET SRAM cell circuit is conducted through Monte Carlo simulation, encompassing a range of essential parameters and metrics under real-world conditions. This analysis encompasses aspects such as static noise margin during read/write operations in 9T SRAM cells, power dissipation, as well as read current and the variability of different SRAM cell configurations including the conventional 6T, TA8T, 11T, and D2p11T, all evaluated under diverse conditions. Monte Carlo simulation offers a comprehensive assessment of the SRAM cell's performance by factoring in uncertainties that affect read/write access times, power consumption, stability metrics, and energy efficiency. This approach facilitates precise design decisions to ensure the SRAM cell's reliability and functionality across a wide array of practical scenarios.

4.6.1 Butterfly curve

The curve represents the voltage of complementary bit line (Qb) and bit line (Q) during a read/write operation, illustrating the voltage transitions as the cell switches between logic states, '0' and '1'. SRAM cell reliably differentiates between these states and provides stability under varying conditions.

The Figure shows the butterfly curve for the proposed 9T SRAM in relation to the 6T, 11T, TA8T and D2P11T configurations. The square represents the most reliable and stable region [40]. A wider square indicates a larger voltage margin between the '0' and '1' logic levels. In Figure, 9T shows a large square as compared to 6T, 11T, TA8T and D2P11T. It signifies enhanced robustness of 9T SRAM against noise and process variations with a more reliable operation and enhanced tolerance to external factors.

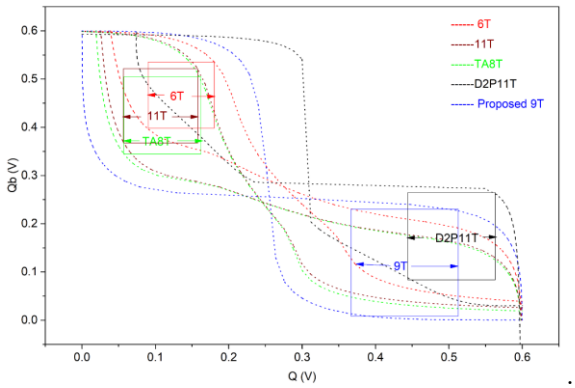

Fig. 15. Butterfly Curve for SRAM cells

The overall simulation results of the proposed 9T SRAM cell are intended to evaluate various characteristics of the 9T FinFET cell in comparison to existing structures. This evaluation encompasses power dissipation, variability, read current, access time, and the stability of write and read operations. Monte Carlo simulation is conducted to showcase the performance of the proposed 9T cell and to compare it with the conventional 6T, TA8T, 11T, and D2p11T configurations. The study focuses on Monte Carlo simulations for write, read, and hold operations in SRAM, employing 4000 samples to assess the defined factors at a temperature of 27 ^{0}C and supply voltage of 0.6V. FinFET technology is employed in the compared bit cells due to its superior channel control [39]. In the simulation setting, we used models with minimal standby power with great performance that are available at current technological nodes. The proposed 9T cell employs loop FinFET transistors along with access transistors to improve drive strength during write operations, without relying on write assist techniques [43]. The study performs simulations of the proposed bit cells under varying supply voltage conditions using the 20 nm technology. Additionally, the operating margin of SRAM cell during hold, write, and read modes, along with power calculations, has been determined. The speed of the proposed technique in terms of access time is further evaluated with energy consumption, while the static noise margin demonstrates the SRAM cell's stability.

TABLE II. COMPARISON OF SRAM PARAMETERS BETWEEN EXISTING WITH PROPOSED 9T CELL

SRAM / Parameters		Conv. 6T	TA8T	11T	D2p11T	Proposed 9T Cell
Power	Read Power (µW)	1.07	1.02	0.95	0.84	0.715
	Write Power (nW)	94.49	115	106	87.1	46.5
	Read Current (µA)	9.17	9.2	9.19	9.27	9.32
Stability	RSNM (mV)	117	142	143	154	206
	WSNM (mV)	190	182	201	225	195
Speed	Read Access time (pS)	37.66	35.48	35.92	28.57	25.97
	Write Access time (pS)	60.64	67.67	78.4	84.55	49.98
Energy	Read Energy (aJ)	40.29	36.18	34.12	23.99	18.56
	Write Energy (aJ)	5.7	7.7	8.3	7.3	2.3
Vdd	Supply Voltage (V)	0.6	0.6	0.6	0.6	0.6

From the obtained outcomes, it can be illustrated that the proposed 9T cell reduces read power dissipation (0.715 µW) by factors of 1.50, 1.42, 1.33, and 1.17 when compared to 6T, TA8T, 11T, and D2P11T, respectively. Similarly, the write operation with low power dissipation (46.5 µW) is reduced by factors of 2.03, 2.47, 2.27, and 1.87, enhancing the SRAM cell's performance. Furthermore, the read current of proposed 9T cell (9.32 µA) slightly increases by factors of 1.016, 1.013, 1.014, and 1.005 compared to 6T, TA8T, 11T, and D2P11T, respectively, which benefits the circuit operation. Overall, the advantages of proposed 9T SRAM over other configurations lie in its lower power dissipation and higher read current values.

The circuit stability is assessed based on Static Noise Margins (RSNM, WSNM, and HSNM) values. The results reveal an increase in RSNM for proposed 9T cell (206 mV) by factors of 1.76, 1.45, 1.44, and 1.33 compared to 6T, TA8T, 11T, and D2P11T, respectively. Additionally, the WSNM of proposed 9T (195 mV) is enhanced by

factors of 1.03 and 1.07 when compared to 6T and TA8T, respectively, leading to an overall improvement in the SRAM stability.

The speed of SRAM cells is contingent on their access time, where low access time is imperative for swift memory operations. After comparison with 6T, TA8T, 11T, and D2P11T, the proposed 9T cell demonstrates a reduced read access time (25.97 pS) by factors of 1.45, 1.36, 1.38, and 1.1, respectively. Additionally, the write access time (49.98 pS) is diminished by factors of 1.21, 1.35, 1.56, and 1.69. Consequently, proposed 9T cell emerges as a faster SRAM configuration, reinforcing the overall system speed.

The energy consumption in the 9T cell is curtailed to 18.56 aJ for read and 2.3 aJ for write operations, resulting in reductions of 2.17, 1.94, 1.83, and 1.29 for write, and 2.47, 3.34, 3.60, and 3.17 for read operations, relative to 6T, TA8T, 11T, and D2P11T SRAM cells. Thus, the proposed 9T SRAM cell offers diminished energy consumption, augmenting the energy efficiency of the SRAM cells.

V.Conclusion

The proposed ultra-low power SRAM with a 9T FinFET structure demonstrates enhanced performance for IoT devices. Utilizing the Monte Carlo Simulation technique, a robust assessment of 9T SRAM performance is conducted, considering process variations, temperature fluctuations, and other uncertainties inherent in real-world conditions. This approach facilitates accurate parameter estimation, bolstering the reliability and predictive capability of performance evaluations. The 9T SRAM cells showcase their potential through superior energy efficiency and speed, with a notable enhancement in read stability at a 0.6V supply voltage. Comparative results reveal reduced power dissipation, underscoring the potential of 9T SRAM. The suggested circuit achieves higher energy efficiency by reducing the access time of each operation, thereby showcasing significant speed improvements facilitated by FinFET technology. The study concludes that the overall performance of SRAM is raised with the 9T FinFET cell, resulting in reduced power consumption, increased speed, enhanced energy efficiency, and improved stability during reading and writing operations. This cell emerges as a superior solution for compact SRAM cells than conventional 6T, 8T, as well as 11T cells. Ultimately, the ultra-low power 9T SRAM achieves significant improvements across key SRAM parameters.

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