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Analysis Of P-N Junction Length of Drain and Source in MOSFET Transistor Through TCAD Simulation

Abstract: - This paper delves into the convergence of mathematical and computer science principles within the realm of electronics engineering, particularly focusing on device-level transistor restructuring. A pressing challenge confronting the semiconductor sector is the persistent escalation of leakage current alongside technological advancements. At the heart of any chip or semiconductor device lies the transistor, serving as its fundamental building block. Among the various forms of leakage current, subthreshold leakage stands out as a dominant component in transistors. Within this study, a systematic exploration of the numerical association governing the physical configuration of MOSFET and leakage amount specifically the subthreshold one is undertaken. One innovative algorithm is crafted to facilitate the automated tracking of transistor structures, laying the groundwork for subsequent analyses. The simulation framework is meticulously constructed by leveraging mathematical formulations derived from the algorithmic outputs. Remarkably, the results obtained from the simulation conducted through TCAD software exhibit a remarkable proximity to established mathematical models. Given the ubiquity of Complementary Metal Oxide Semiconductor (CMOS) technology in contemporary semiconductor fabrication, it serves as the cornerstone for the simulation endeavours herein.

Keywords: MOSFET, pn junction length, leakage current, nano, structural engineering.

I. INTRODUCTION

From the ubiquitous presence of chips in everyday electronics like computers and mobile phones to the intricate systems powering satellites, integrated circuits (ICs) stand as the backbone of modern electronic devices. At the core of these ICs lies the MOSFET, appearing as a fundamental building block. MOSFETs come in two primary types: NMOS (Negative MOSFET) where current flow is driven by electrons, and PMOS (Positive MOSFET) where it's propelled by holes. In many circuits, both NMOS and PMOS transistors are required, collectively referred to as CMOS (Complementary MOSFET) technology, which has become the prevailing standard in semiconductor fabrication due to its efficiency and simplicity compared to older technologies like BJT (Bipolar Junction Transistor) [1].

The relentless march of technology, as described by Moore's Law [2] and subsequent concepts like More-than-Moore (MtM) and More-Moore [3], has seen transistors shrink in size, leading to reductions in power consumption and area while improving performance. However, this downsizing has also led to an unwelcome increase in leakage current [4], particularly pronounced in transistors below 65 nm [5]. With each successive generation of microprocessors [4], leakage current tends to escalate significantly. This phenomenon poses a critical challenge for maintaining data stability in CMOS memory circuits, necessitating a thorough analysis of parameters like static noise margin (SNM) [6].

In the realm of nanometer-scale transistors, the discrete effects of gate voltage and drain voltage give way to their mutual influence, highlighting phenomena like gate-induced drain leakage (GIDL) [7] as significant concerns. Various circuit-level techniques [8] have been developed to mitigate leakage current, including transistor stacking and innovative cache designs [9]. Additionally, the optimization of SRAM memory circuits [10], [11] plays a pivotal role in leakage reduction and overall circuit performance.

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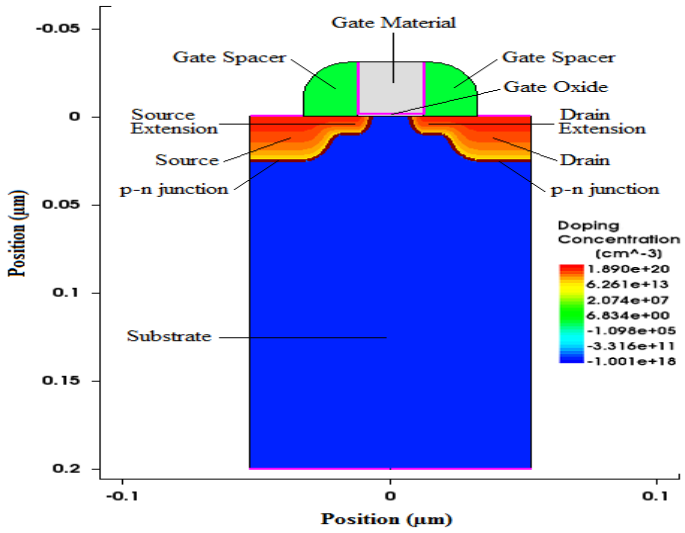


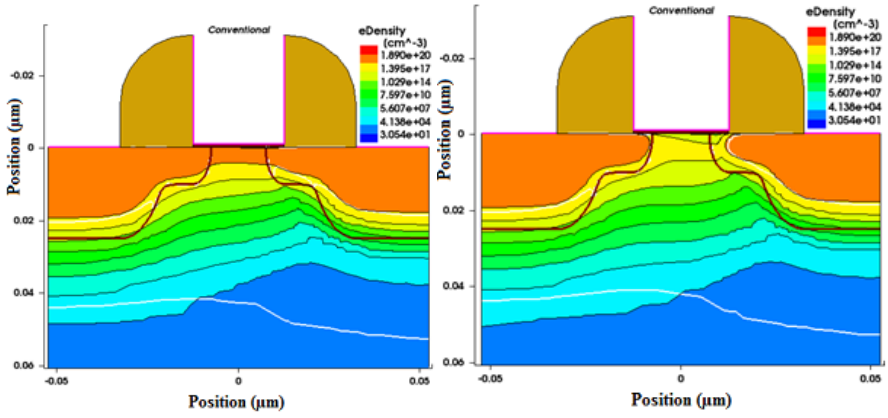
Figure 1: Representation of a Conventional NMOS Configuration at 20 nm Generation. Highlighted elements include pink-colored lines for contact, delineated brown-colored lines of p-n junction, and demonstrated concentration of doping.

Among the myriad forms of leakage currents [12], [13], subthreshold leakage [13], [14]emerges as a dominant concern [15], [16]. This paper addresses this issue by exploring modifications to the p-n junction structure to model and mitigate subthreshold leakage current. The construction and operation of NMOS transistors are detailed, emphasizing the pivotal role of gate voltage in controlling current flow and the onset of subthreshold leakage.

The subsequent sections unfold as given: part 2 dowries the methodology engaged, while part 3 introduces the proposed algorithm. Results and discussions are provided in Section 4, with Section 5 offering a summary and conclusion.

II. METHODOLOGY

The methodology employed in this study utilized a 20 nm NMOS setup [17]. The dimensional parameters were drawn from the 2011 version of ITRS [18]. Implementation tasks were conducted using the TCAD toolkit [19]. Figure 1 illustrates the physical layout of nMOS, while the very next two figures depict the concentration of electrons and current, separately, of the construction of Figure 1.

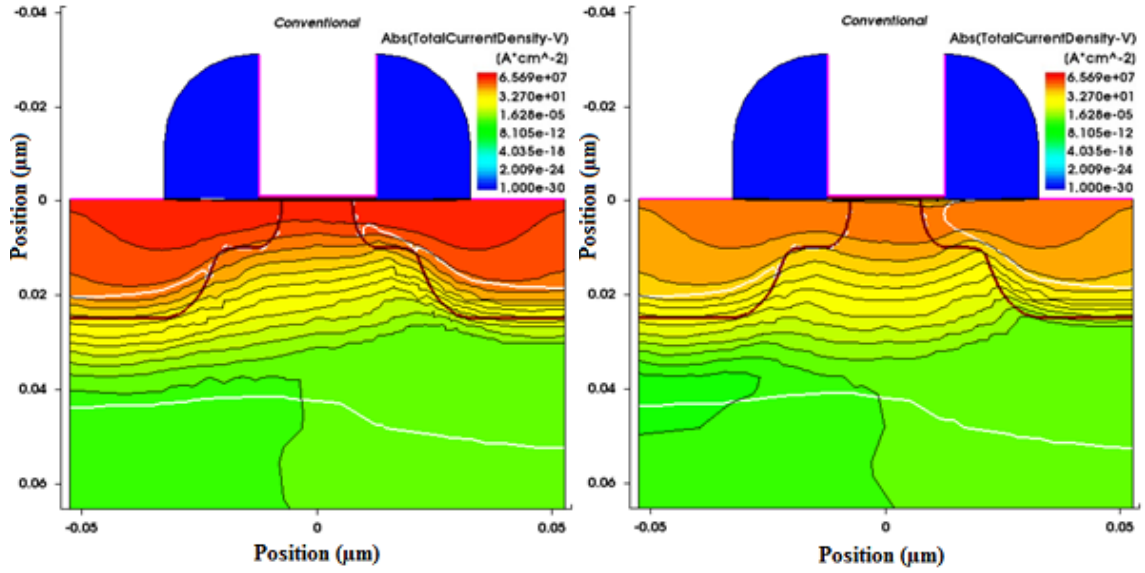


(a) (b)

Figure 2: (a) Spatial sharing of Density of Electron under conditions of matched gate and drain voltages (VDD), indicating transistor activation (ON state). (b) Spatial Distribution of Electron Density under conditions of zero gate voltage and matched drain voltage (VDD), illustrating transistor deactivation (OFF state).

Figure 2 delineates the sharing of electron density within the transistor. As electrons constitute the sole charge carriers facilitating current flow in NMOS, Figure 2 provides insights into the locations responsible for both ON and OFF currents. Subfigure 2(a) portrays the ON situation, where V_{Drain} as well as V_{Gate} are supplied with VDD, 0.8 V following ITRS recommendations [18] for 20-nanometer bulk technology. Notably, the orange band, signifying the maximum concentration of electrons, traverses drain-substrate and source-substrate junctions solely in the top halves of the extensions. Conversely, Subfigure 2(b) illustrates the OFF situation, characterized by a 0V as V_{Gate} and VDD as V_{Drain}. Here, the yellow band denotes the leakage current path, spanning the entirety of the extension part of the source region and a significant part of the extension of the drain region. Consequently, selectively covering portions of the p-n intersections, except for the top halves, could potentially mitigate leakage current without substantial ON current loss, pending experimental verification.

The absence of gate material in the University of California, Berkeley project's configuration [17], compensated by a direct supply of gate voltage through the pink contact line, had no discernible impact on simulation outcomes due to the inclusion of corresponding material work functions within the Sentaurus workbench [20].



(a) (b)

Figure 3: (a) Transistor in the ON state with equivalent drain and gate voltages set to VDD: current concentration. (b) Transistor in the OFF state with V_{Drain} set to full supply voltage and V_{Gate} set to 0V: Absolute value of total current density.

Figure 3(a) depicts the conducting state of the MOSFET, where both V_{Drain} and V_{Gate} are provided VDD voltage. The darkest red portion, indicating the maximum concentration of current, intersects p-n borders solely at the top halves of the extensions. Conversely, Figure 3(b) portrays the nonconducting state, characterized by a zero gate voltage and a drain voltage equivalent to VDD. Here, the darkest brown portion, conforming to the maximum leakage concentration, traverses the p-n intersections with a considerable part of both extensions. It underscores the potential efficacy of selectively covering part of the p-n intersections (excluding the uppermost regions) in significantly reducing leakage current without substantial ON current loss, although the precise association of p-n intersection distance and conducting (and nonconducting) current warrants further investigation, as such data were not encountered in the literature review.

To accurately measure the transistor's ON and OFF currents and discern the contribution of various sections of the p-n intersections, it is imperative to isolate additional parts of the p-n intersections. A straightforward approach involves inserting insulators at the p-n junctions, as previously proposed by [21], [22]. However, achieving it necessitates precise location of the p-n outline.

III. PROJECTED ALGORITHM

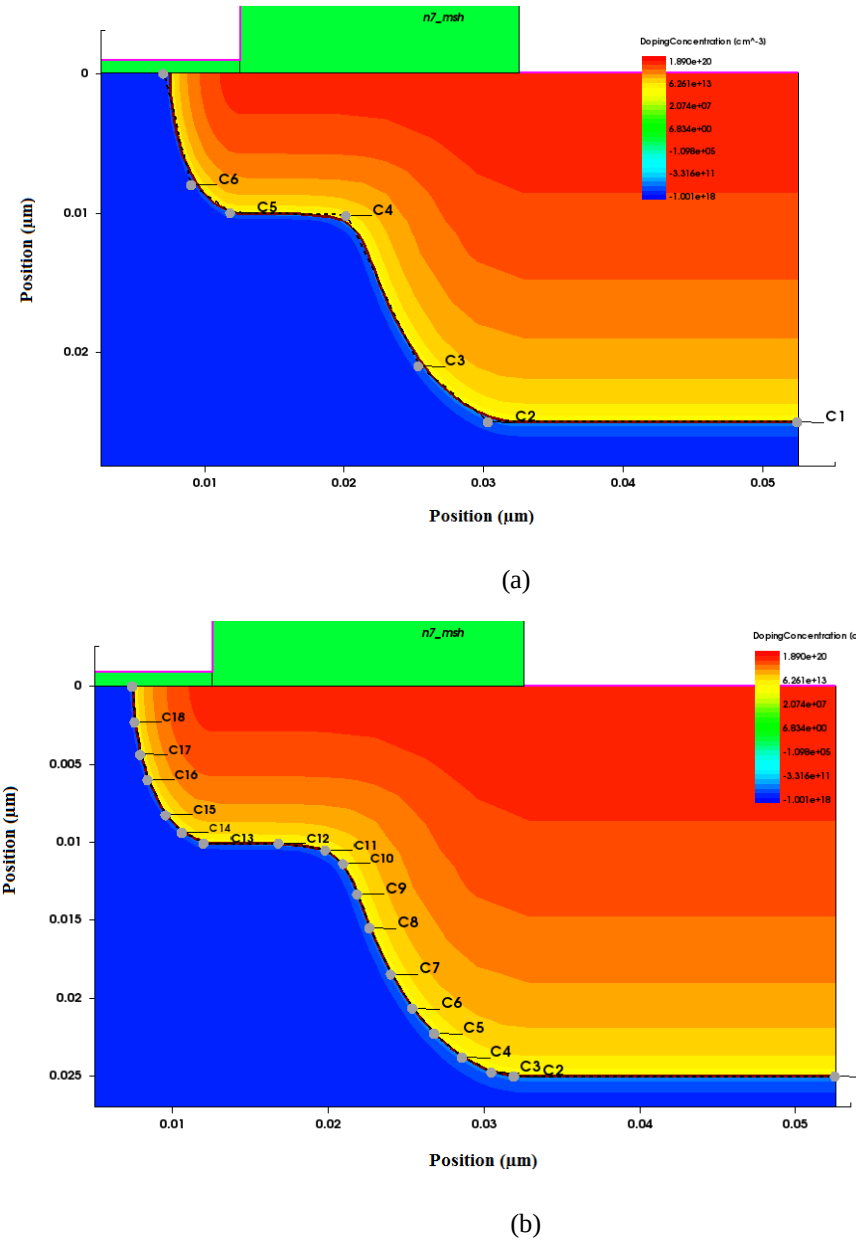


Figure 4: Enlarged depiction of drain section of NMOS focusing on tracking the coordinates. (a) Initial manual tracking process showing deviations such as points C2 and C4. (b) Repeat of the experiment adhering strictly to the algorithm, resulting in precise alignment.

Figure 4 illustrates the necessity of devising an algorithm. Given the symmetry of the left and right sides of the MOSFET and the inherent capability of TCAD software [19] to generate symmetrical components, only the coordinates of one p-n junction need to be determined, with the software generating the counterpart automatically. For the purposes of this experiment, focus was directed solely on the drain region. Initially, a manual approach was undertaken to ascertain the precise coordinates of the p-n junctions, as depicted in fig. number (a) of 4.

In fig. number (a) of 4, the lines were hand-collected in an attempt to delineate the p-n outline. However, this manual practice proved somewhat inadequate, as several instances occurred where the straight lines deviated from the actual one. Notably, point number 2 and 4 in Figure 4(a) lie outside the bounds. To address this limitation, an algorithm was developed. The results yielded by this algorithm, as depicted in Figure 4(b), demonstrate a marked improvement. Notably, in Figure 4(b), no portion of straight lines extends beyond the p-n bounds, indicating the algorithm's efficacy in overcoming the previous shortcomings.

A. Development of the Algorithm

1. Set the point of the right bottom corner as the initial point.

2. Also assign it for the terminating point of 1st line.

3. Progressively forward the termination towards left upper side, adhering to the original line, with the least movement. Halt movement if any irregularity is found.

4. Move back the least reverse one, to correct the irregularity.

5. Confirm this position as termination.

6. Verify whether this corresponds to the uppermost leftmost area. If affirmative, terminate.

7. If negative, designate this one as the beginning of the subsequent straight line.

8. Return to stage 2 for further iteration.

B. Determination of distance of the total junction

To comprehensively analyze the impact of every segment of the source-bulk and drain-bulk border, facilitates the subsequent division of the total length into discrete segments, such as 100 parts for detailed analysis. Leveraging the algorithmic output and insights from Figure 4(b), the coordinates of both endpoints of every line are gathered. Denoting these as (p, q) and (r, s) respectively for any given straight line, the length of the straight line can be computed using the distance formula.

$$l = \sqrt{(p-r)^2 + (q-s)^2} \quad (1)$$

By summing up, as depicted in Figure 4(b), the calculation is determined to be 0.059982539 micrometers.

C. Formulation of Equation for Every Line

With all points gathered, the formulation of equations for these lines proceeds.

$$m = \frac{y-b}{x-a} \quad (2)$$

Given coordinates (x, y) and (a, b) for the ends on a line, the slope (m) and the height at which the line crosses the y -axis (c) are computed.

$$c = y - mx \quad (3)$$

These parameters, from the above two equations, enable the derivation of the desired equation.

$$y = mx + c \quad (4)$$

D. Establishment of Path from line

Fig. 5 underscores the necessity of two side line equations for facilitating the insertion of insulator silicon dioxide (SiO2). Considering the width of SiO2 as equivalent to the gate oxide width (0.9 nm), parallel lines are required, with a distance of 0.45 nm from the main straight line. Two sets of equations are formulated, representing the parallel lines, enabling the delineation of the SiO2 insertion area.

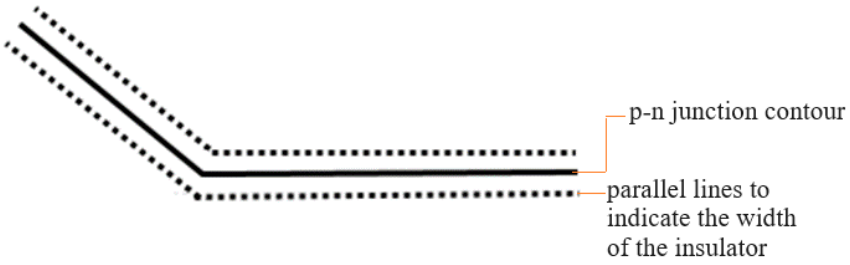


Figure 5: Two parallel lines required for each straight segment of the p-n junction, oriented in opposite directions to delineate the area.

$$c_p = \{(\sqrt{1 + m^2}) * d\} + c \quad (5)$$

$$c_q = \{(\sqrt{1 + m^2}) * d\} - c \quad (6)$$

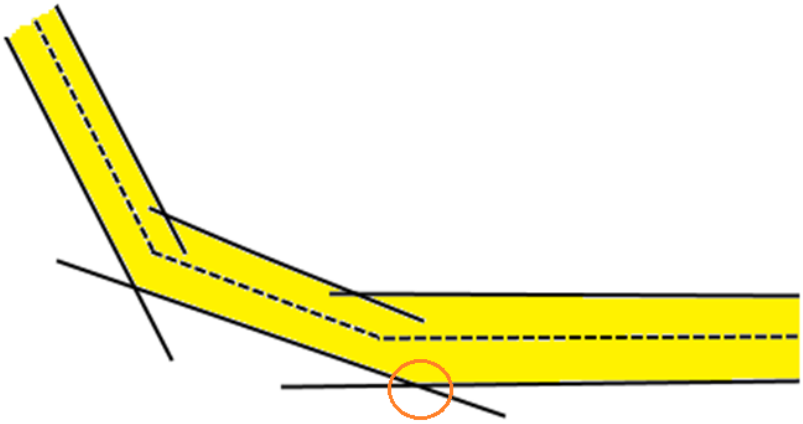


Figure 6: Illustration highlighting the necessity of determining coordinates for intersection points, crucial for defining the boundary line of the SiO2 structure.

E. Derivation of Perpendicular Equations

The path is partitioned into a hundred segments, termed as unit length. Sequentially moving from the lower right position towards the upper left side, coordinates are obtained, guided by the straight line equations. Perpendicular lines are drawn with the angle calculated accordingly. This enables the determination of the equation for each perpendicular line, essential for identifying the intersection points with parallel lines.

$$m_p = \frac{-1}{m} \quad (7)$$

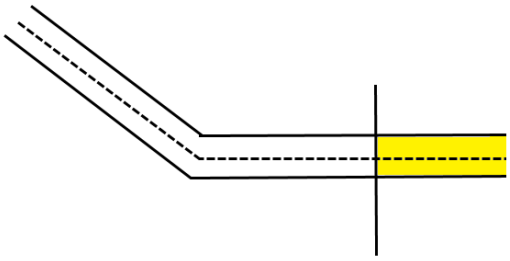


Figure 7: Delineation of the precise shape of the SiO2 structure for each simulation.

F. Practical Implementation

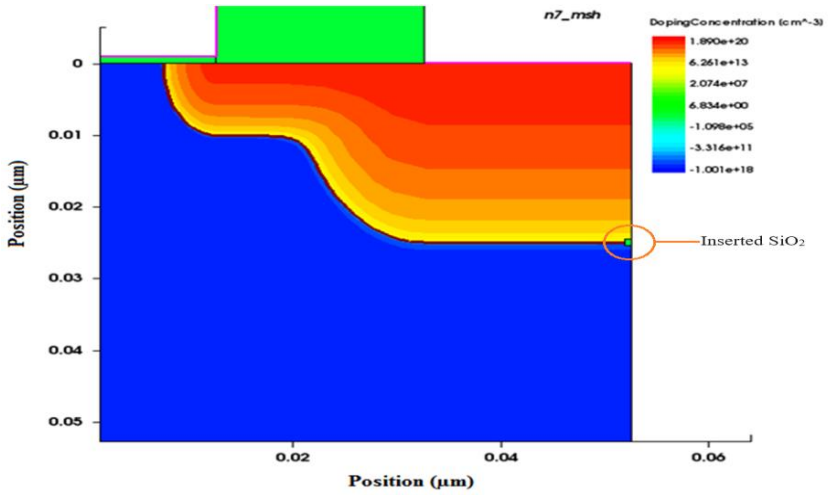


Figure 8(a): Representation of the initial stage. Specifically, the lower right portion is depicted as covered (green).

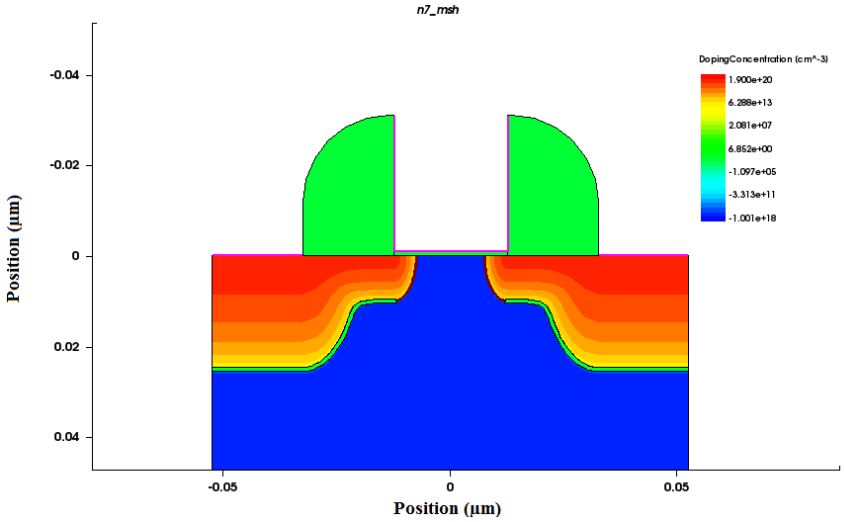


Figure 8(b): Insertion of SiO_2 along the length.

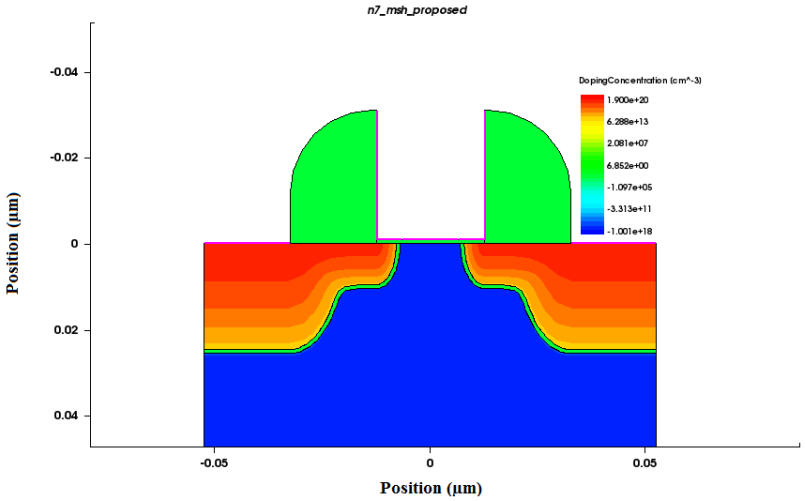


Figure 8(c): Complete coverage.

Figure 8 demonstrates the progressive coverage of the p-n junctions with SiO2 structures. Employing the coordinates obtained through the aforementioned steps, the insulator is filled, sequentially with SiO2, and simulations are iteratively conducted. Figure 8(a) illustrates the initial stage with only one part filled with SiO2. Subsequent iterations, as shown in Figure 8(b) and Figure 8(c), exhibit the gradual filling of SiO2 structures, culminating in the complete deletion of the p-n junction through the inserted insulator.

IV. RESULTS AND DISCUSSION

The development of SiO2 was meticulously executed across 100 incremental steps. As depicted in Figure 8(a), Step 1 commenced with the coverage of a single portion with SiO_2, followed by subsequent simulations to ascertain ON and OFF currents. Each subsequent step involved the increment of SiO2 coverage by two parts of the contour, with a total of 100 simulations conducted, each corresponding to a distinct SiO2 structure.

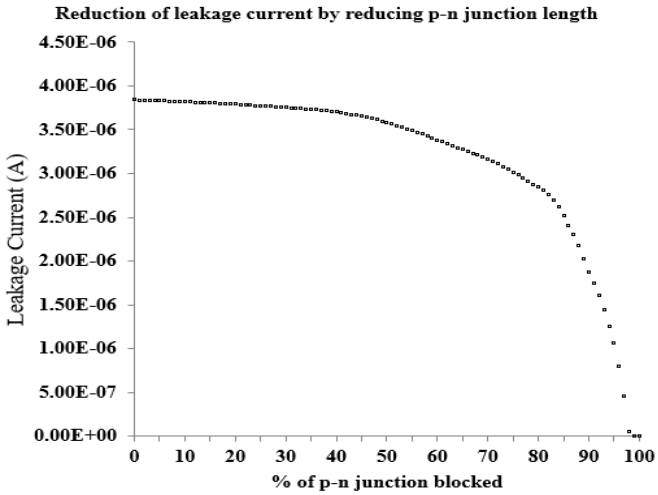


Figure 9: Reduction of leakage current achieved by obstructing specific segments. Result data is represented by black squares.

Figure 9 presents the non-conducting stage, observed across a total of 100 results. The graph exhibits an exponential trend. It suggests that the introduction of SiO_2 at the contour leads to an exponential reduction in leakage current. This observation underscores the potential of SiO2 insertion to significantly mitigate subthreshold leakage current. However, the impact of this method on ON current must also be evaluated. A substantial reduction in ON current, potentially impairing device speed, would outweigh the benefits conferred by leakage current reduction.

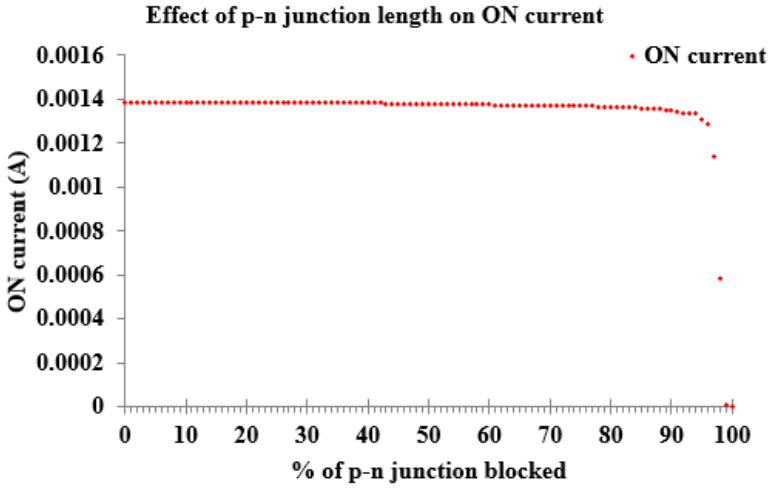


Figure 10: Demonstrating that, aside from the channel portion, the insertion of the insulator does affect conduction.

Analysis of the experimental data reveals that aside from the channel area beneath the gate oxide, the coverage of the border exerts negligible impact on ON current. Remarkably, except the last 5% yields only a slight reduction in ON current. These findings empower designers to tailor their design. The SiO2 emerges as a viable strategy for substantially minimizing leakage current without significantly compromising ON current.

V. SUMMARY AND CONCLUSIONS

The development of a robust algorithm facilitated the precise extraction of coordinates delineating the p-n junction contour of the MOSFET. Leveraging fundamental mathematical equations, a specialized SiO2 structure was devised to envelop the entire contour. This structure was partitioned into 100 segments, and through a series of 100 simulations, each segment was incrementally incorporated.

The graphical representation elucidated a direct mathematical relationship, exhibiting an exponential correlation with the length. Notably, the covering of p-n junctions exerted minimal impact on ON current, barring the channel area. Consequently, designers possess the flexibility to refine conventional MOSFET configurations by selectively masking p-n junction areas, thereby effecting significant reductions in leakage current while preserving ON current integrity.

The algorithm's efficacy in acquiring p-n junction contour coordinates was validated through 100 distinct simulations conducted via TCAD software. These simulations established an exponential term. Armed with these findings, designers can discern and implement optimal combinations tailored to the requirements.

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