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Single Source Switched Capacitor Based Multilevel Inverter With Reduced Number of Components

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Abstract: - Multilevel inverters find extensive use across various applications owing to their capability to generate voltage waveforms of superior quality. thereby minimizing harmonic distortion. Traditional multilevel inverters require a substantial number of power semiconductor devices and passive components, resulting in heightened costs, intricacy, and physical dimensions. These multilevel inverters play a pivotal role in the electric vehicle sector, serving as a critical component in EV power trains for converting Convert DC power from batteries into AC power to operate electric motors.. The research methodology involves the following steps: Design and configuration of a multilevel inverter utilizing switched capacitor technology from a single source.. Design proposed topologies for multilevel inverter design. Design a circuit according topologies in MATLAB. Comparative analysis with existing multilevel inverter designs. Evaluation of the inverter's performance in terms of harmonic distortion, output voltage quality, and efficiency. Rather than employing a multilevel inverter with fewer switches that operates from a single source the highest possible levels are preferred. This paper introduces an innovative 9-level multilevel inverter based on a single source and switched capacitors, which significantly reduces the number of switches required, utilizing only three capacitors and a single DC source. This design approach serves to streamline the inverter's intricacy, decrease costs, and minimize its physical footprint. Furthermore, it elevates the voltage levels by up to 96%, enhancing the overall performance and efficiency of the inverter. Additionally, this technology can be applied in electric vehicles, integrated with renewable energy sources, and utilized in industrial settings. The novelty of this research lies in the utilization of a single-source switched capacitor configuration to achieve multilevel inverter functionality. This approach reduces the number of components required, leading to potential cost savings and improved system reliability. The novel features of this study include: Integration of switched capacitors in a single-source multilevel inverter design. Achieving multilevel inverter functionality with fewer components. Improved performance and efficiency compared to traditional multilevel inverter designs.

Keywords: Multilevel Inverter, Switched Capacitor, Power Conversion, Component Reduction, Harmonic Reduction, Efficiency, Novel Design, Reliability, Single-Source Configuration, Output Voltage Quality

I.INTRODUCTION

Multilevel inverters, widely applied in various fields like industrial drive systems and renewable energy production, typically feature a structure that includes Utilizing an input source, airborne capacitors, and a half H-bridge configuration elements. Within the realm of multilevel inverters, reduced switch configurations, both symmetrical and asymmetrical, offer the advantage of fewer active state switches and reduced overall voltage blocking requirements across the switches[1].

Inverters play a vital role in converting direct current (DC) into alternating current (AC), enabling between various energy sources and electrical systems. Multilevel inverters have gained popularity in various applications due to their ability to synthesize high-quality output voltages with reduced harmonic distortion. Traditional multilevel inverters, however, suffer from increased complexity and a higher number of components, leading to increased cost, size, and maintenance requirements. The suggested multilevel inverter utilizing a single-source switched capacitor aims to address these challenges by using a simplified topology while maintaining high voltage output quality [2]. Multilevel inverters (MLIs) find extensive application across various fields, including industrial drives and the generation of renewable energy. The predominant configuration for multilevel inverters involves an input source, airborne capacitors, and interconnected H-bridge configurations. Among these, the most favored demonstration of MLIs is the combination of cascaded H-bridge and flying capacitors. In comparison to the H-bridge configuration, the flying capacitor has a more pronounced presence in the market. This is primarily attributed to its advantages, which include fewer components, improved efficiency, and superior voltage balancing

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capabilities. [3]

A flying capacitor is a component designed to store and transfer electrical energy between different parts of a circuit. Unlike fixed capacitors, which remain connected to a single voltage source, flying capacitors can change their voltage levels powerfully by interfacing with various voltage sources or hubs inside a circuit. This powerful voltage exchanging ability supplies the flying capacitor with flexibility and empowers its utilization in a scope of uses [4].

The symmetric and asymmetric cascade MLI configurations involve the use of cascading structure was employed to create a switched capacitor converter, which produces an uneven voltage boost, showcasing the utilization of equal and unequal direct current (DC) sources[5]. Likewise, a pioneering approach to creating a cascade MLI with fewer components was presented, imposing elevated voltage demands on the H-bridge. However, the asymmetric MLI configuration necessitates intricate control systems, variable ratings for control switches, and disparate DC power sources. In contrast, the symmetric topology, featuring a single power source, a reduced component count, utilization of n-crisscross capacitor units provides a competitive advantage compared to traditional asymmetric MLIs. This is due to its ability to generate a greater number of voltage steps with a reduced requirement for equal DC power sources. Nonetheless, this cascading method introduces a multitude of components, leading to elevated expenses. [6]

Recently, the implementation of switched-capacitor topologies has played a significant role in reducing the requirement for multiple voltage supplies. Achieving voltage boosting from a single-source, without the use of a transformer, is crucial for grid power production[7]. Detailed comparisons of power converters have been discussed in other sources. While these switched-capacitor configurations offer advantages such as the use of decreasing the number of capacitors, minimizing switches, utilizing single input sources, implementing automated capacitor voltage balancing, and optimizing voltage gain are key strategies for enhancing the efficiency of the system, they still present a challenging task [8].

To highlight that in these configurations, the H-bridge experiences substantial voltage stress across its switches doesn't guarantee voltage boosting. These configurations have undergone testing in various load conditions and have demonstrated their ability to self-balance the capacitor voltages, although they achieve only unity voltage gain[9]. The comparison of parameters for these latest switched-capacitor inverters will be instrumental in the development of new structural improvements.

Multilevel inverters provide unique advantages, including switches experiencing minimal voltage stress and the delivery of high-quality output voltages. [10 - 12]. However, these topologies incorporate diodes positioned leads to increased current demands in the charging circuit between the source and capacitors[13 -14]. These multilevel inverters represent a specialized variant of converters, which offer structural advantages in terms of straightforward horizontal/vertical expansion. One of the primary advantages of these inverters is their ability to maintain minimal voltage stress, but they do come with the drawback of requiring three large capacitors[15 - 16].

Additionally, among multilevel inverters, the switched-capacitor topology is particularly prevalent due to its capacity to keep voltage stress low and facilitate voltage boosting[17 -18][23-24]. Nonetheless, a drawback of this configuration is that it involves the use of four switches to facilitate the flow of a substantial current within the charging loop. Various multilevel inverter topologies are available, each suited for specific applications that require varying degrees of voltage gain[19-20][25].

In this study, the suggested configuration employs a single input DC source to effectively double the output voltage, making it an attractive option. This design provides several advantages by addressing various limitations commonly associated with typical multilevel inverters (MILs). These challenges include issues such as voltage disparities, an increased number of switches, and the necessity for extra circuitry to condition the signal. Interconnected in series or parallel, the switched cells in the extended setup are each equipped with DC-DC transformation branches. Each cell that has been switched contains at least two capacitors and four switches, except for the final cell. As a result, adjusting the number of switched-capacitor cells allows for easy modification of the proposed inverter's output voltage levels.

II.PROPOSED TOPOLOGY

The newly introduced nine-level boosting inverter with a hybrid design effectively minimized the count of active components, comprising specifically three capacitors. Specifically, there are five active switches connected at each voltage level. Given this context, the topology depicted in Figure 1 reducing the component count while

retaining the advantages of the prior configuration, this paper suggests a distinctive design that requires a minimum of four high-current rated power electronic elements and three capacitors, effectively tackling the challenges associated with high current flow through the switches.

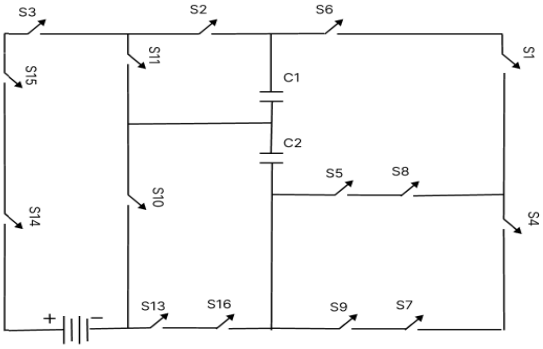


Figure 1 Circuit Diagram of 9-level MLI

The proposed design is a Single Source Switched Capacitor (SSSC) based 9-level MLI and its corresponding extension, illustrated in Figure 1. It features a DC voltage Vin, 2 flying capacitors denoted as C1 and C2, and sixteen semiconductor switches labeled as S1 to S16. This configuration generates an output voltage that is twice providing nine distinct output voltage levels based on the input voltage. Moreover, a half H-bridge is utilized to change the polarity of the output voltages, leading to varying output voltage levels of 0, ± $V_{in}/2$, ± V_{in}, ± $3V_{in}/2$, and ± $2V_{in}$

2.1 Power Losses Analysis

2.1.1The Switching Losses (Psw)

Switching losses arise from the interaction between voltage and current throughout the procedure of turning a switch on or off operation, encompassing both switch-on loss (P_{sw},on) and switch-off loss (P_{sw},off). To streamline the process, the calculation of these switching losses involves utilizing a linear approximation of voltage and current, this calculation method is grounded in [16], the P_{sw},on and P_{sw},off of the i-th switch are expressed as

SWITCH ON

$$Psw, on, i = fswvsw, i(t)i(t)dt$$
$$= fswRton\ 0\ (-Vsw, i/\ ton\ (t - ton)\ ))\ *\ (Ion, i/\ ton\ )t * dt$$
$$= \frac{(fswVsw, iIon, iton)}{6} \quad (1)$$

$$\underline{SWITCHOFF}$$
$$Psw, off, i = fswvsw, i(t)i(t)dt$$
$$= fswRtoff\ 0\ (-Vsw, i/\ toff\ (t - toff)\ ))\ *\ (Ioff, i/\ toff\ )t * dt$$
$$= \frac{(fswVsw, iIoff, itoff)}{6} \quad (2)$$

Overall switching

$$Psw = 12 \sum i = 1\ (Psw, on, i + Psw, off, i). \quad (3)$$

2.1.2 Conduction losses

Conduction losses occur due to the resistance encountered across various components within semiconductor

devices and capacitors. This includes conduction resistance (Rs) in switches, internal resistance (Rd) in diodes, and equivalent series resistance (ESRC) in capacitors.

$$E0 \sim Vdc = \{Iosin(2\pi ft)]\text{^}2 * Req, 1 * (Arefsin(2\pi fot))/ Ac + + Req, 0(1 - Arefsin(2\pi fot) /Ac)\} dt \quad (4)$$

2.1.3 Ripple losses

Ripple losses are a result of voltage fluctuations in capacitors, and you can determine the voltage ripple in capacitors C1, C2, and C3 as follows

$$\Delta VC1 = \Delta VC2 = \Delta Q1/ C1 \quad (5)$$

$$\Delta VC3 = \Delta Q3/ C3 \quad (6)$$

where the ΔVC1, ΔVC2, and ΔVC3 are the voltage ripples of capacitors C1, C2, and C3, respectively. According to the calculation method, the ripple losses of the capacitors are expressed as

$$Prip = fo/ 2\ 3 \sum k = 1(Ck\Delta V\ \text{^}2\ Ck) \quad (7)$$

In summary, the power losses associated with the suggested 9-level topology can be represented as

$$Ploss = Psw + Pcon + Prip. \quad (8)$$

Finally, the theoretical efficiency is indicated by η, which is defined by

$$\eta = Po/ Psw + Pcon + Prip + P \quad (9)$$

III.METHODOLOGY

The proposed topology design for the SSSC-MLI 9-level with reduced components leverages a unique combination of switched capacitor modules and innovative control strategies. By judiciously selecting capacitor values and integrating them with the switching network, it achieves higher reduced component counts result in lower voltage levels. The design minimizes the number of switches and capacitors while ensuring efficient voltage synthesis. This novel approach optimizes component utilization, reducing cost, size, and complexity, ultimately enhancing the SSSC-MLI's practicality and affordability for examples of applications include renewable energy systems and motor drives, without compromising performance.

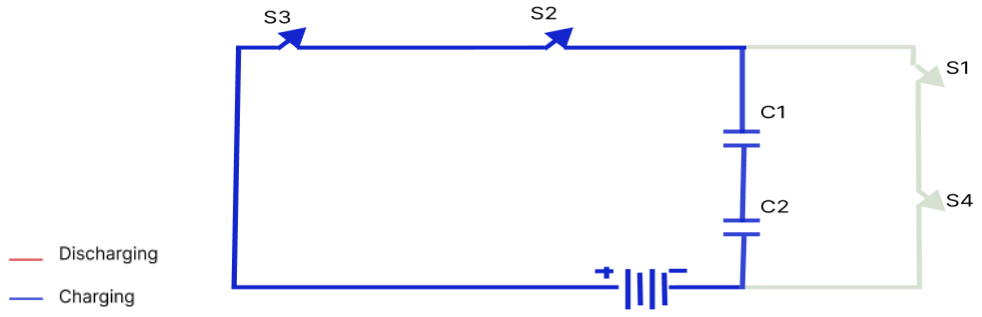


Figure 2 Flow diagram of the switch S3 and S2

In Fig 2, when the switches S3 and S2 is turn on, the voltage from the supply flows through the capacitor then the capacitor C1 and C2 gets charged.

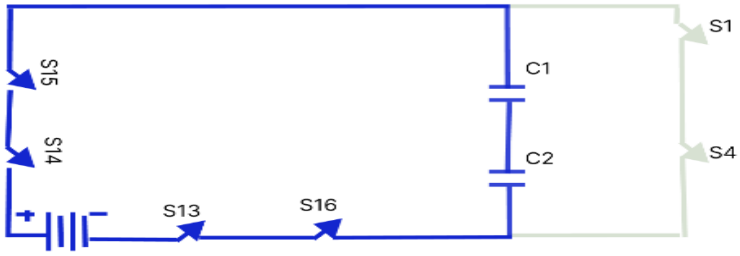


Figure 3 Flow diagram of the switch S15, S14, S13, S16

In figure 3, switches S14 and S15 turns on, the voltage starts flowing through the circuit. When the switches S14 and S15 turned on, the switch S13 and S16 gets turned off. By this repeated switching of switches S14 , S15 and S13, S16 the capacitor C1 and C2 gets charged.

$$S14\,S15 > S13\,S16$$
$$S13\,S16 > S14\,S15$$

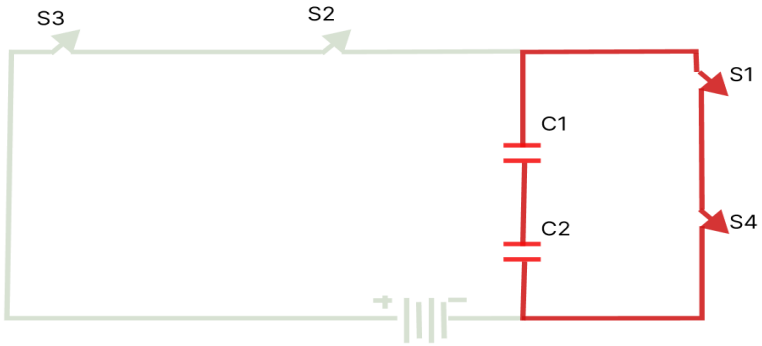


Figure 4 Flow diagram of the switch S1 and S4

In figure 4, the capacitor gets charged by switches S3 and S2 .After the capacitor gets fully charged, the voltage from capacitor C1 and C2 starts discharging by turning on switch S1 and S4.

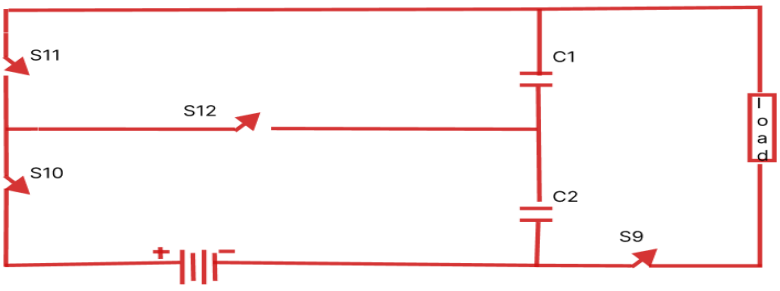


Figure 5 Flow diagram of the switch S11,S10,S12,S9

In figure 5, after the capacitor C1 and C2 gets fully charged the capacitor starts discharging. When switches S11 and S10 gets turned on, switches S9 and S12 gets turned off automatically. Now the capacitor C1 and C2 starts discharging through switches S11 and S10 to load . Similarly when the switches S12 and S9 gets turned on , switches S11 and S10 gets turned off then the voltage from capacitor C1 and C2 starts discharging through switches S12 and S9 to the load.

$$S11\,S10 > S9\,S12$$
$$S9\,S12 > S11\,S10$$

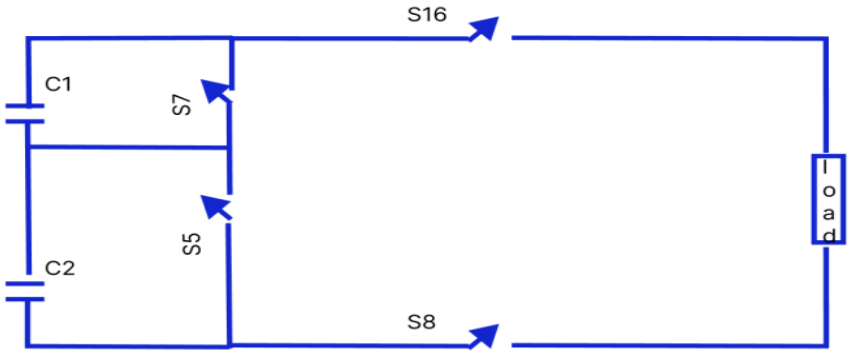


Figure 6 Flow diagram of theswitch S5, S6, S7, S8

In the figure 6,The capacitor C1 and C2 gets charged when the switches S5 and S8 gets turned on, switches S7 and S6 gets turned off similarly when S7 and S6 gets turned on, switches S5 and S8 gets turned off.

$$S5\ S8\ > S7\ S6$$

$$S7\ S6\ > S5\ S8$$

By researching literature review to understand the existing state-of-the-art technologies related to multilevel inverters, switched capacitor techniques, and component reduction strategies. Select the appropriate components for your multilevel inverter design based on the objectives for the project. Consider the factor of component rating, cycle, count and performance. Develop the circuit with flying capacitor topology for inverter. The selected topology should determine the reduction of components while ensuring that have desired voltage and frequency requirements. Flying capacitors is used generate multiple voltage levels from a single dc source. Flying capacitors are capacitors that are connected to multiple switches and can be switched to different voltage levels. This allows the SS9LMI to generate a variety of output voltage levels by switching the flying capacitors in different configurations. 9-level FCMLI typically consists of nine switches and four flying capacitors. The switches are arranged in a series of cascaded H-bridges.

The flying capacitors are connected to the H-bridges in a variety of ways to generate the nine output voltage levels. To validate the inverter's performance and achieve the desired output, it's essential to simulate its operation under various operating conditions and loads. Pulse width modulation (PWM) is a technique employed to regulate the output voltage of power electronic converters. It operates by rapidly switching the converter's switches on and off, and by adjusting the pulse width of these switches to control the output voltage. The 9-level inverter is a power electronic converter capable of producing nine distinct output voltage levels as shown in Table 2. This is accomplished by employing a combination of switches and capacitors to generate different voltage levels from a single DC source. PWM offers versatile control over the output voltage of a 9-level inverter, and the table below illustrates the switching stages and voltage sequences of the switches at different stages levels in which capacitor charges (CH), discharges (DS) and No charge (NC) according to the switching stages as shown in table 1.

Table 1 Switching stages

Stage1	S1	S2	S3	S4	C1	C2
	1	0	0	1	DS	DS
	0	1	1	0	NC	DS
Stage2	S5	S6	S7	S8	C1	C2
	1	0	0	1	CH	CH

	0	1	1	0	CH	CH
Stage3	S9	S10	S11	S12	C1	C2
	1	0	0	1	CH	CH
	0	1	1	0	CH	CH
Stage4	S13	S14	S15	S16	C1	C2
	0	1	1	0	CH	CH
	1	0	0	1	DS	NC

Table 2 Voltage sequence

Voltages	Switches
+2Vin	S1-S2-S8
+2Vin/2	S2-S8-S9
+Vin/2	S2-S5-S6-S9
0	S2-S4-S5-S6
-Vin/2	S3-S5-S6-S9
-Vin	S3-S4-S5-S6
-3Vin/2	S3-S7-S9
-2Vin	S3-S4-S7

IV. Results and Discussion

A 9-level multilevel inverter based on a single switched capacitor source, which minimizes the number of components, operates by utilizing a lone DC source to generate multiple output voltage levels. This inverter relies on capacitors for energy storage and voltage level creation. Employing a reduced switching scheme reduces the component count, resulting in a more compact, lighter, and more efficient inverter. Utilizing MATLAB software aids in mathematical computations, algorithm development, modeling, simulations, prototyping, data analysis, exploration, and visualization. Through the utilization of MATLAB/SIMULINK modeling and simulation software, the performance of the single-source switched capacitor-based 9-level multilevel inverter with reduced components has been simulated, resulting in the desired output.

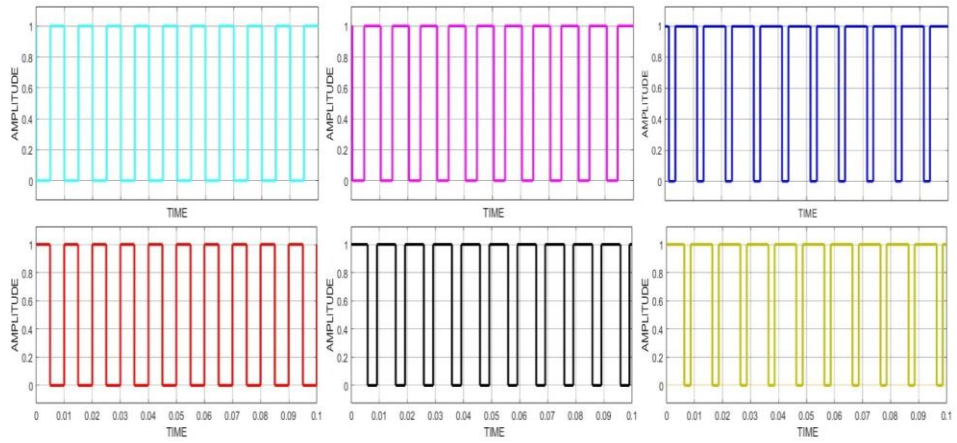
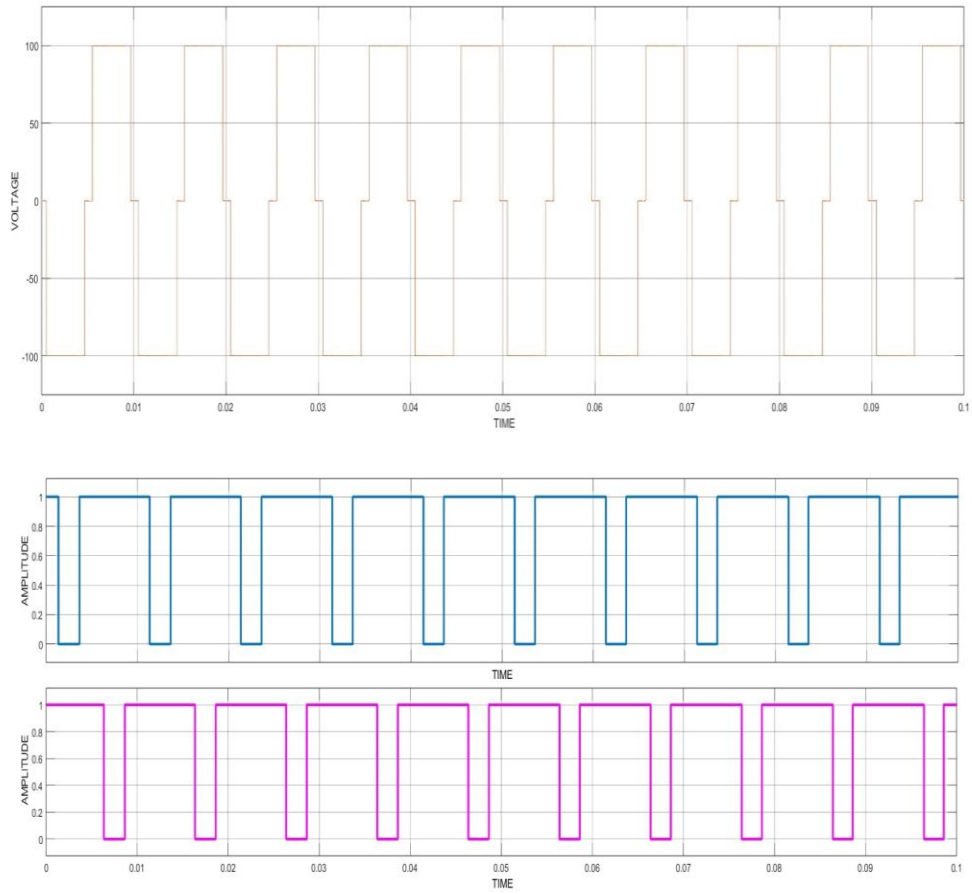


Figure 7 Pulse width modulation curve



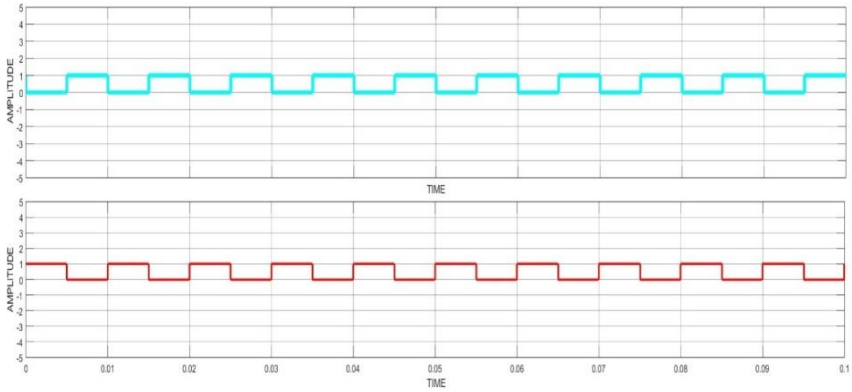


Figure 8 MOSFET switches flow diagrams

Figure7,8 shows about the output waveform of pulse width modulation, PWM rectify the waveform from the pulse generator andgive efficient wave form. It also specifies about the switching frequencies of the MOSFET switches. The inverter uses capacitors to store energy and to create the different voltage levels. The number of components in the inverter can be reduced by using a reduced switching scheme form the related waveforms output. This can lead to a smaller, lighter, and more efficient inverter.

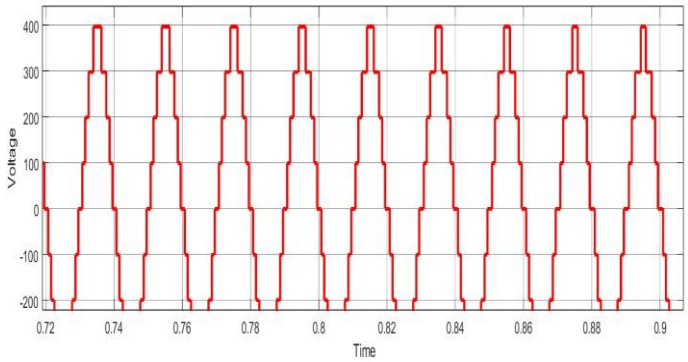


Figure 9 Output Model of the single source switched capacitor based 9-level multilevel inverter with reduced components

Figure 9 provides a visual representation of the results obtained from steady-state experiments, along with an efficiency curve. The output voltage generated by the implemented circuit registers at 400 volts, affirming that the recommended inverter can indeed achieve a voltage amplification of 4. It's worth highlighting that capacitors C1 and C2 maintain charges at approximately 28.66 V and 57.65 V, respectively. Furthermore, the voltage across the capacitors exhibits periodic fluctuations within a 5 V range, demonstrating the inherent self-balancing capacity of the proposed inverter. The capacitors within the extended inverters demonstrate their effectiveness in storing voltage over extended durations. The figure 9 shows the waveform of pulse width modulation for boosting the voltage levels of subsystems.

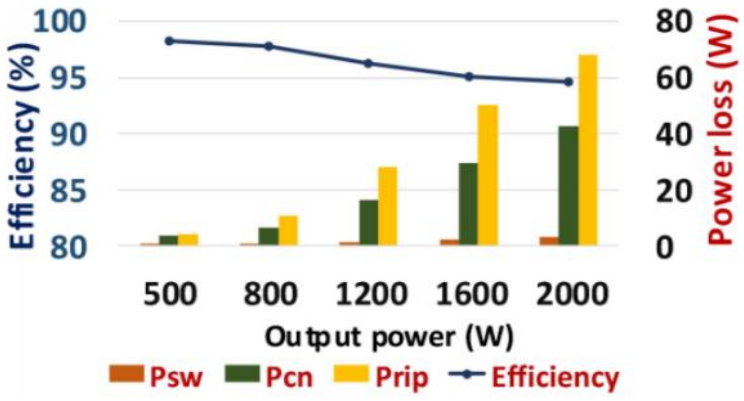


Figure10 Overall efficiency and power loss curve

The figure 10 shows the efficiency and power losses of the proposed model by comparing of other related topology. Here ripple power loss is higher than conduction and switching powers. In the existing 9 level multilevel inverter the overall efficiency is around 90% but in this paper, the efficiency increases by around 3-5% by comparing with any other proposed topologies. This helps to boost up the voltage levels, with the help of the switching sequence. By using this advantage, the performance of the switches will be increases, losses will be reduced, the desired output will be gained, lifespan of the machine will be also increases. By further research and development we can slightly increase the efficiency and boost the voltage levels in different other topologies.

V.CONCLUSION

This paper presents a unique topology featuring nine levels from a single source, along with its extensions. At the core of this innovative nine-level boost inverter topology lies a switched capacitor configuration, which minimizes the need for numerous switches. Through a comprehensive comparative analysis, it becomes evident that this pioneering approach significantly reduces the component requirements for attaining nine distinct voltage levels. Moreover, this technology can be further expanded to support various levels (n levels), it forms the basis for both horizontal and vertical extensions. The paper includes a standardized switching table to clarify the operation of these extended inverters. Simulation and experimental results, presented within this study, validate the operational theory and underscore the effectiveness of the proposed topology, particularly when dealing with high-inductive loads. In summary, a comprehensive comparative analysis underscores the benefits of the suggested topology and underscores its appropriateness for a broad range of uses. These applications include increasing voltage in renewable energy sources, controlling speed through variable frequency operations, and adjusting voltage with different modulation indices, and ensuring consistent torque by managing the voltage/frequency ratio.

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