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Designing Power-Efficient BIST Architecture: Leveraging Reversible Logic for Scalable Digital Systems

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Abstract: - This paper presents a novel approach to optimizing power usage in scalable Built-In Self-Test (BIST) controllers. While BIST mechanisms are crucial for maintaining the reliability of digital circuits, they can be excessively power-hungry during testing phases, particularly in applications where energy consumption is a concern. We propose an innovative architecture incorporating reversible logic gates and circuits to overcome this challenge. Reversible logic is renowned for its low power consumption as it retains information. By integrating reversible logic into our architecture, we can significantly reduce power usage during test cycles, making it an ideal solution for scalable systems ranging from 8 to 32 bits. Our trials showed substantial power savings compared to traditional BIST approaches without sacrificing test coverage or efficiency. Our research provides new opportunities to develop energy-efficient testing methods for digital circuits, contributing to broader efforts in sustainable electronics design.

Keywords: Built-in self-test (BIST), Circuit-Under-Test (CUT), Linear Feedback Shift Registers (LFSRs), Multiple Input Signature Register (MISR)

I. INTRODUCTION

Over the past few years, with the rapid development of digital systems, their complexity and functionality have also increased significantly. As a result, advanced testing methodologies are necessary to ensure the systems' reliability and efficiency. Built-in self-test (BIST) controllers have become essential because they can integrate testing mechanisms directly within the circuitry. This enables continuous and comprehensive evaluation of digital systems' operational integrity, making them an invaluable tool for maintaining high levels of system performance[2,4-6].

As digital systems grow in complexity, the range of the bits used to operate them expands from 8 to 32 bits. This variety is needed to cater to different applications. However, the power consumption associated with BIST (Built-In Self-Test) operations has increased. This poses a significant challenge, especially in power-sensitive environments like mobile devices, wearable technology, and embedded systems. Therefore, there is a pressing need for innovative solutions that ensure the robustness of BIST controllers and address the critical issue of power efficiency. Welcome to the realm of reversible logic, a paradigm that offers a revolutionary approach to traditional logic gates, ensuring that no information is lost during computation. Unlike conventional logic systems, where the loss of information leads to energy dissipation, reversible logic is based on preventing information erasure, resulting in significantly reduced power consumption. This theoretical foundation provides a promising pathway for developing more efficient and sustainable computing systems[1,7-9].

This paper presents a new architecture that uses reversible logic to optimize power consumption in scalable BIST (Built-In Self-Test) controllers. Our approach not only meets the basic requirements of BIST, such as fault detection and diagnostic capability, but also reduces power usage significantly for different system sizes (8, 16, and 32 bits). The innovative architecture provides scalability, power efficiency, and testing integrity, which is expected to set a new standard for designing future digital systems[6,12-15].

The research aims to save power and promote sustainable digital design practices, contributing to the efforts towards energy-efficient electronics.

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In the following sections, we will explain the methodology behind the new architecture, discuss its implementation, and present a comparative analysis against traditional BIST solutions. This will help to highlight the significant advancements made through this research and the potential impact it could have.

II. BASIC PRINCIPLES OF REVERSIBLE LOGIC

The present study is concerned with reversible logic, characterized by a unique non-dissipative nature that distinguishes it from conventional irreversible logic. Unlike the latter, which inevitably results in information loss and heat generation, reversible computing ensures that no information is lost during computation. In reversible logic, each output of a logic gate is uniquely mapped to its inputs, thereby reducing power consumption. This feature is of great significance, given that energy is only dissipated in the event of information erasure, as per Landauer's principle. The proposed architecture employs reversible logic gates to mitigate energy loss, which is expected to pave the way for developing more energy-efficient digital systems.

2.1 Quantum Computing: An Overview

Quantum computing is a revolutionary technology that operates on the principles of quantum mechanics. It differs from classical computing as it uses quantum bits (qubits) that can exist in multiple states simultaneously, thanks to the concept of superposition. This unique feature allows quantum computers to process information significantly faster than classical computers. Although our study primarily focuses on classical reversible logic, understanding the fundamentals of quantum computing is vital as it provides a theoretical foundation and inspiration for implementing reversible principles in classical systems. This implementation can help in reducing power consumption.

2.2 Elementary Quantum Logic Gates

In quantum computing, logic gates function differently than traditional logic gates. Basic quantum gates like the Pauli-X, Hadamard, and CNOT (Controlled-NOT) are crucial in manipulating qubits. These gates are inherently reversible and can perform basic quantum operations without losing any information, similar to the reversible logic gates in our proposed BIST architecture. By drawing parallels between quantum and classical reversible logic gates, we can gain insights into designing more efficient classical systems.

2.3 Optimization Parameters for Reversible Logic

Optimizing reversible logic circuits involves reducing parameters such as quantum cost, gate count, and garbage outputs. Quantum cost is associated with implementing a reversible gate using elementary quantum operations. Gate count refers to the total number of gates used in a circuit, affecting the design's complexity and size. Garbage outputs are extra outputs required to maintain reversibility but are not used. Our architecture takes special care to consider these parameters, ensuring power optimization is achieved without increasing complexity or inefficiency.

2.4 Fundamental quantum gates

Fundamental quantum gates are the basic building blocks of quantum computing, similar to the classical logic gates in traditional computing. Here's a brief description of some of the primary ones:

- **Pauli Gates (X, Y, Z)**: These are the quantum equivalents of bit-flip (X), phase-flip (Z), and a combination of bit and phase-flip (Y). The X gate works like a classical NOT gate, flipping the state of a qubit.

- **Hadamard Gate (H)**: It creates a superposition of states, putting a qubit into an equal combination of 0 and 1, which is crucial for many quantum algorithms.

- **Controlled NOT Gate (CNOT)**: A two-qubit operation where the second qubit flips if the first qubit (control qubit) is in state 1. It's essential for entangling qubits, a fundamental property of quantum computing.

- **Toffoli Gate (CCNOT)**: A three-qubit gate flips the third qubit only if the first two (control qubits) are in state 1, often used for classical logic operations within quantum circuits.

- **Phase Shift Gate (S, T)**: These apply a phase to the qubit state, with the S gate applying a quarter turn and the T gate an eighth turn on the Bloch sphere. They're used for more precise control over qubits.

These quantum gates manipulate the state of qubits to perform operations. They can execute complex algorithms that outperform classical computing for specific tasks.

2.5 BIST Controller

The Built-In Self-Test (BIST) controller is an indispensable component of contemporary digital systems that guarantees the dependability and correct functioning of integrated circuits (ICs) and systems on a chip (SoC). The device can test itself by shifting from external testing methods to an internal mechanism, resulting in numerous advantages, such as decreased testing duration, expenses, and intricacy. This is especially significant as ICs become increasingly advanced and compact.

2.6 Functionality of BIST Controllers

The primary function of the BIST controller is to generate test patterns, apply them to the circuit-under-test (CUT), and analyze the output results to detect any faults. This is accomplished through two key components: the Test Pattern Generator (TPG) and the Output Response Analyzer (ORA). The TPG creates binary patterns to stimulate the CUT, with the complexity and type of patterns varying based on testing requirements and the nature of the circuits being tested. The ORA evaluates the CUT's response to the test patterns. It employs signature analysis techniques like Linear Feedback Shift Registers (LFSRs) to compress output responses and make it easier to spot discrepancies that indicate faults.

2.7 Types of BIST and Advantages

BIST (Built-In Self-Test) methodologies for ICs can be categorized into three types: Memory BIST (MBIST) for testing memory elements, Logic BIST (LBIST) for testing logic circuits, and Mixed-Signal BIST for testing systems with digital and analog components.

Advantages of BIST

Integrating BIST (Built-In Self-Test) controllers into digital systems has several advantages. Firstly, ICs (Integrated Circuits) can self-test, which reduces dependency on external testing resources, resulting in lower production costs and faster time-to-market. Secondly, BIST can cover many fault types and conditions, offering comprehensive testing capabilities. Thirdly, as systems become complex, BIST can scale accordingly to handle increased testing requirements without significantly altering the testing infrastructure. Lastly, BIST allows for continual testing during regular operation, enhancing reliability and fault detection over the product's lifecycle.

2.8 Challenges and Considerations

BIST controllers help ensure the reliability and functionality of modern digital systems. However, they can pose particular challenges, such as increased chip area and potential impact on system performance due to the additional logic required for testing. Therefore, balancing thoroughness and test time is essential to optimize the BIST controller for a practical yet efficient testing process. In conclusion, designing and implementing a BIST controller requires careful consideration of efficiency, coverage, and resource utilization to meet the evolving demands of complex ICs and SoCs. The BIST controller is pivotal in modern digital systems, offering a self-contained mechanism for ensuring system reliability and functionality.

III. Literature Review

These papers show a noticeable trend of improving LBIST (Logic Built-In Self-Test) architectures by enhancing their phase shift capabilities, reducing power consumption, and optimizing their area efficiency. These improvements have been made without compromising the quality of test patterns and fault coverage. Such advancements have significantly contributed to the scalability and effectiveness of LBIST modules in modern integrated circuits. These advancements contribute considerably to the scalability and effectiveness of LBIST modules in modern integrated circuits[1-3,24-25].

These works focus on the significance of enhancing LBIST through different methodologies. These include improving test pattern generation with DT-LFSR-TPG, reducing power consumption with weighted TPG, using reversible logic to achieve computational efficiency, and refining TPI strategies to address RPR faults[4-5].

"Optimized Designs of Reversible Arithmetic Logic Unit" discusses the creation of new, cost-effective reversible Arithmetic Logic Units (ALUs) using quantum gates. Reversible logic is a promising paradigm in low-power VLSI design and quantum computing, reducing power dissipation by preventing information loss during computation. The paper proposes two innovative designs of reversible ALUs with better performance and function generation than current designs[6].

These studies collectively advance the efficiency and effectiveness of built-in self-test applications and reversible computing, taking significant steps towards more energy-efficient and comprehensive testing methods in modern integrated circuits[7-10].

The research proposes a new way to optimize digital circuit testing. Combining an accumulator-based method with machine learning enhances built-in self-test mechanisms and reduces the number of test vectors required. This streamlines testing without compromising quality by improving time, power consumption, and resource efficiency[11-14].

This paper introduces an innovative approach for enhancing delay fault testing in BIST environments for high-speed circuits through machine learning-based directed random generation, aiming for improved efficiency and cost-effectiveness. It also investigates low-power testing strategies for VLSI circuits, focusing on reducing power consumption during the test phase through test pattern compaction and reordering, demonstrated via the ATALANTA tool and MATLAB. This leads to significant power savings and testing efficiency[15-16].

The research collectively proposes advanced LBIST methodologies for enhancing VLSI and ASIC chip testing. It introduces a novel scan-based LBIST approach utilizing the Low Power Linear Feedback Shift Register (LP-LFSR), significantly reducing power droop and area consumption by 72.5% while maintaining high fault coverage. Additionally, it presents a design for a restartable logic BIST controller for combinational circuits, improving testing flexibility and fault detection by allowing dynamic suspension of signature generation. Furthermore, it details a programmable BIST design based on the STUMPS architecture. It focuses on at-speed testing, power efficiency through multi-voltage design, and area cost reduction, with successful tool implementation demonstrated in Xilinx ISE and Design Compiler. These studies underscore a shift towards more efficient, flexible, and power-conserving testing methodologies in semiconductor design[17-20].

Advancements in LP-LFSR applications and test pattern generation are showcased to reduce power consumption while maintaining or improving fault detection efficiency. This highlights the growing need for power-efficient testing methods in VLSI circuit design[21-23].

IV. PROPOSED DESIGN

In this section, we elaborate on the design and implementation of the novel BIST architecture. We begin with an overview of reversible logic principles and how they can be applied to create energy-efficient testing mechanisms. The architecture's scalability is addressed through the modular design of reversible gates and circuits, which can be adapted to different data widths (8, 16, and 32 bits) without significant alterations in logic complexity or power efficiency.

We then detail the specific reversible gates selected for the BIST operations, including their design, logic functions, and reasons for their selection. The integration of these gates into the BIST controller is explained, highlighting how they contribute to overall power reduction while maintaining or enhancing the test coverage compared to conventional BIST solutions.

The methodology also covers the simulation environment, tools used for design and testing, and the criteria for evaluating power consumption and test effectiveness. This provides a comprehensive framework for assessing the novel architecture's performance in real-world scenarios.

4.1 Optimization of BIST Controller

As integrated circuits grow more complex, the necessity for efficient Built-In Self-Test (BIST) controllers becomes paramount. These controllers, vital for ensuring circuit reliability, face challenges balancing thorough testing with minimal power consumption. This paper explores strategies for optimizing BIST controllers to improve power efficiency without compromising test quality, focusing on innovative approaches that address the evolving demands of modern digital systems. We aim to offer solutions that contribute to more energy-efficient and reliable electronic devices.

4.1.1 Reversible Bit Swapping Linear Feedback Shift Register (BS-LFSR)

The Reversible Bit Swapping Linear Feedback Shift Register (BS-LFSR) architecture integrates several reversible gates, each contributing uniquely to the system's functionality. Here's a breakdown of these components:

Sam Gate

- Type: 3x3 reversible gate (3 inputs, three outputs).
- Input/Output Relationship: Given inputs A, B, and C, the outputs are defined as P = !A, Q =!AB XOR!AC, R = !AC XOR AC. This gate combines inversion and exclusive OR (XOR) operations on its inputs.
- Quantum Cost: 4. The quantum cost indicates the complexity of realizing the gate with basic quantum operations.
- Functionality: Sam Gate can be used for logic operations where inversion and conditional toggling are needed.

Feynman Gate

- Type: 2x2 reversible gate (2 inputs, two outputs).
- Function: Performs the XOR operation on inputs A and B. It's also used for copying outputs due to the reversible logic's restriction of fan-out being one, as shown in Figure 3.
- Quantum Cost: 1. This low cost makes it efficient for operations requiring duplication of signals or simple XOR operations.
- Role: Essential for generating feedback polynomials and facilitating the duplication of signals within the circuit.

Rmux Gate

- Type: 3x3 reversible gate (3 inputs, three outputs).
- Output Equations: P = A, Q = A'B + AC, R = A'C + AB'. It functions based on the input conditions to forward or combine inputs selectively.
- Quantum Cost: 4. Like the Sam Gate, this indicates a moderate level of complexity.
- Purpose: Used for bit swapping based on the most significant bit (MSB) of the LFSR, effectively reducing bit transition and switching activity, which is crucial for power optimization.

Integration and Functionality:

- **Sam and Feynman Gates:** These gates act as a D-flip-flop, capturing input values at the clock's rising edge and maintaining output otherwise. This setup is pivotal for sequential logic and state retention in the reversible LFSR, as shown in Figure 1.

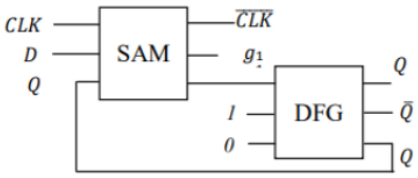


Fig.1. Proposed D-FF

- **Bit Swapping with Rmux Gate:** The Rmux gate's unique functionality for bit swapping based on the LFSR's MSB and the system's state (number of flip-flops) optimizes bit transitions, reducing power consumption. This is especially significant in architectures where minimizing switching activity is a priority for energy efficiency, as shown in Figure 2.

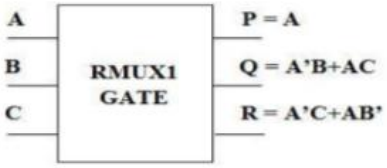


Fig.2. Proposed RMUX

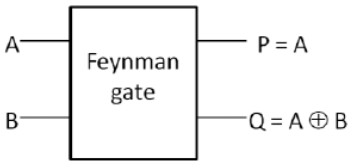


Fig.3. Proposed XOR

The integration of these reversible gates within the BS-LFSR framework shown in Figure 4 underpins a novel approach to BIST controller design. By leveraging the unique properties of reversible logic, this architecture aims to enhance power efficiency, reduce quantum cost where possible, and maintain or improve digital systems' test coverage and reliability.

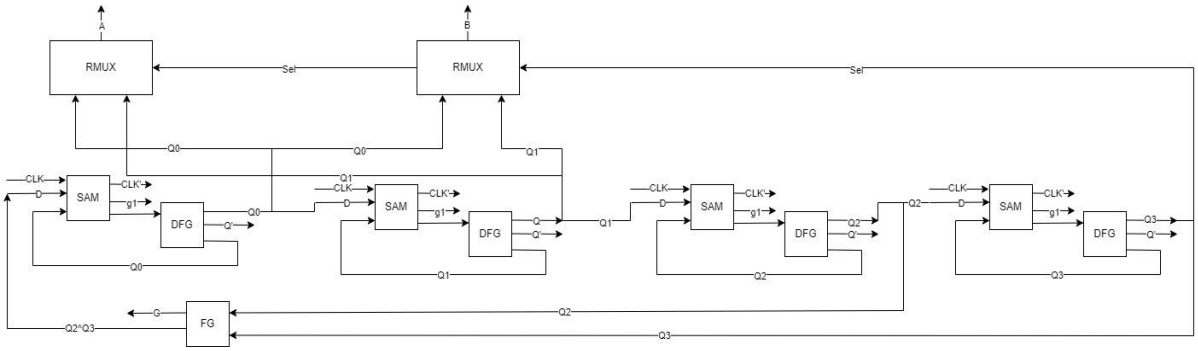


Fig.4. Proposed Reversible BS-LFSR Architecture

4.1.2 8-bit BIST Architecture with Reversible BS-LFSR

Our work introduces an innovative approach to optimize the power efficiency of BIST (Built-In Self-Test) controllers. We implement a novel reversible Bit Swapping Linear Feedback Shift Register (BS-LFSR). Our design uses reversible logic gates - Sam Gate, Feynman Gate, and RMUX Gate - to form the core of the BS-LFSR. This enhances the traditional BIST controller framework, which includes the Controller, Circuit Under Test (CUT), Response Analyzer, Comparator, Multiple Input Signature Register (MISR), Memory, Multiplexer (Mux), Demultiplexer (De-Mux), and LFSR. Our architecture significantly reduces power consumption by leveraging reversible logic, as shown in Figure 5. This is a critical consideration in today's energy-conscious electronics industry.

The reversible BS-LFSR is designed to be scalable across various system sizes, including 8-bit, 16-bit, and 32-bit BIST controllers. This ensures broad applicability in digital circuit testing. The system has been simulated and synthesized using Xilinx tools, demonstrating its feasibility and efficiency.

Furthermore, we implemented the design using 180nm Technology and analyzed it using Cadence and open-source EDA tools. This provides a comprehensive evaluation of power, area, and timing metrics. The review

underscores the design's potential to contribute significantly to the advancement of low-power, efficient testing methodologies in semiconductor technologies.

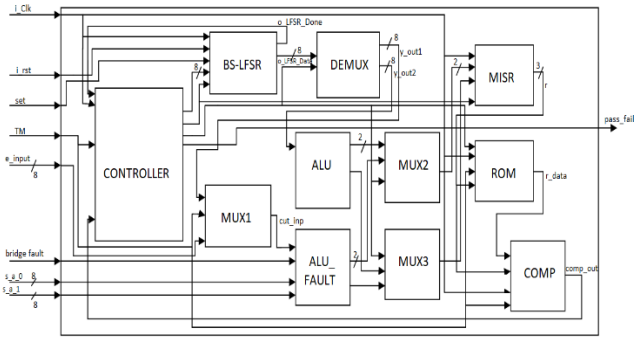


Fig.5. Overall Proposed 8-bit BIST architecture

The data presented in Table 1 compares three different architectures of 8-bit BIST (Built-In Self-Test) Controllers. One uses a reversible Bit-Swapping Linear Feedback Shift Register (BS-LFSR), while the other uses conventional BS-LFSR and LFSR designs. The key performance metrics are power consumption, pre and post-synthesis delays, and circuit area.

Table 1. 8-bit BIST Controller Comparison

Architecture	Power (Watts)	Pre-Synthesis Delay(ns)		Post-Synthesis Delay(ns)		Area (um^2)
		Max Delay	Min Delay	Max Delay	Min Delay	
8-bit BIST Controller with reversible BS-LFSR	1.183	1.017	0.376	1.739	0.336	53.76*52.3
8-bit BIST Controller with Conventional BS-LFSR	1.398	1.008	0.274	1.020	0.277	53.2*51.3
8-bit BIST Controller with Conventional LFSR	1.427	0.820	0.266	0.827	0.269	54.96*52.3

Power Consumption:

- The integration of reversibility into the BS-LFSR reduces power consumption to 1.183W, outperforming conventional BS-LFSR and LFSR designs. This indicates the potential for more power-efficient BIST controllers.

Delay:

- The reversible BS-LFSR has a slightly longer pre-synthesis delay than conventional designs, with a maximum delay of 1.017 ns. This suggests that there may be a trade-off between power efficiency and initial speed.

- Interestingly, the reversible BS-LFSR exhibits a significantly longer post-synthesis delay than its conventional counterparts, with a maximum delay of 1.739 ns. This could be due to the increased complexity introduced by reversible logic, which may result in longer critical paths in the synthesized design.

Area:

- The area occupied by the reversible BS-LFSR design (53.7652.3 um^2) is slightly larger than that of the conventional BS-LFSR (53.251.3 um^2) but smaller than the traditional LFSR (54.96*52.3 um^2). This suggests that the reversible design does not significantly impact the physical footprint of the BIST controller compared to conventional designs.

Integrating reversible logic into the 8-bit BIST controller design of BS-LFSR holds significant promise for reducing power consumption in energy-efficient electronics. However, this benefit comes at the expense of increased delays, particularly after synthesis, implying a trade-off between power efficiency and speed. The area requirements of the reversible BS-LFSR is similar to traditional designs, indicating minimal impact on the physical size.

4.1.3 BIST Controller with Reversible BS-LFSR Comparison

Table 2 contains data on three BIST Controller architectures with different bit sizes: 8-bit, 16-bit, and 32-bit. Metrics for comparison include power consumption, pre- and post-synthesis delays, and area.

Table 2. BIST Controller with Reversible BS-LFSR Comparison

Architecture	Power(Watts)	Pre-Synthesis Delay(ns)		Post-Synthesis Delay(ns)		Area (um^2)
		MAX DELAY	MIN DELAY	MAX DELAY	MIN DELAY	
8-bit BIST Controller	1.142	1.017	0.376	1.739	0.336	53.76*52.3
16-bit BIST Controller	2.172	1.115	0.374	1.140	0.383	73.28*69.3
32-bit BIST Controller	4.042	1.196	0.367	1.282	0.372	237.6*223

- It is observed that as the bit size increases, the power consumption also increases. For instance, the 8-bit design consumes 1.142 Watts, while the 32-bit design consumes 4.042 Watts. This trend is expected, as more significant BIST controllers typically require more resources and power.

- The maximum delays before synthesis slightly increase with bit size, but not significantly. This suggests that initial design complexity does not drastically alter with bit size. The minimum delays before synthesis are stable across varying architectures, indicating a consistent lower bound in operational speeds. These observations imply that initial design variations due to bit size do not significantly impact performance metrics.

- The 32-bit design has a lower maximum delay of 1.282ns despite its more prominent architecture, suggesting more effective optimization. The minimum delays increase slightly with complexity, but optimization processes remain robust, ensuring consistent operational speed.

As expected, the area required for the BIST controllers significantly increases with the bit size, directly reflecting the increased circuit complexity and functionality in larger designs. As BIST controller's designs become more significant, they require more power and space. However, modern synthesis and optimization advancements can

effectively counteract potential delays in operation. Maintaining a balance between power, space, and time is crucial when creating efficient testing mechanisms for advanced integrated circuits. Future BIST controller research should aim to refine this balance, using innovative design approaches, improved synthesis algorithms, or new architectures to enhance efficiency in more extensive systems without affecting their function or power efficiency.

4.1.4 BIST Controller with Fault Detection

A "stuck-at fault" is a type of fault model used in digital circuit testing to simulate a common failure where a digital signal is fixed at a logical high(1) or low (0), regardless of the input to the circuit. This model helps identify potential points of failure within an integrated circuit (IC) or any digital system.

Stuck-at Fault Model

Definition: It assumes that a digital circuit's wire or pin is permanently set to a logical '1' (stuck-at-1) or '0' (stuck-at-0), disregarding its expected behavior based on the given inputs.

Application: This model is extensively used in testing and fault diagnosis of digital circuits to ensure reliability and proper functionality. It simplifies the detection of manufacturing defects that cause such permanent faults.

Detection: Test patterns are generated and applied to the circuit to check if the output matches the expected result. A discrepancy indicates the presence of a fault.

Bridging Faults

Bridging faults occur when two or more circuit nodes that are not supposed to be electrically connected end up being shorted together due to a manufacturing defect or physical damage. This can lead to unpredictable behavior as the logical values of the bridged nodes can affect each other, often leading to a situation where the circuit output does not correspond to the expected logic for any given set of inputs. Unlike stuck-at faults, which are relatively straightforward to model and test for, bridging faults can be more complex due to the numerous potential short-circuit combinations and their varied impact on circuit behavior. Testing for bridging faults often requires sophisticated fault models and testing strategies to cover the range of possible fault conditions adequately.

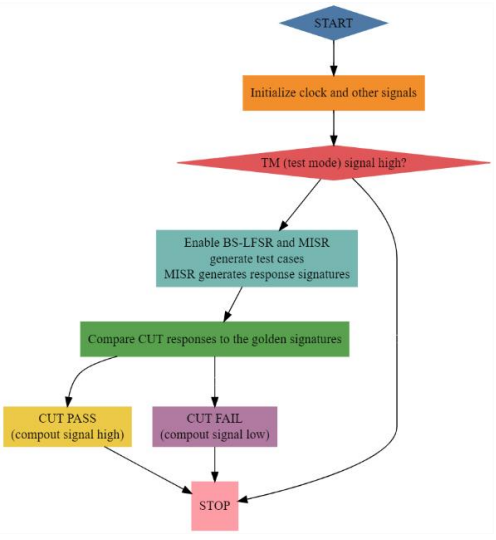


Fig. 6. Flowchart for Fault detection in CUT

This process outlines a sequence for conducting a Built-In Self-Test (BIST) using a Reversible Bit Swapping Linear Feedback Shift Register (BS-LFSR) and Multiple Input Signature Register (MISR). It initializes necessary signals and then checks if the system is in test mode. If in test mode, the BS-LFSR generates test patterns, and the MISR captures the output responses. These responses are compared to pre-defined correct responses (golden signatures). If the output matches the golden signature, the system indicates a PASS (compost signal high); if not,

it suggests a FAIL (compost signal low), concluding the BIST cycle shown in Figure 6. This method allows for automated, efficient system functionality testing and fault detection.

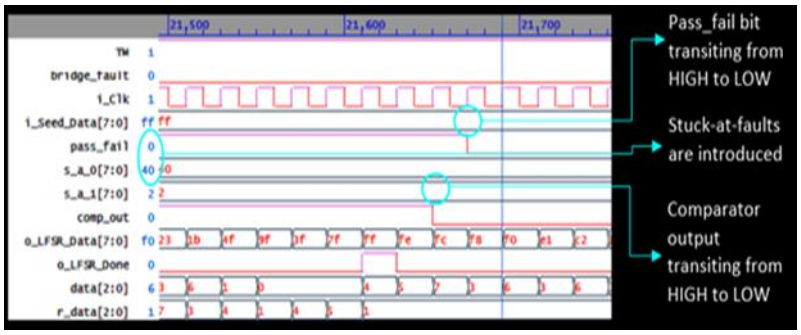


Fig. 7. 8-bit BIST Controller without faults

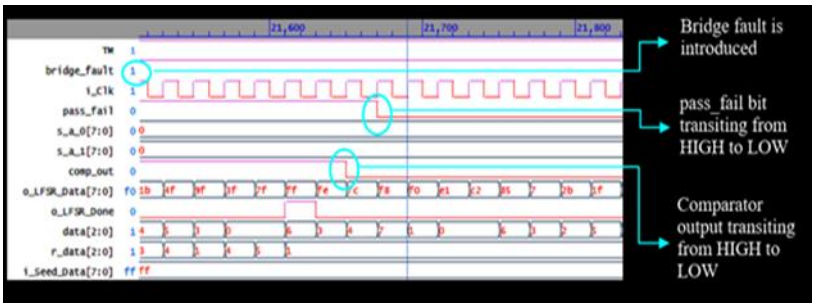


Fig. 8. 8-bit BIST Controller with stuck-at-fault

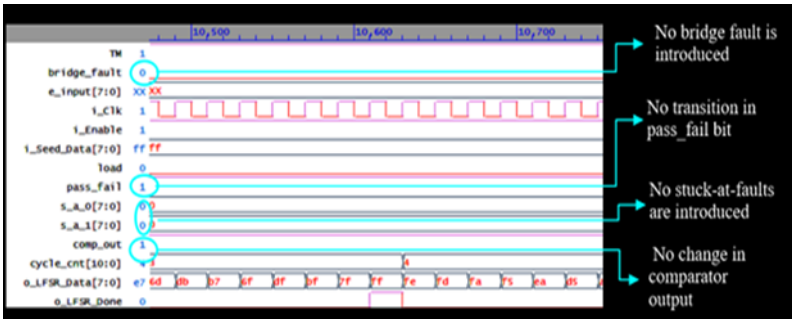


Fig. 9. 8-bit BIST Controller with bridge fault

Figures 7, 8, and 9 show the simulation results for fault detection for stuck-at-fault and bridging fault for 8-bit BIST Controller and Arithmetic Logic Unit(ALU) as Circuit Under Test(CUT).

Similarly, simulations were performed for 16-bit and 32-bit BIST Controller and Arithmetic Logic Unit(ALU) as Circuit Under Test(CUT).

4.1.5 Scalable BIST Architecture with Reversible BS-LFSR

The Scalable BIST Architecture with Reversible BS-LFSR shown in Figure 10 is a significant advancement in digital circuit testing. This architecture combines the principles of reversible logic with the efficiency and adaptability of Built-In Self-Test (BIST) systems. By incorporating a Reversible Bit Swapping Linear Feedback Shift Register (BS-LFSR), this architecture aims to reduce power consumption during testing, a crucial challenge in modern electronic design. The scalable nature of this architecture enables it to be applied across various digital systems, from tiny IoT devices to complex processors, providing a tailored and energy-efficient testing solution. This innovation promises to improve the sustainability and reliability of digital systems by offering more efficient and comprehensive testing processes.

Final System Architecture

In the Built-In Self-Test (BIST) Controller, a range of modules work in concert to automate the testing of digital circuits for faults. Below is a brief overview of these critical components and their roles within the BIST framework:

LFSR (Linear Feedback Shift Register)

- **Purpose**: Acts as a test pattern generator.
- **Functionality**: The Reversible BS-LFSR generates sequences of test patterns. For instance, an 8-bit LFSR produces 256 sequences, a 16-bit LFSR generates 65,535 sequences, and a 32-bit LFSR can produce approximately 4.29 billion sequences. These sequences are used as test cases for the Circuit Under Test (CUT) of corresponding bit sizes.

MISR (Multiple Input Shift Register)

- **Role**: Serves as a response analyzer and signature generator.
- **Operation**: MISR collects the output from a fault-free CUT to construct reference responses or "golden signatures," which are stored for comparison against the output from the CUT under test conditions.

CUT (Circuit Under Test)

- **Description**: The digital design is being tested for logical faults.
- **Indicator**: A "comp out" signal indicates the health of the CUT; a low signal suggests a fault.

Response Analyzer

- **Task**: Generates reference responses, also known as golden signatures.
- **Process**: Uses sequences generated by the BS-LFSR applied to a fault-free CUT. The output is then fed into the MISR to create golden signatures, which are saved for later comparisons.

Memory

- **Function**: Stores golden responses for comparison against the CUT's output to determine the presence of faults.

Controller

- **Responsibilities**: Manages the operation of the BS-LFSR and MISR based on the test mode signal. It initiates test sequence generation and analysis when the test mode is active and ensures the CUT usually operates when the test mode is inactive.

Comparator

- **Activity**: Compares the responses from the CUT against stored golden signatures to ascertain the CUT's integrity. A match indicates a fault-free CUT, while a discrepancy signals a potential fault.

This overview encapsulates the cooperative function of various modules within a BIST controller, highlighting the system's capacity to autonomously identify and signal faults in digital circuits, enhancing reliability and efficiency in electronic systems testing.

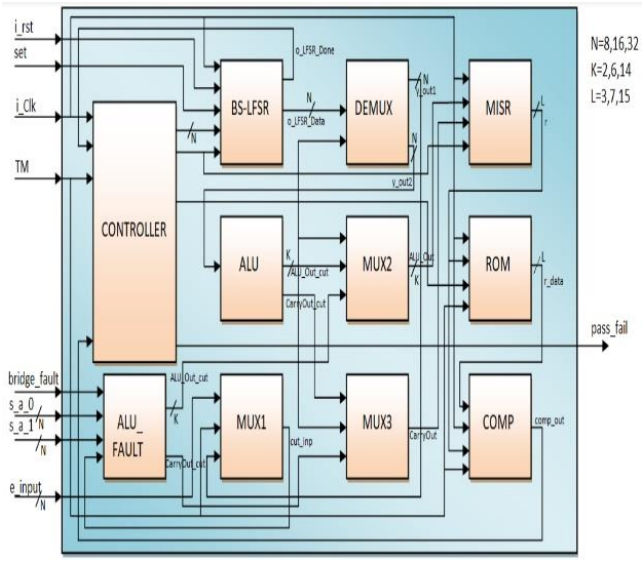


Fig. 10. Scalable BIST Architecture with Reversible BS-LFSR

Analysis of the Scalable BIST Architecture with Reversible BS-LFSR in backend flow using Cadence is shown below.

Timing Analysis

Timing analysis is a critical step in designing and developing digital integrated circuits (ICs), ensuring that the circuit meets the required performance specifications and operates reliably under all conditions. Using Cadence tools, timing analysis is typically conducted at two significant stages of the design process: pre-synthesis and post-synthesis.

Pre-Synthesis timing analysis

The primary goal is to estimate the timing based on generic or estimated models. The exact gate-level details are unavailable at this stage, so the analysis uses ideal or estimated delays for standard cells.

```
====================================================
  Generated by:           Genus(TM) Synthesis Solution 17.22-s017_1

  Module:                 controller
  Technology library:     tsmc18 1.0
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================

             Pin                        Type       Fanout Load Slew Delay Arrival
                                                     (fF) (ps) (ps)  (ps)
-----------------------------------------------------------------------------------
(clock i_Clk)                           launch                                5000 F
(create_clock_delay_domain_1_i_Clk_F_0) ext delay                    +0       5000 F
i_Clk                             (i)   in port        16  0.0     0   +0       5000 F
genblk1.l1_as1/a (i)
  g28/S0                                                             +0       5000
  g28/Y                                 MX2X1           1  1.7    78 +175       5175 F
genblk1.l1_as1/r
genblk1.l1_T_reg[0]/D                <<< SDFFTRX1                    +0       5175
genblk1.l1_T_reg[0]/CK                    setup                   100 +722       5896 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock i_Clk)                           capture                              10000 R
                                        uncertainty              -10         9990 R
-----------------------------------------------------------------------------------
Cost Group   : 'i_Clk' (path_group 'i_Clk')
Timing slack :    4094ps
Start-point  : i_Clk
```

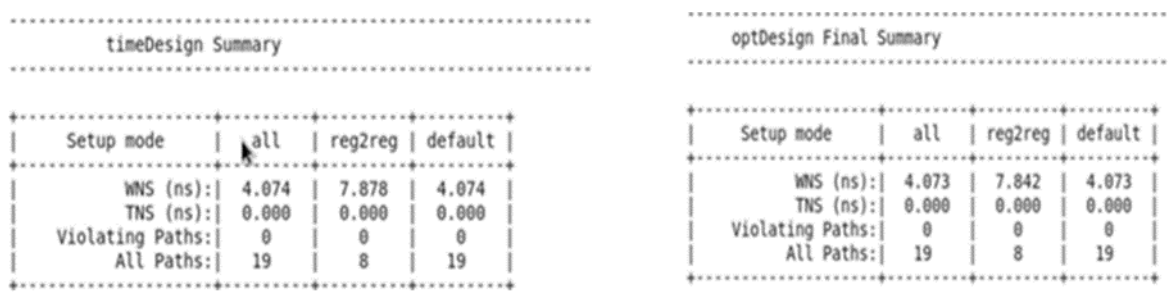
Fig. 11. Pre-Synthesis timing analysis

Figure 11 shows the pre-synthesis timing analysis for the scalable BIST architecture with reversible BS-LFSR and the positive slack, indicating no timing violations. The pre-synthesis timing analysis helps make architectural decisions, optimize the RTL design, and set realistic timing constraints for synthesis.

Post-Synthesis timing analysis

After synthesis, the design is transformed from RTL code to a gate-level netlist, which includes specific logic gates and connections based on the target technology library.

After synthesis, more detailed timing information becomes available, allowing for a more accurate analysis. The post-synthesis timing considers the standard cells used, their placements, and the routed wires' physical characteristics.



timeDesign Summary

Setup mode	all	reg2reg	default
WNS (ns):	4.074	7.878	4.074
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	19	8	19

optDesign Final Summary

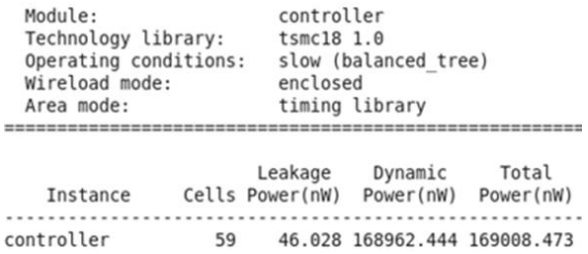
Setup mode	all	reg2reg	default
WNS (ns):	4.073	7.842	4.073
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	19	8	19

Fig. 12. Post-Synthesis timing analysis

Figure 12 shows the post-synthesis timing analysis for the scalable BIST architecture with reversible BS-LFSR critical paths identified, slack times analyzed to ensure no violations occur, and more detailed timing information becomes available, allowing for a more accurate analysis.

Power Analysis

Power analysis in the Cadence design environment is crucial for understanding and optimizing the energy consumption of integrated circuits (ICs), especially in today's market, where power efficiency is a significant concern. Cadence provides several tools and methodologies for power analysis, targeting different stages of the IC design process.



Module: controller
Technology library: tsmc18 1.0
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
controller	59	46.028	168962.444	169008.473

Fig. 13. Power Analysis

Figure 13 shows the power analysis for the scalable BIST architecture with reversible BS-LFSR, which provides the leakage and dynamic power in the design.

Throughout the design process, power analysis in Cadence enables designers to understand, predict, and optimize the power consumption of ICs, leading to more energy-efficient and reliable products. It's a multi-stage process, with each phase providing deeper insights and guiding optimizations to meet the stringent power requirements of modern electronic devices.

Area Analysis

After the synthesis process, the tool provides a more accurate area report. This report is based on the synthesized design's standard cells selected from the Technology Library. The report includes information on the cell area, total gate area, and the estimated interconnect area.

```
  Technology library:     tsmc18 1.0
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
==========================================


  Gate    Instances    Area    Library
------------------------------------------
AOI221X1          7   162.994    tsmc18
AOI22X1           7   116.424    tsmc18
AOI22XL           1    16.632    tsmc18
DFFHQX1           7   372.557    tsmc18
INVX1             2    13.306    tsmc18
INVXL            16   106.445    tsmc18
MX2X1            14   372.557    tsmc18
NOR2X1            1     9.979    tsmc18
SDFFTRX1          1    73.181    tsmc18
XOR2X1            3    79.834    tsmc18
------------------------------------------
total            59  1323.907
```

Fig. 14. Area Analysis

Figure 14 shows the power analysis for the scalable BIST architecture with reversible BS-LFSR cell area, total gate area, interconnect area, library, and gate instances.

Physical View

The "Physical View" refers to the representation and visualization of the physical layout of an integrated circuit (IC). This view is crucial for understanding how the design will be physically implemented on silicon and is used extensively during the physical design phase of IC development.

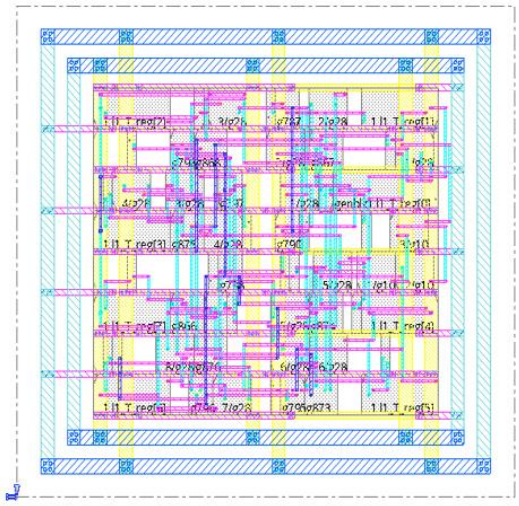


Fig. 15. Physical view of scalable BIST architecture with reversible BS-LFSR

The physical view is essential for ensuring the IC design meets all physical, electrical, and manufacturing requirements. It allows designers to directly interact with the layout, identify potential issues, and apply necessary optimizations, all of which are critical for the successful fabrication of the chip.

In summary, the Physical View in Figure 15 Cadence provides a comprehensive and detailed representation of the IC layout, serving as a critical tool for designers in ensuring the design's manufacturability, performance, and reliability.

V. CONCLUSION AND FUTURE WORK

The extensive analysis underscores the inherent trade-offs present in BIST controller architectures, particularly between power efficiency, speed, and physical size across varying bit configurations. While more significant BIST controllers offer enhanced functionalities, they also demand higher power and occupy more space, posing significant design challenges. However, advancements in reversible logic, like the reversible BS-LFSR, offer promising avenues for mitigating power consumption without severely impacting operational speed, although they introduce synthesis complexities.

The study indicates that while increasing the bit size of BIST controllers introduces initial design complexities, it does not disproportionately affect core performance metrics, thanks to scalable post-synthesis optimizations. The transition to more extensive and complex BIST architectures remains challenging yet feasible with continuous optimization and advanced synthesis techniques.

Future research should focus on balancing performance with power efficiency, exploring innovative reversible logic designs, and refining synthesis processes to develop BIST controllers that align with modern electronic systems' growing complexity and stringent requirements. Ultimately, the aim is to create efficient, effective, and sustainable BIST solutions that address the current and future demands of the electronics industry.

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CONFLICTS OF INTEREST

The authors have no conflicts of interest to declare.

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