[1] S Farook
[2] Samat Iderus
[3] P. Jamuna
[4] R. Sankar Ganesh
[5] Panneer Selvam
[6] Piyush Kumar Yadav

Performance Characteristics of a Newly Developed Asymmetric Seven-Level Inverter Utilizing Various Hybrid Pulse Width Modulation Strategies

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Abstract: - This study unveils a notable breakthrough in inverter technology, holding promise for substantial improvements in voltage quality and the attenuation of harmonic distortions within power systems. This study concentrates on the design and implementation of a novel Seven-Level Asymmetric Inverter (NSLAI) by incorporating various hybrid Pulse Width Modulation (PWM) techniques. The primary goal is to improve the output voltage magnitude while decreasing the Total harmonics compared to conventional PWM methods.
The investigation introduces a novel Seven-Level Asymmetric Inverter (NSLAI) with innovative Hybrid Pulse Width Modulation (PWM) strategy. The purpose of this study is to investigate the distinct features of a recently developed asymmetric seven-level inverter, with a focus on exploring its characteristics through the implementation of diverse hybrid pulse width modulation strategies. Hybrid PWM methodology intricately centers on enhancing voltage quality and achieving better harmonious spectral characteristics. The gate signal producing approach for this suggested PWM technology incorporates a hybrid PWM methodology that combines trapezoidal and sinusoidal waveforms, as well as a standard triangular carrier signal enabling NSLAI. The hybrid version of PWM practices is deliberately used to generate switching signals for the NSLAI. An intensive evaluation of numerous indicators of effectiveness across multiple modulation indexes leads in the demonstrating of quantitative findings that compare the unique Hybrid PWM practice with established PWM tactics. Notably, the hybrid reference Carrier Overlapping strategy has emerged as a leading approach surpassing conventional pulse width modulation techniques. It achieves a significantly higher fundamental Root Mean Square voltage output and remarkably lower percentage of Total Harmonic Distortion values compared to all within the hybrid reference Variable Frequency strategy. The principal analytical tool used in the modeling investigation is MATLAB-SIMULINK. This study marks a watershed moment in the development of inverters, claiming significant improvements in battery power quality and distortion caused by harmonics avoidance across power systems, as evidenced by extensive simulation and prototype-based discoveries.

Keywords: Hybrid pulse width modulation, seven-level asymmetric inverter, sinusoidal pulse width modulation, total harmonic distortion.

I. INTRODUCTION

The primary function of a Multilevel Inverter (MLI) lies in the synthesis of a desired AC output voltage by ingeniously amalgamating several DC voltage sources while maintaining an exceedingly low distortion profile. MLIs exhibit the remarkable capability to deliver high output voltages with minimal harmonic content, all without the need for transformers or a series of synchronized switching devices. The advantages offered by MLIs are manifold. Multilevel inverters have emerged as a pivotal development, particularly in the realm of medium voltage and high-power applications, thanks to their proficiency in shaping waveforms with an improved harmonic spectrum. The term "multilevel inverters" refers to inverters capable of producing output voltages that encompass more than the standard two voltage levels relative to the pole. This unique feature, which yields an output voltage level surpassing the ratings of the power semiconductor switching devices, firmly situates MLIs within the high-power inverter category. Moreover, the application domain of MLIs has expanded into the medium-power range due to their inherent advantages, which encompass reduced distortion, [1]. However, it is not without limitations, primarily the requirement for a considerable number of switches [2]. To circumvent these challenges, involving the cascading of smaller, dissimilar inverter circuits [3]. In one instance [4], a novel transformer-based cascaded multilevel inverter is outlined, capable of operating in both symmetric and asymmetric configurations. Additionally, a seven-level inverter utilizing series/parallel

[1] Department of Electrical and Electronics Engineering, Mohan Babu University (Formerly Sreevidyanikethan Engineering College), India
[2] *Corresponding author: CRISD, School of Engineering and Technology, University of Technology Sarawak, Malaysia
samat.iderus@uts.edu.my
[3] Department of Electrical and Electronics Engineering, Nandha Engineering College, Erode, India
[4] Department of Electrical and Electronics Engineering, K.S.R. College of Engineering, Tiruchengode, India
[5] Department of Electrical and Electronics Engineering, Sona College of Technology, Salem, India
[6] Department of Electrical Engineering, Netaji Subhas University of Technology, India

conversion with fewer switching devices than conventional multilevel inverters is proposed in [5]. Furthermore, an approach detailed in [6] achieves a higher number of levels without increasing the number of voltage sources by employing a specific switching sequence of non-equal voltage sources, with gating signals generated through comparison with modulating and carrier waves [7]. In the domain of PWM techniques employed in inverters, the choice between unipolar and bipolar types is crucial, with unipolar switching being favored for its capacity to produce superior waveform quality compared to bipolar switching [7]. Various advanced modulating techniques are introduced in [8], and a trapezoidal PWM scheme for single-phase multilevel inverters is proposed in [9]. The concept of trapezoidal amalgamated rectangular reference-based unipolar PWM is explored for enhanced multilevel inverter performance in [10], while [11] delves into PD modulation strategies rooted in multilevel inverters, even presenting an Field Programmable Gate Arrays (FPGA) based implementation with optimized PWM switching patterns. In a cascaded multilevel inverter, the DC voltages across each cell are usually equal, but asymmetric multilevel inverters can have varying voltage levels among the cells, leading to increased voltage levels without a proportional increase in H-bridge cells. This can be further enhanced through the use of hybrid switching, where a subset of switches is triggered at high-frequency PWM, while others operate at a lower or fundamental frequency [12]-[16]. However, traditional PWM techniques having some limitation Research in this field has given rise to novel inverter topologies and distinctive modulation schemes. As highlighted in existing literature, recent Multilevel Inverter (MLI) structures encounter pivotal challenges such as the extensive use of power semiconductor devices, DC input sources, capacitors, complex control methodologies, and an increased number of on-state switches, leading to elevated losses. Conversely, as the number of levels in the MLI increases, so does its complexity. This research is dedicated to the development of a novel Seven-Level Asymmetric Inverter (NSLAI) that mitigates these challenges by utilizing fewer semiconductor switches and adopting an Asymmetric sequence (1:2) of DC sources. The proposed MLI configuration detailed in this article employs a 1:2 sequence of DC sources to achieve higher voltage levels with a reduced number of key switching elements. A key aspect of this setup is its capability to generate resultant voltage levels through all possible combinations of DC supplies. This research work investigates the distinct features of a recently developed asymmetric seven-level inverter, with a focus on exploring its characteristics through the implementation of diverse hybrid pulse width modulation strategies.

To this end, four distinct unipolar multi-carrier PWM strategies, namely Phase disposition PWM (PDPWM), Alternate phase opposition and disposition PWM (APODPWM), carrier overlapping PWM (COPWM), and Variable Frequency PWM (VFPWM) are thoroughly investigated and analyzed. These strategies utilize sinusoidal and hybrid references and are implemented using MATLAB-SIMULINK and a laboratory model for a selected NSLAI.

II. New Seven-level Asymmetric Inverter

A. Selecting a Template (Heading 2)

This template has been tailored for output on the US-letter paper size. If you are using A4-sized paper, please close this template and download the file for A4 paper format called “CPS_A4_format”. These innovative Asymmetric MLIs serve as viable alternatives for mitigating the undesirable harmonic distortions in the output voltage, all while adeptly circumventing the need for an increased number of power devices. The introduction of hybrid asymmetrical multilevel inverters serves to streamline the complexity of inverter topologies across various applications, resulting in a reduction in the quantity of switching devices and the curtailment of circulating energy within interconnected cells. Comparatively, when juxtaposed with the conventional H-bridge cascade multilevel inverter, the single-phase hybrid asymmetrical multilevel inverter markedly reduces the overall count of isolated DC sources and semiconductor switches. In Fig. 1, we are presented with the envisioned configuration of the NSLAI, where the judicious manipulation of switches S1 to S3, A1, A2, B1, and B2 allows for the precise generation of the desired load voltage. The accompanying Table 1 offers a detailed portrait of the switching patterns and their corresponding output voltages. It is discernible that the pairs A1-A2 and B1-B2 are orchestrated to operate complementarily, thereby yielding negative and positive voltages, respectively.

Simultaneously, switches S1 to S3 follow a well-conceived modulation pattern, aligning to generate the intended load voltage. Consequently, the inverter depicted in Fig. 1 represents a seven-level single-phase inverter, where switches S1 to S3 operate at a high frequency and are rated for half of the DC-link voltage, while switches A1, A2, B1, and B2 are rated for the full DC-link voltage. Table 1 provides the essential switch configurations that create every voltage stage, and these states are cautiously controlled by creating the required voltage ranges.

Based on this strategy, the proposed inverter is an asymmetric (unequal DC sources) hybrid (multi-carrier frequencies) multilevel inverter. Based on this strategic configuration, the proposed inverter emerges as an asymmetric entity, given its unequal DC sources, and a hybrid system, denoting the presence of multiple carrier frequencies within its operational framework.

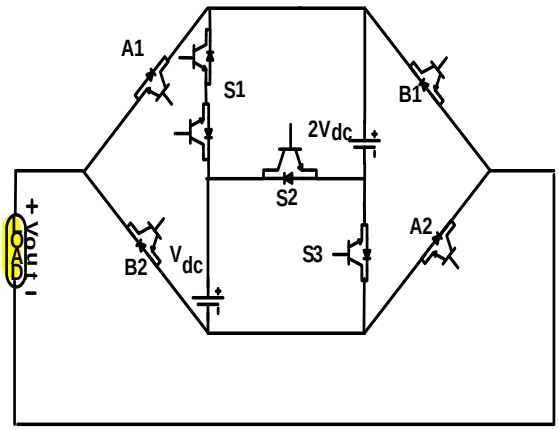
From the Fig. 1 (b), When S1and pairs A1 and A2 are turned ON, the output voltage becomes +Vdc, and then S3 and pairs A1 and A2 are switched ON to produce +2Vdcas an output voltage. S2 and pairs A1 and A2 are turned ON to make output voltage as +3Vdc. When A1and B2 are turned ON, the output voltage becomes 0Vdc, similarly 0Vdc is obtain by turning on switches A2 and B2. Then Vout becomes −Vdc by turning ON S1 and pairs B1 and B2. To synthesize −2Vdc as the output voltage, S3 and pairs B1 and B2 are turned ON. S2 and pairs B1 and B2 are turned ON to make an output voltage −3Vdc.

III. HYBRID - MULTICARRIER PWM STRATEGY (H-MCPWM).

A hybrid multicarrier modulation strategy combines fundamental frequency switching for high-power cells and MCPWM control for low-power cell switching at higher frequencies. With this modulation strategy, the effective spectral response of the output depends on the low-power cell switching while the overall voltage generation is decided by the voltage rating of the higher power cell [13]. Figure 2 illustrates the utilization of a rectified sinusoidal, trapezoidal reference waveform, and triangular carrier to generate NSLAI firing pulses. Implementing and synchronizing these two waveforms necessitates intricate control algorithms and methodologies. However, this hybrid PWM approach streamlines the process by employing only three NSLAI-specific carriers, thereby enhancing efficiency. Despite operating at the same frequency, these carriers possess varying maximum magnitudes. Notably, the reference waveform is intentionally positioned above the zero-time line, enabling continuous comparison with each carrier signal. As the modulating waveform surpasses the amplitude of the carrier signal, driving pulses are generated accordingly. Through adept utilization of logical circuits, these initial driving pulses are meticulously processed to yield precise firing pulses for the NSLAI. Our investigation delves into various PWM approaches, including Phase Disposition (PD), Alternate Phase Opposition and Disposition (APOD), Carrier Overlapping (CO), and Variable Frequency (VF) Level-Shifted PWM. Each of these methodologies significantly influences the performance and behavior of the NSLAI, enriching and expanding the scope of our research. Several CFDs exist in H-MCPWM strategies for NSLAIs. The following sections involve CFDs on references. This research presents two types of references (sinusoidal and Hybrid reference) for unipolar PDPWM, APODPWM, COPWM, and VFPWM strategies. Hybrid reference is the combination of sinusoidal and trapezoidal reference. For an m-level inverter using unipolar H-MCPWM, (m-1)/2 carriers with the same frequencies f_c and same peak-to-peak amplitude Ac are used. The reference waveform as amplitude Am and frequency fm and it is centered above the zero level. Implementing a hybrid modulation strategy may introduce additional control overhead. Coordinating the switching between fundamental frequency and MCPWM, along with the generation of firing pulses, can increase computational requirements and may impact the real-time responsiveness of the system.

Table 1
Switching Position

Switches							Vout
S1	S2	S3	A1	A2	B1	B2	
off	on	off	on	on	off	off	3Vdc
off	off	on	on	on	off	off	2Vdc
on	off	off	on	on	off	off	Vdc
off	off	off	on	off	on	off	0Vdc
off	off	off	off	on	off	on	0Vdc
on	off	off	off	off	on	on	-Vdc
off	off	on	off	off	on	on	-2Vdc
off	on	off	off	off	on	on	-3Vdc



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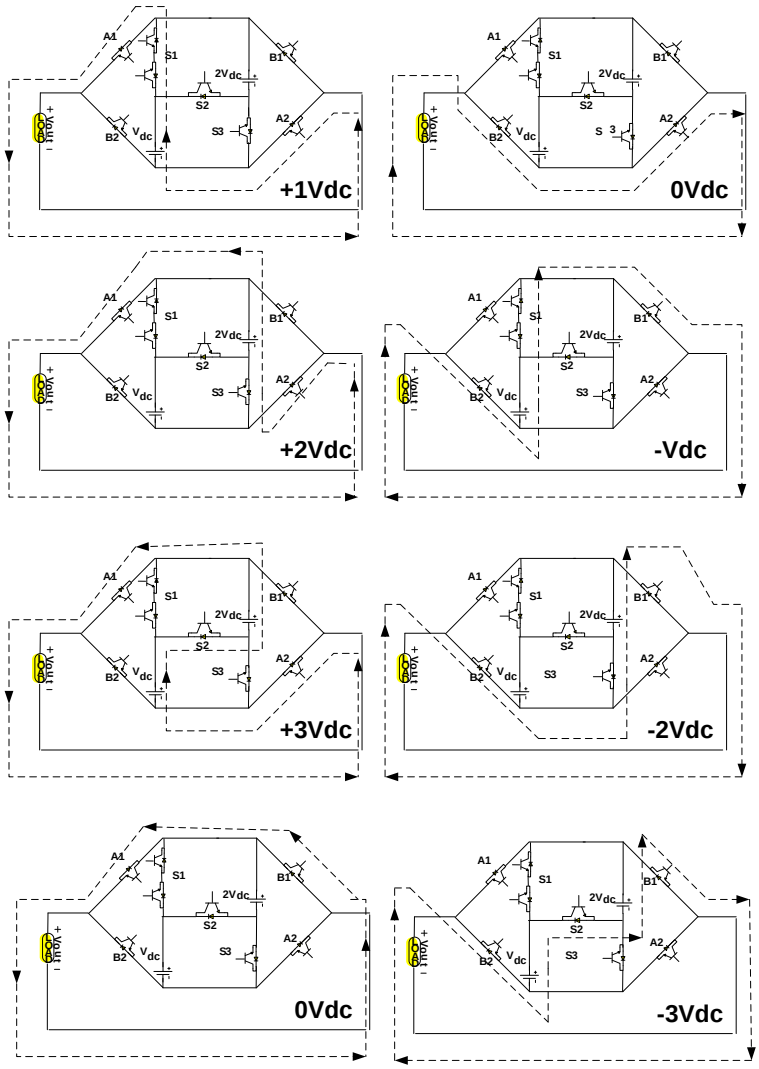


(b)

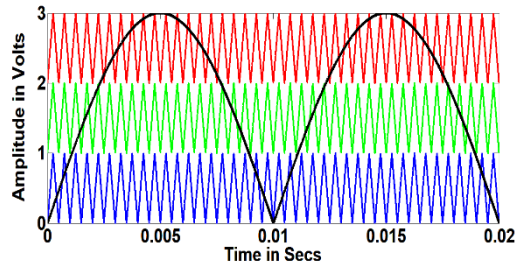
Fig. 1. Proposed (a) New Seven level asymmetric inverter (NSLAI) (b) Current path with each levels

IV. SIMULATION RESULT

The chosen NSLAIs undergo simulation using the SIMULINK-POWER SYSTEM block set [15]. Various simulations are conducted, adjusting the modulation index (ma) within the range of 0.8 to 1, while maintaining a load (RL) of 100 ohms and 50 mH. The simulated output voltage of the selected NSLAIs employing different PWM strategies is showcased specifically for a representative case with ma = 1. The selection of the modulation factor (mf) is made based on a compromise considering two key factors: (i) mitigating switching losses and (ii) minimizing the filter size required for closed-loop control. To achieve this, the filter size is optimized at moderate frequencies.

Additionally, the distortion factor, crest factor, and form factor of the output voltage are computed from the simulation results and tabulated. The simulation employs specific parameter values: Vdc = 100V, RL (load) = 100Ω and 50 mH. The Fast Fourier Transform (FFT) plot and seven-level output voltage and current obtained by the Multi-Carrier Unipolar (MCU) PD (MCU-PD) a PWM approach with a sine reference is exhibited in Figures 3 (a) and (b).

. The RMS voltage is measured at 212.3 V, with harmonic distortion at 17.96%, and 3.19% harmonic content in the resulting current. Figures 4 (a) and (b) illustrate the seven-level output voltage and current generated by the MCU-APODPWM strategy with a sine reference, along with its FFT plot. The RMS voltage is recorded at 212.2 V, with harmonic distortion at 18.21%, and 4.29% harmonic content in the resultant current.



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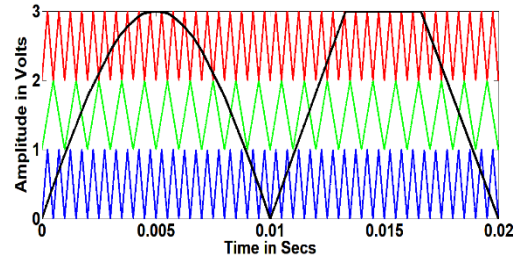

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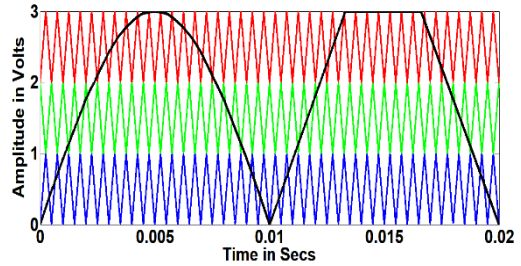

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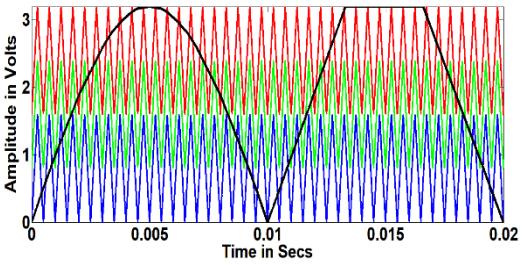

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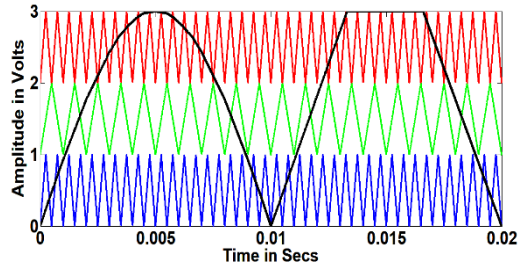
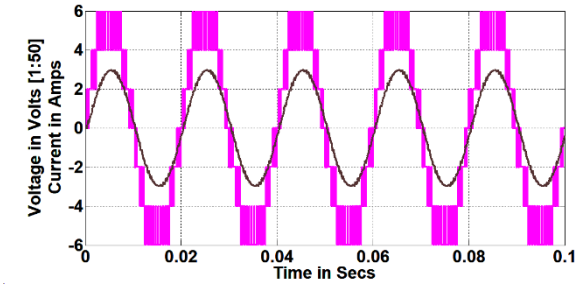


(e)

Fig. 2. The layout of
a) Sinusoidal PWM with PD b) Hybrid PWM with PD c) Hybrid PWM with APOD d) Hybrid PWM with CO e) Hybrid PWM with VF approach

The seven-level results from current and voltage developed by the MCU-COPWM strategy with a sine reference, as well as its FFT plot, are illustrated in Figures 5 (a) and (b). The fundamental voltage peak is 218.2 V, with harmonic distortion at 22.88%, and 5.85%harmonic content in the resulting current. Figures 6 (a) and (b) showcase the seven-level output voltage and current generated by the MCU-VFPWM strategy with a sine reference, along with its FFT plot. The fundamental voltage peak is 212.2 V, with harmonic distortion at 16.74%, and 2.85% harmonic content in the resultant current. Figures 7 to 10 follow a similar pattern, presenting results for various strategies with different reference waveforms and providing RMS values, harmonic distortions, and harmonic content percentages for the output voltage and current in each case.



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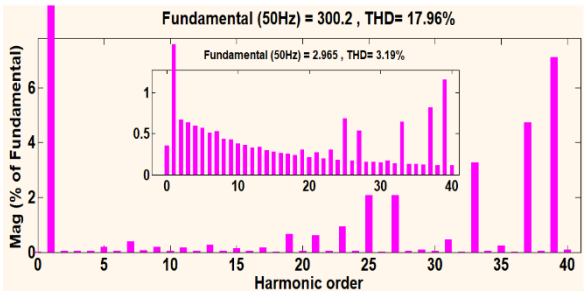
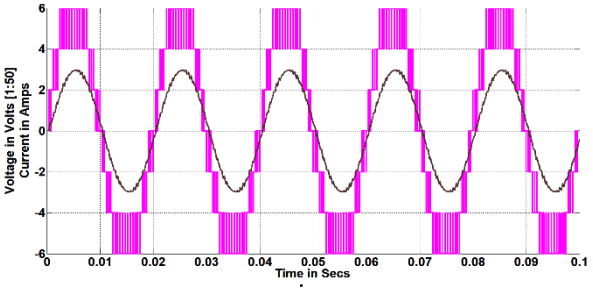


(b)

Fig. 3 The outcomes from the simulation with MCU-PD SPWM (a) the voltage and current waveforms (b) Harmonic band



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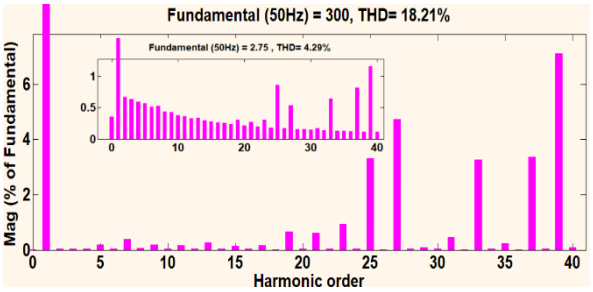
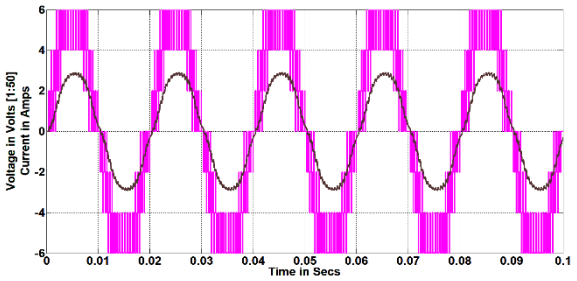


(b)

Fig. 4 The outcomes from the simulation with MCU-APOD SPWM (a) the voltage and current waveforms (b) Harmonic band



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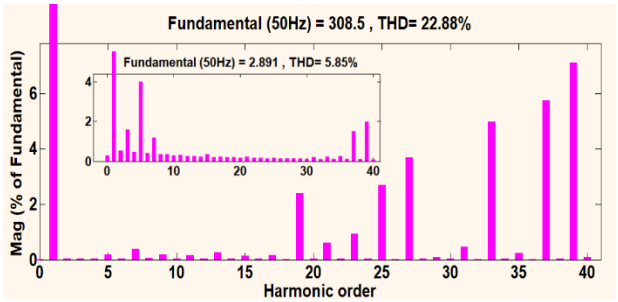

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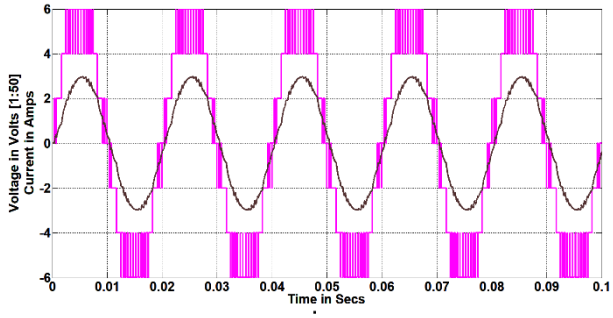
Fig. 5 The outcomes from the simulation with MCU-CO SPWM (a) the voltage and current waveforms (b) Harmonic band



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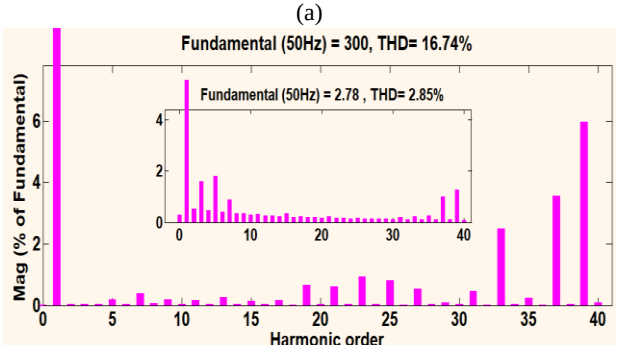
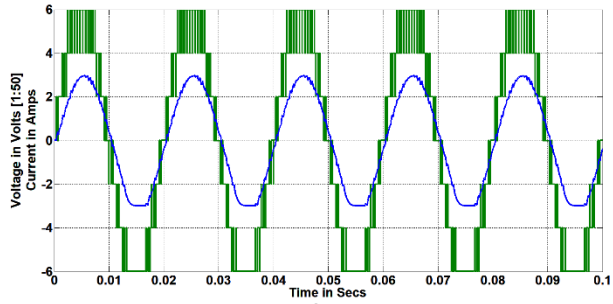


(b)

Fig. 6 The outcomes from the simulation with MCU-VF SPWM (a) the voltage and current waveforms (b) Harmonic band



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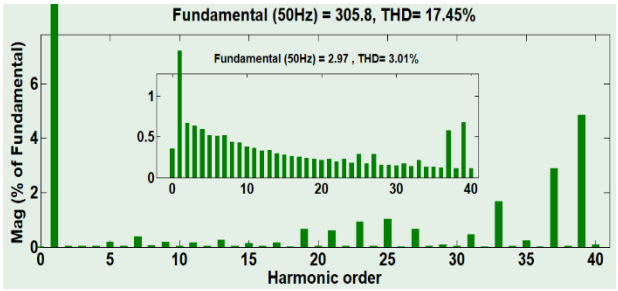

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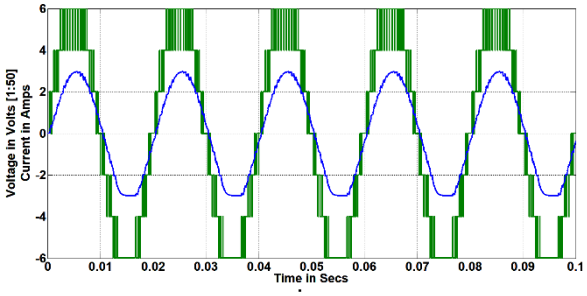
Fig. 7 The outcomes from the simulation with MCU-PD Hybrid PWM (a) the voltage and current waveforms (b) Harmonic band



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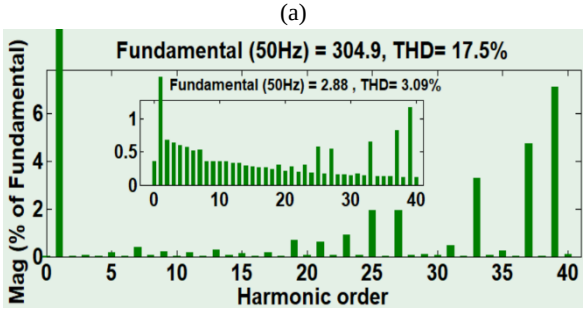
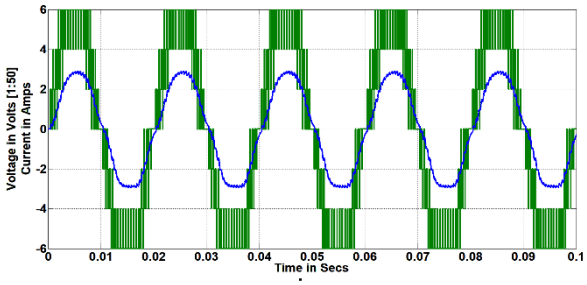


(b)

Fig. 8 The outcomes from the simulation with MCU-APOD Hybrid PWM (a) the voltage and current waveforms (b) Harmonic band



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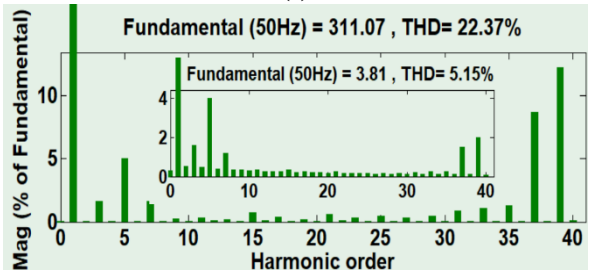

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Fig. 9 The outcomes from the simulation with MCU-CO Hybrid PWM (a) the voltage and current waveforms (b) Harmonic band

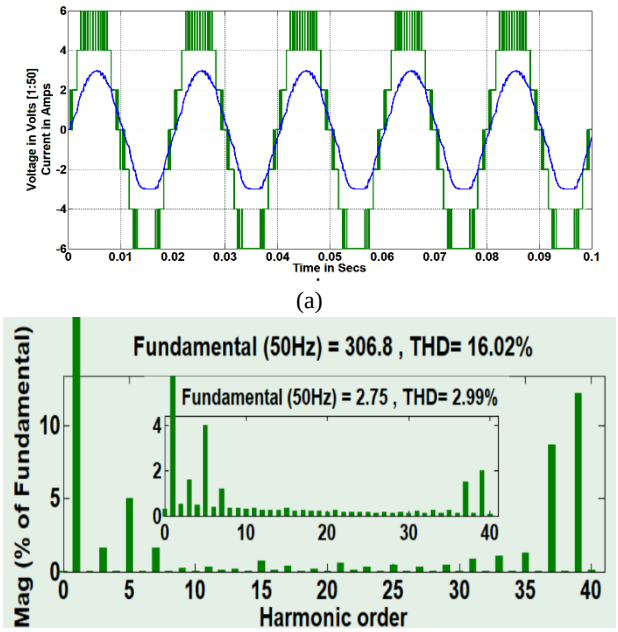

Fig. 10 The outcomes from the simulation with MCU-VF Hybrid PWM (a) the voltage and current waveforms (b) Harmonic band

Table 2
%THD for different modulation indices

ma	Sine Ref.				Hybrid Ref.			
	MCU-PD	MCU-APOD	MCU-CO	MCU-VF	MCU-PD	MCU-APOD	MCU-CO	MCU-VF
1	17.96	18.21	22.88	16.74	17.45	17.5	22.37	16.02
0.95	20.39	20.16	25.15	18.81	20.56	20.63	24.88	21.14
0.9	22.11	22.06	27.53	21.59	21.65	21.88	29.40	20.99
0.85	23.42	23.17	29.8	23.49	29.42	24.36	29.42	24.12
0.8	24.25	24.13	32.25	24.43	25.02	25.11	31.47	24.49

Table 3
V_{RMS} (fundamental) for different modulation indices

m_a	Sine Ref.				Hybrid Ref.			
	MCU-PD	MCU-APOD	MCU-CO	MCU-VF	MCU-PD	MCU-APOD	MCU-CO	MCU-VF
1	212.3	212.2	218.2	212.2	216.3	216	220.4	216.2
0.95	201.4	201.7	209.6	202.3	205.1	205.2	211.4	206
0.9	191.2	191	200.1	191.6	194.6	194.4	202.3	195.4
0.85	180.6	180.4	190.2	180.5	183.8	183.6	192.5	183.9
0.8	169.6	169.7	180	169.8	172.9	172.9	183	173

Table 4
%DF for different modulation indices

m_a	Sine Ref.				Hybrid Ref.			
	MCU-PD	MCU-APOD	MCU-CO	MCU-VF	MCU-PD	MCU-APOD	MCU-CO	MCU-VF
1	0.0206	0.0202	0.1970	0.1001	0.5599	0.5409	0.8337	0.04025
0.95	0.0314	0.0190	0.2413	0.0685	0.5291	0.5410	0.8018	0.04298
0.9	0.0437	0.0187	0.3675	0.0709	0.5081	0.5440	0.7482	0.04150
0.85	0.0583	0.0303	0.5420	0.0715	0.7491	0.5410	0.7491	0.04340
0.8	0.0197	0.0206	0.6943	0.0719	0.5449	0.5502	0.7858	0.04871

In the context of Multiple Carrier Pulse Width Modulation (MCPWM) strategies employing sinusoidal reference, several observations emerge: (i) The harmonic content of the output voltage is minimal compared to the MCU-VF strategy within the modulation index range of 0.9-1, as detailed in Table II and Figure 6. (ii) The carrier overlapping strategy exhibits the highest DC bus utilization, while all other strategies maintain relatively consistent DC bus utilization, albeit lower than the MCU-CO strategy, as outlined in Table III and Figure 5. (iii) The Form Factor (FF), a metric indicating the shape of the output voltage, attains its maximum for the MC-UCO strategy, as presented in Table IV. (iv) The MCU-APOD strategy demonstrates relatively lower harmonics after second-order attenuation, as indicated by the Distortion Factor (DF) in Table IV. Furthermore, in the context of Hybrid Pulse Width Modulation (PWM) strategies: (i) The harmonic content of the output voltage is minimized compared to the MCU-VF strategy across various modulation indices, as shown in Table II and Figure 10. (ii) Similar to MC-PWM, the carrier overlapping strategy exhibits the highest DC bus utilization, with other strategies maintaining relatively consistent, yet lower, DC bus utilization compared to MCU-CO, as evidenced by Table III and Figure 9. (iii) Crest Factor (CF) remains nearly constant across all strategies. (iv) The Form Factor (FF) achieves its maximum for the MCU-CO strategy, according to Table IV. (v) In the modulation index range of 0.8-0.9, MCU-VF strategies show relatively lower harmonics after second-order attenuation, as indicated by DF in Table IV.

V. Experimental results

In this segment, the outcomes of experimental investigations conducted on a recently designed seven-level asymmetric inverter using the SPARTAN-3 FPGA system are presented. FPGAs typically feature on-chip PWM controllers, facilitating straightforward implementation. Therefore, this work involves the real-time execution of the selected inverter through FPGA. Multi-carrier PWM strategies designed for the chosen inverter, employing a hybrid reference (which exhibits superior performance in simulations), are crafted using Xilinx's system generator software. The gate signal generator model, created with the system generator, is compiled, converted into bits, and subsequently loaded into the FPGA for real-time execution. In this segment, we showcase the outcomes of our experimental endeavors conducted on NSLAIs utilizing FPGA technology. Employing the Xilinx system generator software, we devised MCPWM strategies tailored for the selected inverter with a hybrid reference. The experimental findings are presented through oscillograms of PWM outputs and the corresponding harmonic spectra, as measured by a power analyzer. The experiments encompassed variations in the modulation factor (ma) while maintaining the modulation factor (mf) at the same level as in simulation studies. We specifically illustrate the output voltages' Root Mean Square (VRMS) for the fundamental frequency and analyze their Total Harmonic Distortion (%THD), Distortion Factor (%DF), and Crest Factor (CF). The experimental data and harmonic spectra are displayed for a singular ma value of 1 for the hybrid asymmetrical configuration. Figure 11 elucidates the complete hardware setup, while Fig. 12-19 depict the experimental output voltages and Fast Fourier Transform (FFT) analyses of chosen NSLAIs achieved through FPGA, employing Hybrid PWM strategies such as PDPWM, APODPWM, COPWM, and VFPWM, respectively. Considering laboratory constraints, the experimentally obtained peak-to-peak output voltage is scaled down to 36V. Table 5 and Fig. 20 offers a comparative analysis of %THD in output voltage concerning different multi-carrier unipolar hybrid PWM strategies for diverse modulation index values. VRMS (fundamental) values for the aforementioned strategies across various modulation indices are detailed in Table 6, with graphical representations presented in Fig. 21. Table 7 and Fig. 22 provide a comparison of %DF in the output voltage for different multi-carrier unipolar PWM strategies, considering various modulation index values. The crest factor of the output voltage for all the mentioned strategies is measured and falls within the range of 1.3 to 1.4. Experimental parameters include $VDC = 6V$, $R\ (load) = 100\Omega$, $fc = 2000\ Hz$, $fm = 50$ Hz, and $mf = 40$.

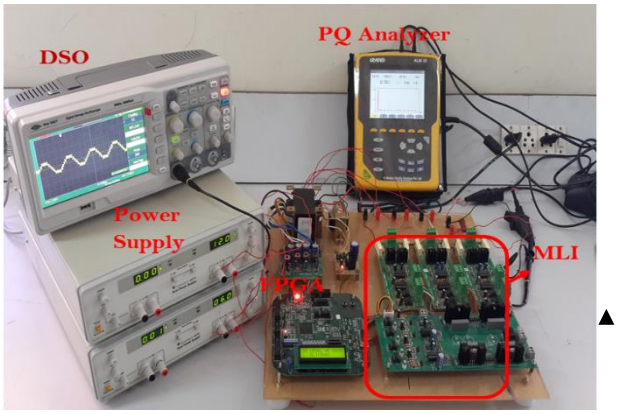

Fig. 11 Hardware setup of NSLAI

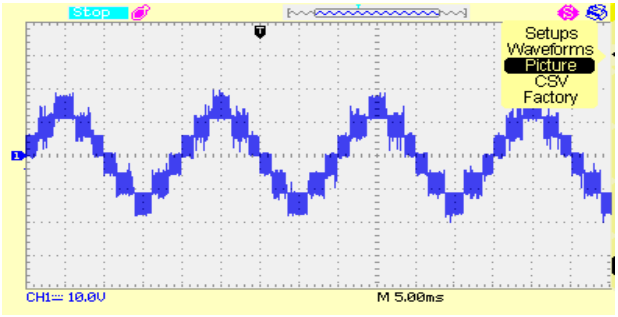

Fig. 12 Experimental output voltage with PDPWM strategy

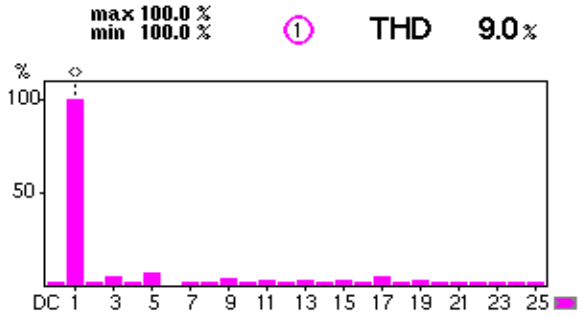

Fig. 13 FFT plot for output voltage of PDPWM strategy

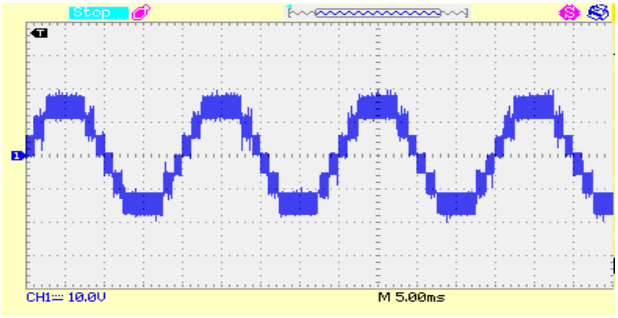

Fig. 14 Experimental output voltage with APODPWM strategy

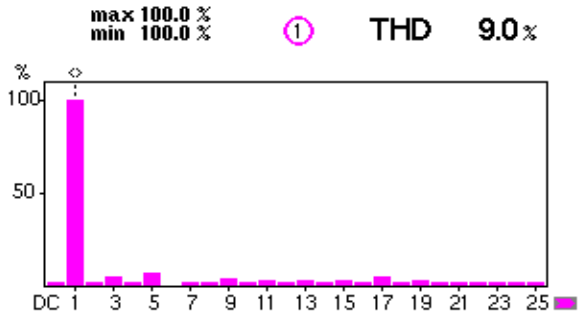

Fig. 15 FFT plot for output voltage of PDPWM strategy

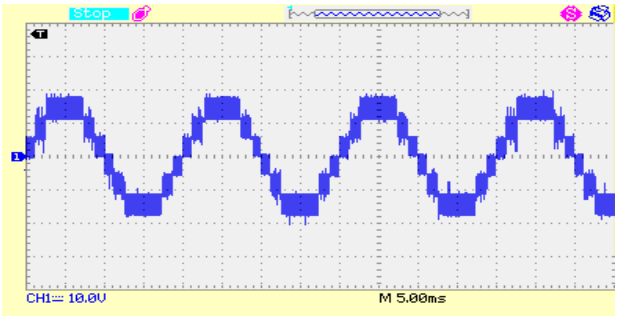

Fig. 16 Experimental output voltage with COPWM strategy

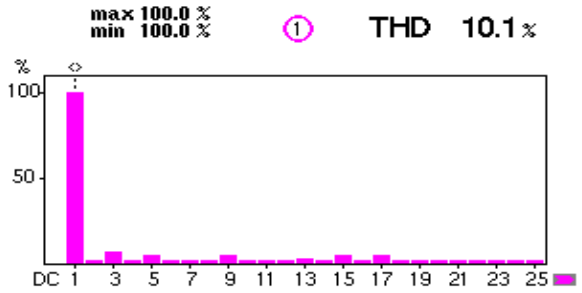

Fig. 17 FFT plot for output voltage of COPWM strategy

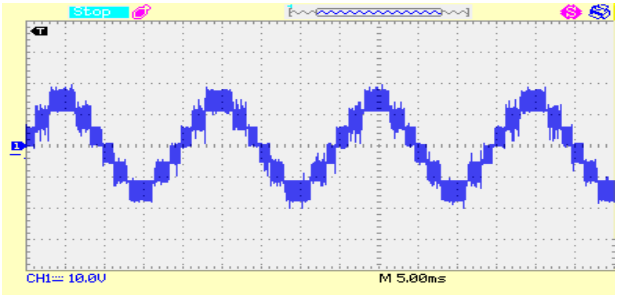

Fig. 18 Experimental output voltage with VFPWM strategy

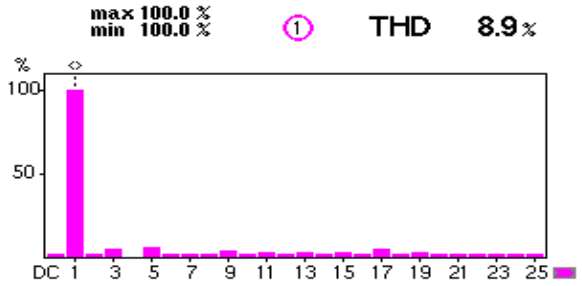

Fig. 19 FFT plot for output voltage of VFPWM strategy

Table 5
% THD for different modulation indices

m_a	MCU-PD	MCU-APOD	MCU-CO	MCU-VF
1	9	10.1	10.8	8.9
0.95	9.6	10.3	10.9	9.5
0.9	9.8	10.5	11.1	9.5
0.85	9.9	10.7	11.3	9.6
0.8	9.98	10.8	11.37	9.69

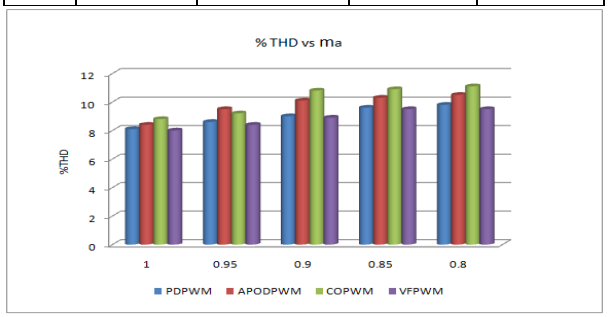

Fig. 20 %THD of output voltage vs ma

Table 6
VRMS (fundamental) for different modulation indices

m_a	MCU-PD	MCU-APOD	MCU-CO	MCU-VF
1	9.31	8.34	9.55	8.45
0.95	8.45	8.56	8.70	7.80
0.9	7.56	7.55	7.85	7.53
0.85	7.45	7.39	7.60	7.45
0.8	7.34	7.25	7.55	7.35

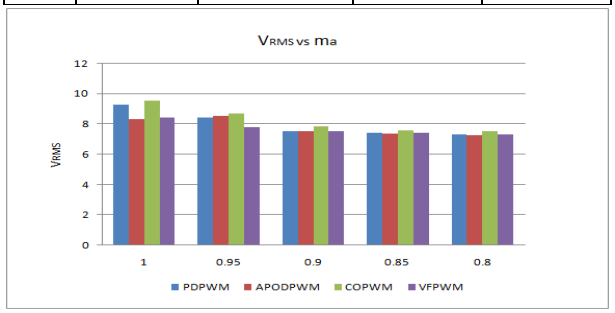

Fig. 21 RMS output voltage (fundamental) vs ma

Table 7
%DF for different modulation indices

m_a	MCU-PD	MCU-APOD	MCU-CO	MCU-VF
1	0.080	0.082	0.09	0.082
0.95	0.082	0.09	0.091	0.085
0.9	0.091	0.10	0.10	0.095
0.85	0.1	0.102	0.10	0.101
0.8	0.1	0.105	0.104	0.102

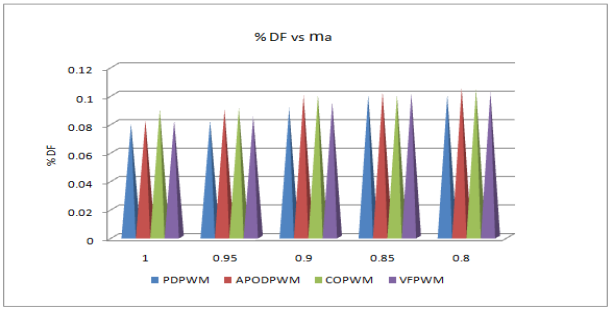

Fig. 22 %DF vs ma (By experiment)

As evident in the findings presented in Table 5 and Figure 20, it is noteworthy that the VFPWM strategy exhibits the least harmonic content in the output voltage. Analyzing Table 6 and Figure 21, it is discerned that the COPWM strategy yields a higher Root Mean Square (VRMS) output voltage compared to other Pulse Width Modulation (PWM) strategies. Furthermore, insights derived from Table 7 and Figure 22 indicate that PDPWM strategies display a lower percentage of Distortion Factor (%DF).

Table 8
Power loss comparison and efficiency of the mli with different output power.

Load Rating	Conventional			Proposed		
	Output Power	%η	% Loss	Output Power	%η	% Loss
150 Ω	621.91	98	2	630.45	98.94	1.16
120Ω	752.42	97.81	1.19	782.32	98.10	1.90
100Ω	882.91	97.74	1.26	899.82	97.72	1.28

80Ω	997.91	97.71	1.29	1001.92	97.68	1.32
60Ω	1307.01	97.71	1.29	1406.922	97.69	1.31

According to Table 9, suggested MLI have better efficiency with proposed PWM method (98.94%) due to the lower power loss. The power loss of the MLI is determined using PLECS software. The net losses were measured at the power output of 630.45 W. In this particular aspect, effective switching loss of the MLI is 0.16 % and the conduction loss is 1.00%. Furthermore, % η and power loss of the MLI is assessed for various power ratings using simulation setup, and the results are shown in Table 9. Table 9 shows that suggested MLI performs better in 630.45W, with efficiency value of 98.94 % in proposed PWM and 98% in conventional method.

VI. Conclusions

This study introduces a hybrid reference Pulse Width Modulation (PWM)-based seven-level asymmetric inverter with fewer components. This suggested inverter reduces switching needs, boosts output voltage, and reduces harmonic distortions. THD, RMS, Crest Factor, Form Factor, and Distortion Factor were rigorously evaluated, reported, and scrutinized. The hybrid reference Carrier Overlapping approach outperformed traditional PWM techniques with a greater fundamental RMS voltage output (220.4V) and lower % THD (16.02%) than all in the hybrid reference Variable Frequency strategy. Strangely, all PWM methods had similar Crest and Form Factors. The Variable Frequency method had a low Distortion Factor (0.0402%). Reduced power loss improved multilevel inverters (MLI) efficiency (98.94%) with the hybrid reference technique. This study generated both simulation models using Matlab SIMULINK-POWER SYSTEM and the prototype setup and control using SPARTAN-3 FPGA. The innovative seven-level asymmetric inverter architecture and enhanced PWM approach were proven feasible. The study also shows that the hybrid reference PWM strategy improves inverter performance and output voltage harmonic spectra compared to Sinusoidal PWM. This discovery bodes well for inverter technology, improving efficiency and voltage quality for many applications. This topology is ideal for low- and medium-power applications.

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