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Investigating the Impact of Technology Scaling on Stability Performance of Sub-threshold Static Random Access Memory Bitcell Topologies

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Abstract: - Static random-access memory (SRAM) is increasingly being used in VLSI circuits as a result of the development of portable devices. As the demand for low-power devices increases, sub-threshold operation of SRAMs has become a popular method to reduce power consumption but at the cost of reduced stability. The work aims to propose design parameters for SRAM bit cell topologies- 6T and 10T with proper device sizing and to investigate the impact of technology scaling on its stability performance in the sub threshold region. Moreover, analysis demonstrates the impact of variations of device sizing in terms of Cell ratio and Pull up ratio on stability margins of designed SRAM topologies. Simulations are carried out in the HSPICE environment using 16 nm and 22 nm CMOS process nodes. We find that the stability margins of 10T SRAM cell outperform the 6T SRAM cell; however stability margin decreases with decreasing technology nodes. The Read Static Noise Margin (RSNM) and Write Static Noise Margin (WSNM) of 10T SRAM cell is improved by 48.38% and 308.64% respectively in 22nm and 53.04% and 243.93% respectively in 16nm process technology as compare to 6T SRAM cell.

Keywords: CMOS, Read Static Noise Margin, SRAM, Stability, Write Static Noise Margin

I. INTRODUCTION

The development of SoC & nanotechnology has led to SRAM becoming a significant component of VLSI circuit designs. System-on-Chip (SOC) design has evolved rapidly in recent years, with the integration of various components onto a single chip. Static Random Access Memory is an essential component of any SOC, providing high-speed data storage for a range of applications. As SOC designs have become more complex, stability concerns have also grown in importance. Any instability in the SOC can lead to system failures and reduced performance, making stability a critical consideration in SOC design. Performance enhancement in terms of power, area of SRAM is possible through technology scaling. The decline in the technology leads to instability in SRAM circuit and makes the device more susceptible to external unwanted noise signal [1, 2]. The power saving i.e reduction in dynamic power consumption using scaling of supply voltage is predominantly been adopted as a measure of power saving technique. The power saving technique is the preferred choice in the development of low power applications however it comes at the cost of reduced stability margin[3]

In the design of SRAM cell, parameters to be fundamentally considered are: stability, area, power and delay. Delay increases with increasing complexity and the need for more transistors in a smaller area [4]. A low threshold voltage degrades the transistor's performance; nonetheless, a rise in threshold voltage increases cell leakage and compromises the stability of the cell [5]. In order to stretch the capacity of portable devices for longer periods, power-saving measures are being taken which lead to a scaling down of CMOS devices this in turn improves performance in terms of operating speed, area and power [6]. The researchers have increased the density of SRAM by scaling the device in order to improve system performance. The scale down approach leads to several challenges for SRAM design in nanometer regime. As feature sizes shrink, it becomes increasingly difficult to maintain high manufacturing yields and reliability of the circuit. Moore's law states that as transistor sizes get smaller, the number of transistors on a device doubles every two years. Consequently, when the device size decreases, the chip density rises. A crucial design consideration for ultra-low power applications is reduced power dissipation. With the advancement of technology, leakage power has emerged as a significant contributor in total power dissipation. One useful method for lowering the SRAM cell's power dissipation is voltage scaling [7]. Many researchers emphasize lowering the supply voltage in scaled-down CMOS technology, which negatively impacts SRAM data stability, i.e. cell reliability. The device sizing in terms of cell ratio[8] and pull up ratio[8] prominently determines the stability of the circuit.

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In this paper 6T SRAM cell [9] and 10T SRAM cell [10] are designed in terms of cell ratio and pull up ratio to get optimum value of read and write stability. The 6T and 10T SRAM cells are analyzed at 16nm and 22nm technology node in terms of stability and power.

A. CMOS 6T SRAM Cell Topology:

The conventional 6 transistor (6T) SRAM cell as shown in above Fig.1 is formed by two cross couple inverters [M1,M2,M3,M4] and two access transistors [M5,M6]. The bitlines BL and BLB read the data stored in the cell, while the word line WL allows the bitlines to access the cell and its value.

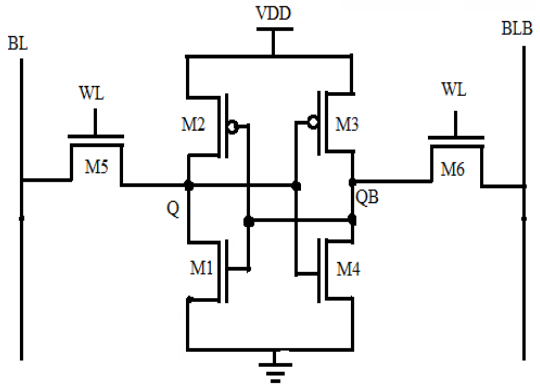


Figure 1. 6T SRAM Cell[9][17]

In a read operation, the WL is maintained at a HIGH level and the data available in the cell is accessed via the BL and BLB. In the course of a Write operation, WL, BL, and BLB are maintained at HIGH levels. One bit line (BL,BLB) will be discharged keeping a LOW value and the other with a HIGH value in accordance with the values available in the cell.

B. CMOS 10T SRAM Cell Topology

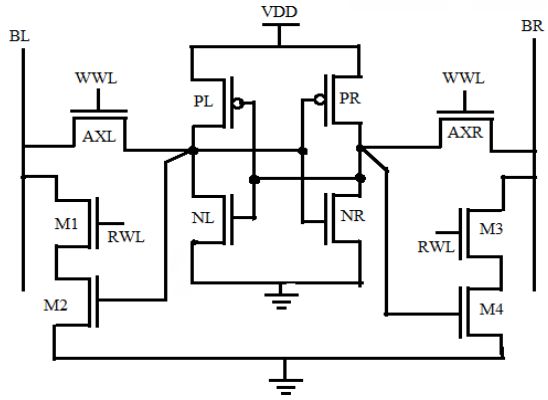


Figure 2. 10T SRAM Cell[10]

The figure above shows 10T SRAM cell consisting of separate access transistors for read and write operation. RWL signal is set to logic high state whereas WWL signal is set to logic low level in read mode of cell. BL and BR are pre-charged bit-lines. The read access transistor RWL is turned on to read the data bit from the cell, assuming that the starting values of the cell are VL='0' and VR='1'. A path to ground for the charged BR is provided by the bottom right NMOS transistor, which is turned on by a high logic signal at VR. If a VL store “1,” the complementary bit-line (BL) is get discharged through the bottom left NMOS transistor.

II. PERFORMANCE PARAMETERS AND METHODOLOGY

The section elaborates the performance parameter- Stability in hold, read and write mode. Besides, the methodology for measurement of stability and Cell Ratio (CR) , Pull up ratio (PR) is explained in the section.

A. Read Stability and Write ability:

The main performance factor that affects how accurately a memory cell can work is the SRAM cell's stability. Alternatively, it also provides the measure of failure probability of SRAM cell. Data protection is the SRAM cell's primary functional constraint in advanced technology nodes. Technical scaling will cause the cell to become less stable when the supply voltage drops, leakage currents and variability rises.The stability of the cell is determined by its capability to preserve data against noise. [11].

Stability is characterized by the SNM [12]. Stability of SRAM cell deteriorates with decreased supply [13].

With cross-coupled inverters, the stability of the SRAM cell is the noise voltage needed to flip the hold data with the least possible noise. The SNM is calculated using butterfly curve method in which maximum side of the square that fits in the lobe of VTC of cross coupled inverters is determined [14-17]. In the read mode of operation of SRAM cell, the highest possible side of the square which fits in the lobe of VTC (Voltage Transfer Characteristics) curves of cross coupled inverters, is the static noise margin as shown in Fig. 3. Using SRAM cell DC analysis, the SNM is determined.

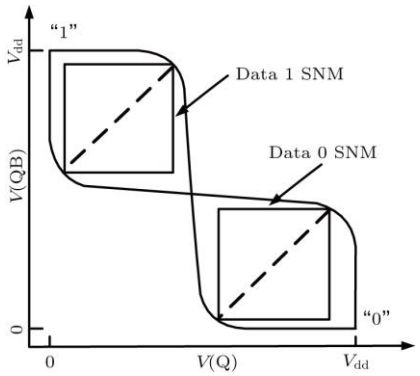


Figure 3. Butterfly curve to find Static Noise Margin in Read Mode[9]

The write ability of the SRAM is to flip the data stored in the cell during write mode of operation. WSNM – write static noise margin can be evaluated by means of word-line sweep [18, 19], bit-line voltage sweep [20,21] analytical approach[22]. In the paper, the write ability of the SRAM cell is determined by using the butterfly (VTC) curve method [23]. The Fig. 4 shows the 6T SRAM cell performing writing '1' operation.

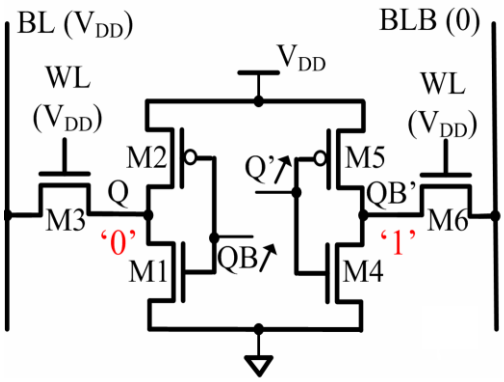


Figure 4. WSNM of 6T SRAM Cell exhibiting writing'1' [20]

The VTC curve is obtained by executing the DC simulation with sweeping of the inputs of inverters Q and QB' as shown in Fig. 5[20].

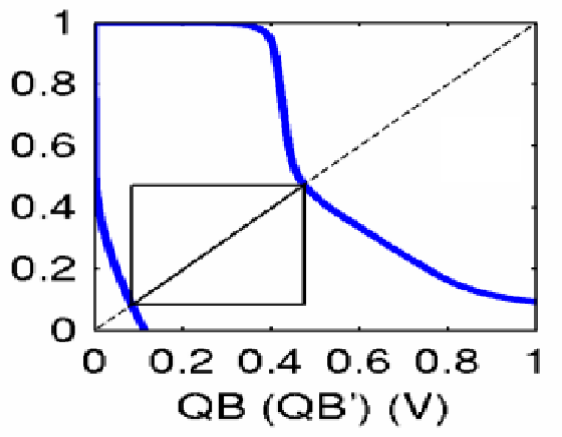


Figure 5. WSNM using butterfly curve method [20]

B. Cell Ratio and Pull Up Ratio

Cell ratio(CR), pull up ratio(PR) [8] determines the read stability and write ability respectively. Read stability i.e Read SNM [9] is the minimum noise voltage which is able to flip the data contents in the cell. Write ability is the noise voltage level that is required to be available at the bit lines to write or flip the data correctly. In order to read and write data to and from the cell correctly SRAM cell should be designed properly keeping CR and PR at optimum proportion.

The figure 1 shows the conventional 6T SRAM cell [9] with back to back inverters and access transistors. The cell ratio and pull up ratio for the same is:

Cell Ratio (CR) = (W1/L1) / (W5/L5).

Pull up Ratio (PR) = (W2/L2) / (W5/L5).

III. RESULTS AND DISCUSSION

The first section of results and discussion, explains the design considerations of 6T and 10T SRAM cell topologies. The stability analysis-HSNM, RSNM, WSNM of 6T, 10T SRAM cell topologies is investigated at 16nm and 22nm CMOS process node. In addition, the impact of technology scaling is discussed. The second section evaluates the impact of CR-PR variations on 6T SRAM cell topology.

These investigations provide a comprehensive understanding of how technology scaling and CR/PR ratios impact the stability of SRAM cells in the given CMOS technologies and supply voltages.

A. Design Considerations, Stability Performance Analysis of 6T and 10T SRAM CMOS Topologies at 22nm and 16nm Process Node:

Referring to Fig.1, the read and write operation is conducted through common access transistors M5 and M6. The read stability is dependent on the strength of M1 i.e to prevent read failure; M1 pull down transistor should be strong enough with high threshold voltage to avoid flipping of the data in the cell due to noise at Q node. Similarly, M4 should be strong enough to withstand noise at QB node. It is characterized by Cell ratio (CR). Alternatively, to enable write ability of the cell, access transistor M6 should be strong enough so that the drain voltage at node QB falls below drain voltage of M3. It is characterized by Pull Up ratio(PR). Thus, the design of transistors with high CR for high read stability and low PR for better write ability put constraints on the improvement in both the read stability and write ability in 6T SRAM cell since the read and write operations happens through common access transistors.

a. Design Parameters of 6T SRAM Cell at 22nm:

Supply Voltage VDD =0.8V; L=22nm;

Pull Down NMOS Transistor (WN) =M1 and M4=132nm

Pull Up PMOS Transistor (WP) = M2 and M3=264nm

Width of Access Transistor (Width of M5and M6) =44nm

CR=3 (Width of Pull Down)/(Width of Access Transistor)

(WP) =2*WN

b. Design Parameters of 6T SRAM Cell at 16nm:

Supply Voltage VDD =0.7V; L=16nm;

Pull Down NMOS Transistor (WN) =M1 and M4=96nm

Pull Up PMOS Transistor (WP) = M2 and M3=192nm

Width of Access Transistor (Width of M5and M6) =32nm

CR=3 (Width of Pull Down)/(Width of Access Transistor)

(WP) =2*WN

c. Design Parameters of 10T SRAM Cell at 22nm:

Referring to Fig. 2 , maximum stability during read and write operations is obtained by designing 10T SRAM cell with CR (cell ratio) value of 3 and a PR (pull-up ratio) value of 0.5. The main advantages of 10T SRAM cell over 6T SRAM cell is availability of the separate read and write access transistors in 10T cell which allows to design high value of CR and low value of PR to maintain high RSNM and high WSNM respectively.

Supply Voltage VDD =0.8V; L=22nm;

Pull Down NMOS Transistor (WN) =NL and NR=132nm

Pull Up PMOS Transistor (WP) = PL and PR=264nm

Width of Write Access Transistor WNA1 (Width of AXL and AXR) =528nm

Width of Read Access Transistor WNA2 =44n

CR=3 (Width of Pull Down)/(Width of Access Transistor)

PR=0.5 (Width of Pull Up)/(Width of Access Transistor)

WP=2*WN

d. Design Parameters of 10T SRAM Cell at 16nm:

Supply Voltage VDD =0.7V; L=16nm;

Pull Down NMOS Transistor (WN) =NL and NR=96nm

Pull Up PMOS Transistor (WP) = PL and PR=192nm

Width of Write Access Transistor WNA1 (Width of AXL and AXR) =384nm

Width of Read Access Transistors WNA2 =32nm

CR=3 (Width of Pull Down)/(Width of Access Transistor)

PR=0.5 (Width of Pull Up)/(Width of Access Transistor)

WP=2*WN

The simulation results focus on evaluating the stability performance of 6T and 10T SRAM cell at 22nm and 16nm CMOS technology node. The results are obtained using Synopsys H-spice environment. The simulations are conducted at 16nm and 22nm CMOS technologies with supply voltages of 0.9V and 0.95V, respectively. The stability analysis in read and write mode i.e Read stability (RSNM) and Write ability (WSNM) respectively determines the reliability of the cell. The Hold static noise margin (HSNM) determines the cell's stability in standby mode. The stability performance is obtained by using butterfly curve methodology. The read stability performance is also validated by means of Vnoise method. As shown in Fig. 6 the Vnoise source (Vn) is

introduced at the input of the each inverter in a cross coupled pair to evaluate maximum noise voltage withstand by the circuit. The voltage at which the output of the inverter flips from its initial position is taken as maximum noise margin or the stability of the cell.

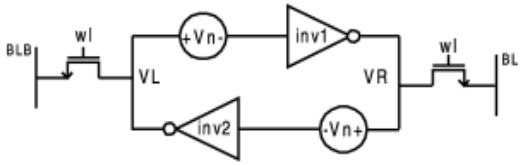
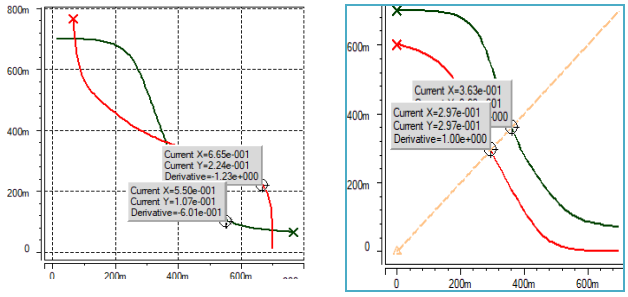


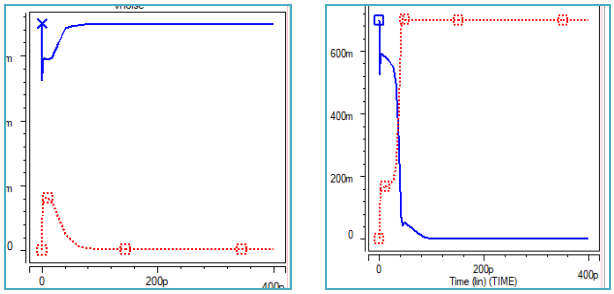
Figure 6. Conventional 6T SRAM cell with Vnoise source

As shown in Fig. 7(a) and (b), the RSNM and WSNM of 6T SRAM cell at 16nm technology is found out by butterfly curve method. The side of maximum square is evaluated as 115mV and 66mV respectively.



(a) (b)

Figure 7. (a) 6T SRAM cell RSNM at 16nm (b) 6T SRAM Cell WSNM at16nm using Butterfly curve method



(a) (b)

Figure 8. 6T SRAM cell Read Stability at 16nm using Vnoise Method.

The RSNM of 6T SRAM cell is evaluated by using butterfly curve method as shown in Fig 7 and also validated by using Vnoise source method as shown in Fig. 8. It can be seen that the voltage at the nodes of output of each of cross coupled inverters remain steady at its initial position of Q and QB till the point Vn=115mV. As soon as the voltage of the noise source increased to 116mV, the output voltages shifts and data got disturbed at the output of cross coupled inverter of SRAM cell. The same approach is used for finding out the stability performance of 10T SRAM cell at 16nm and 22nm process node technology. The findings of 6T and 10 T SRAM cell pertaining to HSNM, RSNm and WSNM are depicted as shown in table I and II.

TABLE I: 6T SRAM CELL STABILITY PERFORMANCE

Noise Margin/ Technology Node	HSNM	RSNM	WSNM
22nm	237mV	155mV	81mV
16nm	174mV	115mV	66mV

It is investigated that there is a trade-off between Cell Ratio and Pull up Ratio in 6T SRAM cell since reading and writing operation in 6T SRAM cell takes place through common access transistors. Thus, improving read degraded

the write operation and vice-versa. The WSNM of 6T SRAM cell as shown in the above Table I, is substantially lower than RSNM since CR is at value '3' and width of PMOS transistor is kept twice than the width of NMOS transistor, consequently it leads to the PR at value '6' which in turn weaken the write ability of the cell.

TABLE II: 10T SRAM CELL STABILITY PERFORMANCE

Noise Margin/ Technology Node	**HSNM**	**RSNM**	**WSNM**
22nm	235mV	230mV	331mV
16nm	179mV	176mV	227mV

As shown in Table II, the RSNM and WSNM of a 10T SRAM cell shows enhancement in stability as compared to a 6T SRAM cell. Technology scaling has a prominent effect on the 6T SRAM cell in comparison to the 10T SRAM cell. The significant improvement in WSNM for the 10T SRAM cell is achieved through the design of a cell with high CR and low PR.

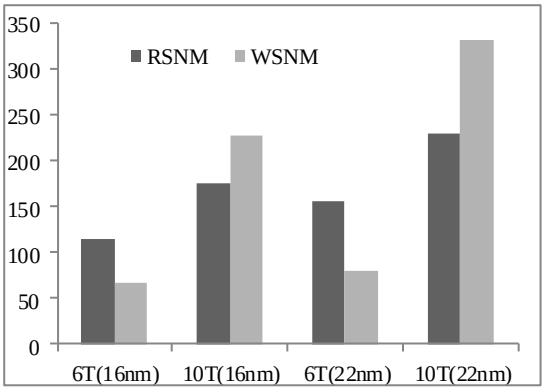


Figure 9: Stability performance analysis of SRAM bit cell topologies at 16nm and 22nm process node.

The Fig. 9 shows the overall read and write stability of 6T and 10T SRAM. It is inferred that the 10T SRAM cell provides improvement in stability performance over 6T SRAM cell however the technology scaling from 22nm to 16nm degrades the SRAM stability performance.

B. Impact of CR-PR variations on stability of 6T SRAM CMOS Topology at 22nm and 16nm Process Node:

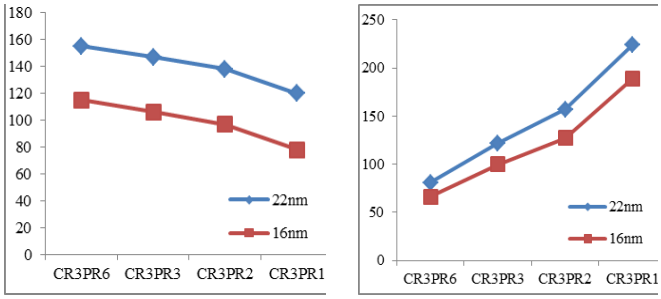
Modulating the width ratios between the pull-up and pull-down transistors relative to the access transistors induces variations in the static noise margins of SRAM bitcells [24][25]. The second part of this analysis investigates the impact of cell ratio (CR) and pull-up ratio (PR) on the stability performance of a 6T SRAM topology. Simulations sweep CR and PR while holding technology node and supply voltage constant. The resulting influence on hold static noise margin (HSNM), write static noise margin (WSNM), and read static noise margin (RSNM) is quantified. This parametric evaluation aims to elucidate the optimal CR and PR design space that maximizes stability during read and write operations of the 6T bitcell. Determining the tradeoffs between noise margins while tuning these key ratios provides insights into balanced SRAM design that ensures robust read and write functionality for a given application.

TABLE III: IMPACT OF CR-PR VARIATIONS ON STABILITY OF 6T SRAM CELL

Noise Margin	**RSNM**		**WSNM**	
CR-PR/Technology Node	**22nm**	**16nm**	**22nm**	**16nm**
CR=3 PR=6	155mV	115mV	81mV	66mV

CR=3 PR=3	147mV	106mV	122mV	100mV
CR=3 PR=2	138mV	97mV	157mV	127mV
CR=3 PR=1	120mV	78mV	224mV	189mV

The Table III below shows that the change in CR and PR affects the read and write stability of 6T SRAM cell. As the PR value reduces, the write mode stability of the cell improves with decrease in the read mode stability.



(a) (b)

Figure 10 (a) RSNM of 6T SRAM (b) WSNM of 6T SRAM Cell with Changes in CR and PR

Fig. 10 (a) illustrates the variation in read static noise margin (RSNM) as the cell ratio (CR) and pull-up ratio (PR) are modulated. It is investigated that the read stability decreases with decrease in PR however write stability (WSNM) as shown in Fig. 10 (b), increases significantly with decrease in PR. The common access transistors for read and write operation in 6T SRAM cell led to the tradeoff between RSNM and WSNM with CR and PR. Thus, in 6T SRAM cell, the optimum value for RSNM and WSNM can be obtained by designing the cell with effective CR and PR. As can be seen from the table the optimum value of CR and PR for this configuration of the 6T SRAM cell can be CR=3, PR=3 or CR=3, PR=2.

With the design of 6T and 10T SRAM cell considering the preset design parameters, stability of 10T SRAM cell in read and write mode is much improved over 6T SRAM cell. The improvement in stability in 10T SRAM cell is because of isolation of the bit line from the core of the cell preventing the data from external noise voltage. Besides, separate read and write access transistor allows 10T SRAM cell design with high CR and Low PR.

IV. CONCLUSION

With the advancements in high speed, low power applications, the need of the reliable memory arises which can store the data with highest accuracy. In this paper, the investigations of the memory cell performance pertaining to stability in read and write operation has been carried out. We have proposed optimum design considerations in terms of Cell ratio and Pull up ratio of 6T and 10T SRAM memory cell to achieve comparatively higher stability in nanometer regime. The simulations are carried out in 16nm and 22nm CMOS process technology. The results show that the technology scaling from 22nm to 16nm process impacts on stability margin. The RSNM and WSNM of 6T SRAM Cell is reduced by 25.80% and 18.51% respectively with the technology scaling from 22nm to 16nm CMOS process node. The same impact is observed in 10T SRAM cell with reduction in RSNM and WSNM by 23.47% and 31.42% respectively.

Furthermore, it is evaluated that the effect on stability margin of 6T SRAM cell is highly dependent on CR and PR due to common access transistor. Due to the separate access transistors for read and write operations in 10T SRAM cell, the RSNM and WSNM is improved in the cell by 48.38% and 308.64% respectively in 22nm and by 53.04% and 243.93% respectively in 16nm process technology as compare to 6T SRAM cell.

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