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Implementation of Full adder in Multiple valued Logic for Performance Optimization

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Abstract: - Multiple valued logic is now becoming more significant in real-world applications. Mathematical design blocks are essential in digital and mixed-signal systems. A system's arithmetic blocks often use the most power because of the high switching activity. Implementations of quaternary arithmetic may be a way to cut down on energy use while improving system performance. In this paper, quaternary adders are developed using three different approaches, and their binary equivalents are evaluated in terms of size, predicted logic depth, and performance estimation.

Keywords: Quaternary Logic , Multiple valued logic (MVL),Full adder, One hot encoder.

I. INTRODUCTION

This Since 1968, there has been significant growth but a reduction in the value of numerous types of research that is done in academic circles as opposed to industry. The attempts to design an effective multiple valued logic system in microelectronics mirror the rapid evolution of digital systems. Charge coupled devices (CCDs), integrated injection logic (I2L), CMOS technology, Emitter-coupled logic (ECL) and quantum devices have all been used to construct MVL circuits in bipolar technology. Also taken into consideration are other technologies like charge coupled device technology and opto electronics technology. Early multiple valued research focused mostly on multiple valued semiconductor circuits, multiple valued semiconductor circuits, and multiple valued network synthesis [1].These three domains interact and overlap one another quite a bit.

The term "multiple-valued logic" refers to logic that has more than two values, or many values, such as ternary, quaternary, and quinary logic. When it comes to this kind of reasoning, the decision of which base to use can be determined in either the theoretical or practical realm. It is possible to find an optimal choice that satisfies both aspects[2,3]. Daniel Etiemble conducts a comparison between the speed, power dissipation, and chip size of two important and contrasting technologies in m-valued integrated circuits (ICs) for MOS. In contrast to the two-valued circuits, the comparison focuses on the circuit complexity of the encoder, decoder, and two-valued circuits in the m-valued case. [2] Consider a quaternary function that has 'm' quaternary inputs and a binary function that has 'n' binary inputs. Equation gives the binary equivalent of the quaternary one. $F_b eq = F_q$

One needs to combine any two binary functions in order to obtain any quaternary number.

$$F_b \times F_b = F_q$$

So in terms of a number's radix

$$m = 2 \cdot n$$

$$2^{2^n} \cdot 2^{2^n} = 4^{4^m}$$

$$2^{2^{n+1}} = 2^{2 \cdot 2^{2 \cdot m}}$$

$$2^{2^{n+1}} = 2^{2^{2m+1}}$$

Therefore $m = 2 \cdot n$

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This implies that in order to have the same amount of logic as a quaternary circuit, the number of binary inputs (n) must be equal to twice the number of quaternary inputs (m). This demonstrates how quaternary logic can be used in a circuit to reduce the number of interconnections, as well as the area, propagation delay, and power consumption of a system based on quaternary integrated circuits[3].

RELATED WORK

Thoidis et al. concentrated on a set of innovative voltage-mode quaternary encoder and decoder circuits that implement level-up, level-down, logical-sum, logical-product, and level-conversion operations. These circuits include appropriately built depletion- and enhancement-modes [4, 5]. In addition, dynamic and pseudo-static latches, a pass gate with a single signal control, and dynamic and static master-slave storage units were built. These circuits can operate with just one control signal (often a clock) and have two threshold voltages for each type of MOS transistor, therefore their complementary form is not required. [6] According to Cristiano Lazzari[7,8,9], a quaternary version of arithmetic circuits like the adder can lower transistor and connectivity costsUsing voltage-mode circuits,a comparison between quaternary and binary arithmetic module implementations based on lookup table structures was also done..also gives a comparison of ripple carry adder implementations in lookup table structures in binary and quaternary forms for the first time.[10] Voltage-mode circuits use most of their energy only when switching between logic levels. Voltage-mode circuits do, in fact, offer lower power consumption in light of dynamic switching activity, which has been the main benefit of standard CMOS binary logic circuits in Datla's description [14], Gates were used to construct three distinct addition circuit architectures: carry-ripple, carry-select. carry-look-ahead. Ifat Jahangir et al. have devised a set of operators that can handle both coupled-binary and regular inputs. Sequential circuit components like latches, flip-flops, registers and counters are created using the special operators design. Sufficient requirements are developed theoretically and illustrated graphically for the sequential blocks to operate stable [15].Combinational blocks such as encoder, decoder ,multiplexer, demultiplexer and adder are designed in [16] using these operators and functions. NMAX and NMIN circuits are constructed with DLC and offered as voltage comparator applications, respectively, and the voltage-mode quaternary logic circuits NOT only realise three fundamental logic functions [17]..Various authors have designed adders using differential logic,quaternary signed digit number system,withmux,using dual RCA circuit. This paper is organised as part I consist of literature survey, part II consist of methodology with adder design, part III consist of result and conclusion part.

II. DESIGN OF QUATERNARY FULL ADDER CIRCUITS

2.1 Type I Quaternary full adder

The output of a Type I Quaternary complete adder is only available in quaternary logic once the inputs have been converted to hot codes. Fig. 1 shows block diagram for the quaternary full adder, which consist of sum calculator as barrel shifter .The two inputs, X and Y control of the barrel shifter. Depending on the inputs X, Y, Carry in, the carry block only selects and permits the carry output. The one hot encoder will have carry input added to it beforehand. Voltage levels of 0V, 1V, 2V, and 3V are used to represent the quaternary logic levels inputs 0, 1, 2, and 3 respectively. When the carry input is zero, all possible combinations of inputs are shown in Table 1, and all possible combinations are shown in Table 2 when the carry input is one.

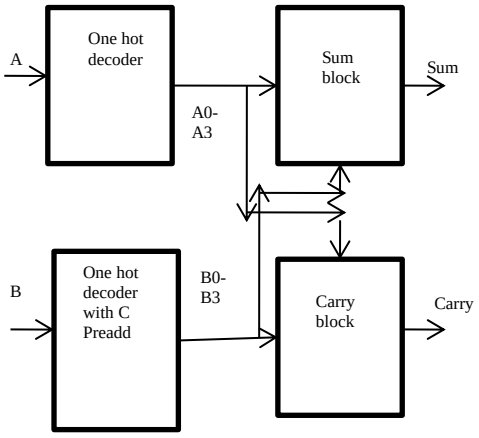

Figure.1 Schematic of Type I Quaternary Full Adder

Y	Y0	Y1	Y2	Y3
0	3	0	0	0
1	0	3	0	0
2	0	0	3	0
3	0	0	0	3

Table 1: When Carry In = 0, then One Hot Code For Input Y

Y	Y0	Y1	Y2	Y3
0	0	3	0	0
1	0	0	3	0
2	0	0	0	3
3	3	0	0	0

Table 2: When Carry In = 1then One Hot Code For Input Y

DLC1, DLC2, DLC3, one inverter and two XOR gates are required to produce Four hot codes from input Y using: Hy0, Hy1, Hy3, and Hy4. The output voltage levels are switched using hot signs produced in the single hot encoder.

Table 1&2 displays these hot codes. Because the full adder has two inputs, X and Y, it needs two one-hot encoders and hot codes that are comparable to those in tables 1 and 2..

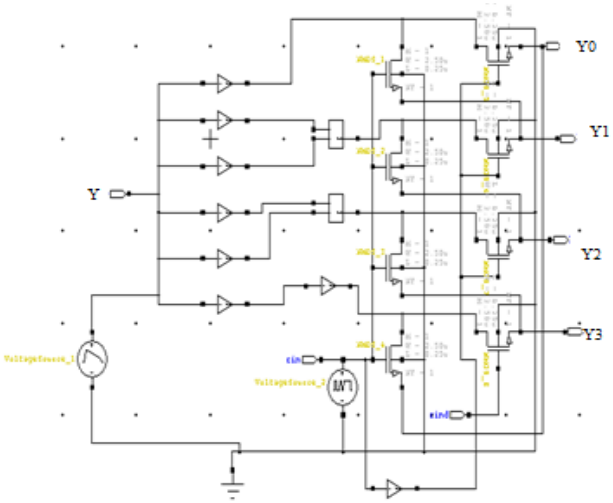

Figure.2 Schematic of one hot encoding for carry pre addition

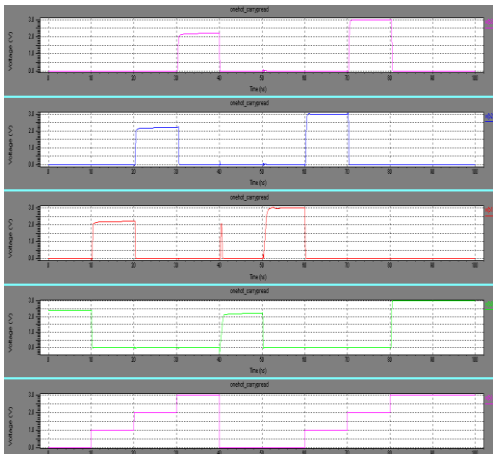

Figure. 3 Simulation result of one hot encoding for carry pre addition

2.1.1 Summer Block

The full adder truth table clearly shows that the total component of the adder is determined by shifting one input according to the other. To minimize circuit complexity, a barrel shifter is used to switch a constant 4-level voltage level of 0 V, 1 V, 2 V, and 3 V directly to the output based on the encoded input value. In this instance, the output line is driven by the barrel shifter via wired-AND logic. The sum generator's circuit architecture is depicted in Figure 4.. A0-A3, B0-B3, and Sum represent the output of a single hot encoder block and sum block, respectively

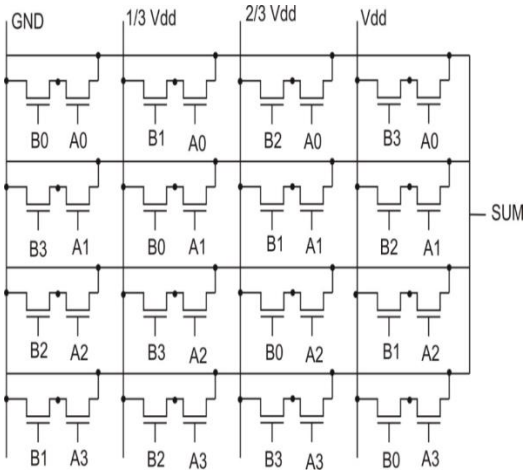

Figure. 4 Schematic of Sum block

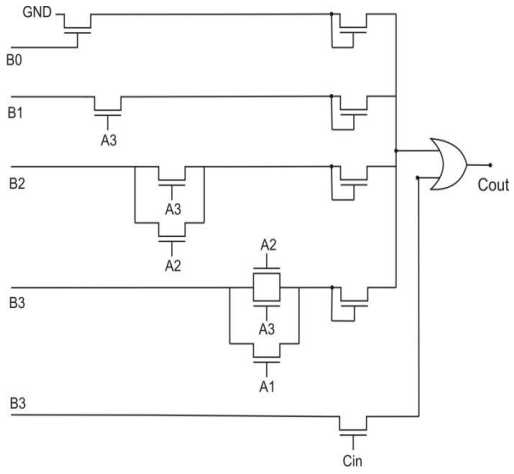

Figure. 5 Schematic of carry block

One input line serves as the choose line for the carry generating block, which only combines inputs. If the combination of inputs meets the criteria for producing carry output, the choose line will accept or reject another line.If the voltage input B is 3V and the carry in signal is high, an OR gate is employed to preserve the carry and direct it to the carry out signal in the carry generating circuit. This ensures that the carry is not lost during the initial carry pre-addition operation in the adder. The circuit diagram for the carry generator depicted can be seen in Figure 5.

2.2 Type II Quaternary full adder

In Type II ,Unique code is generated from quaternary input. Radix converters are not needed at the output side in either case since the output is in quaternary form after the addition operation.

The proposed full adder circuit composed of a sum block, a carry block, an encoder and a code generator. The conversion indicated in table 5 requires an encoder, which comprises of the DLC1 and DLC3 (Down Literal Circuit) [11]. The sum and carry for the whole adder circuit are generated the use of the code generator output code. Figure 6 is a block diagram of a complete adder circuit. Voltage ranges of 3V, 2V, 1V, and 0V are used to

symbolize the common sense ranges of the quaternary inputs 3, 2, 1, and 0. The quaternary inputs of the overall adder are X and Y.

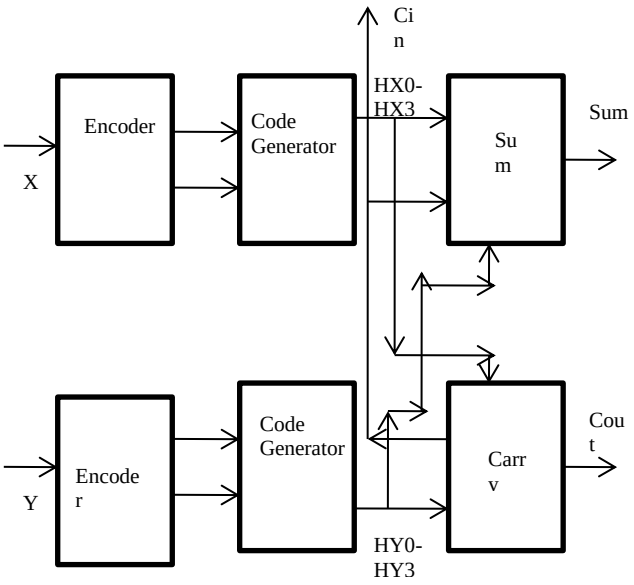

Figure. 6 Schematic of Type II Quaternary full adder

2.2.1 Encoder block

The encoder block in the proposed full adder circuit converts the quaternary values X and Y into binary representation. The code producing unit receives the encoder's output. The codes that are employed in the sum and carry block to produce the final sum and carry value are generated by this code producing unit. The encoder block consists of the DLC1 and DLC3, two inverters, and a binary X-OR gate. The circuit logic designs for encoders are shown in Figure.

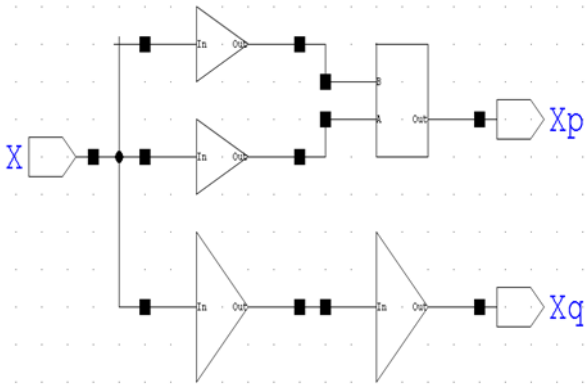

Figure. 7 schematic of Encoder block

2.2.2 Code generator block

A block diagram for X and Y the Code Generator is shown in Figure 8. Quaternary input X is divided into two equivalent binary values, Xp and Xq, as was demonstrated in the preceding section. Hx0, Hx1, Hx2, and Hx3 are generated from these two signals. The binary equivalents Yp and Yq are created from the quaternary input Y. Using these two signals, Hy0, Hy1, Hy2, and Hy3 are produced. The code generator's circuit diagram is displayed in Figure 8. There are four AND gates in it.

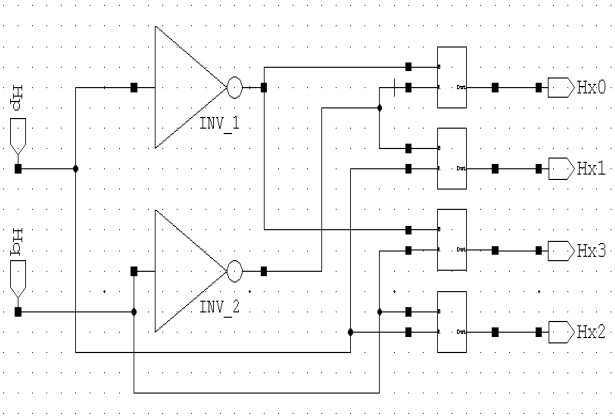

Figure. 8 schematic of code generator block

2.2.3 Sum and carry block

Pass transistors are used to build sum and carry blocks. Transmission gates can be used instead of pass transistors to achieve the required logic levels. Depending on the input level, the 4th order voltage level is adjusted towards the output. Code created by code generator blocks Hx0, Hx1, Hx2, Hx3, and Hy0, Hy1, Hy2, and Hy3 controls these pass transistors.. Figures 10 and 11 show the sum and carry circuit diagrams, respectively.

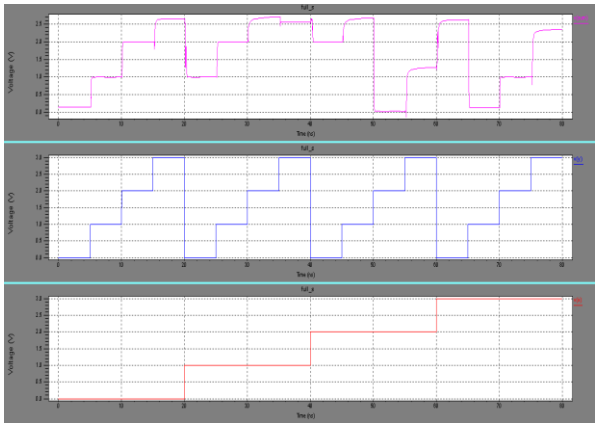

Figure.9 Simulation result of Sum block

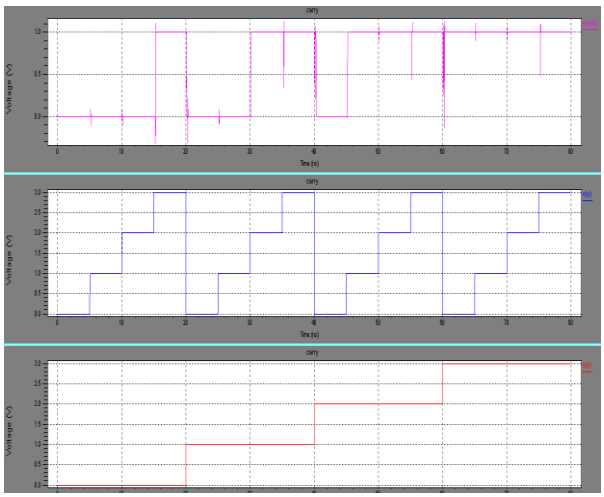

Figure.10 Simulation result of Carry block

2.3 Proposed Design Of Quaternary Adder Circuits

The four voltage levels that correspond to 0V and the additional three power supply lines of 1V, 2V, and 3V are

used by the quaternary CMOS circuit to operate.

The MIN gate, MAX gate, and inverter make up the fundamental circuit. These fundamental circuits were created by taking three different NMOS and PMOS threshold voltages into account.All further gates are constructed using these fundamental gates as a guide, simulation result of sum and carry block is shown in figure 9 and 10.

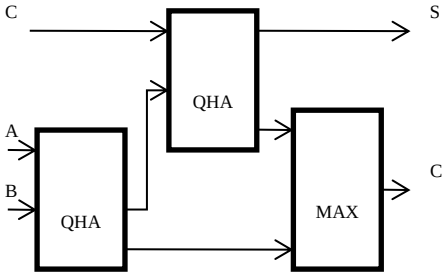

Figure. 11 Block diagram of quaternary Full adder

	X			
Y	0	1	2	3
0	0	1	2	3
1	1	2	3	0
2	2	3	0	1
3	3	0	1	2

(b)

	X			
Y	0	1	2	0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	3	1	1	1

(c)

Table 3: (b)and(c) Truth table for quaternary full adder sum & carry

III. RESULTS AND DISCUSSIONS

All of the findings and discussions ought to be included in this section. Using the number of transistors needed for each quaternary and binary equivalent circuit, the total size of the adder is calculated. Transistors are employed in quaternary logic cells in greater quantities than they are in binary circuit designs. When compared to Type I, Type II, and analogous binary circuits, the suggested quaternary adder has a reduced switching power usage. When compared to conventional binary circuits, quaternary circuits require less average voltage swing and contain more intermediate logic levels, which is the primary reason for their power savings.

Device	Power (w)
Proposed QFull adder	0.01 e-06
QFull adder (one hot decoder)	9.06 e-06
QFull adder (encoder)	2.07e-04
Binary Full adder	762E-06

Table. 4 Comparative analysis of adder based on power consumption

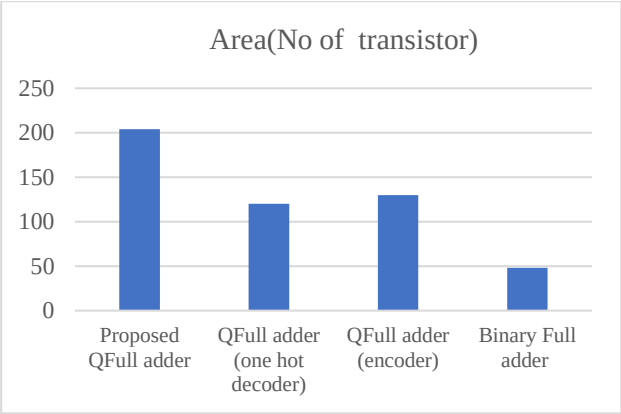

Figure. 12 Comparative analysis of adder based on area

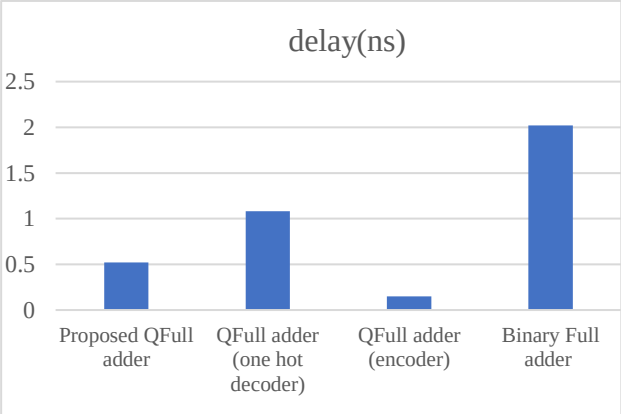

Figure. 13 Comparative analysis of adder based on delay

IV. CONCLUSION

Type I quaternary adder circuits performed better in terms of timing than Type II and binary equivalent circuits, based on the depth (number of transistors) of the critical path. When comparing the proposed full adder to its binary counterpart, 75% less latency was needed when considering delay.

REFERENCES

[1] Stanley Hurst 1988 “Two decades of multiple valued logic- An invited Tutorial”, 18th International Symposium on Multiple-Valued Logic, Palma de Mallorca, Spain, 24-26 IEEE 1998

[2] Daniel Etiemble 1988 “Comparison of Binarv and Multivalued ICs According to VLSI Criteria”, IEEE Computer Society Press Los Alamitos, CA, USA Volume 21 Issue 4, April Page28-42

[3] Kenneth C. Smith 1988 “Multiple-Valued Logic: A Tutorial and Appreciation”, Journal Computer IEEE Computer Society Press Los Alamitos, CA, USA Volume 21 Issue 4, Page 17-27,

[4] Ramakrishna Reddy M.Parvathi 2013 “Efficient Carry Select Adder using 0.12µm Techology for Low Power Applications”, Proceedings of International Conference on advances in computing Communications and informatics IEEE pp.550-553.

[5] Thoidis, D. Soudris, I. Karafyllidis, A. Thanailakis, T. Stouraitis 1998 “Design Methodology Of Multiple-Valued Logic Voltage-Mode Storage Circuits” International Symposium on Circuits and Systems vol.2 IEEE pp. 125-128

[6] I.Thoidis D.Soudris I. Karafyllidis S. Christoforidis A.Thanailakis 1998 “Quaternary voltage-mode CMOS circuits formultiple-valued logic”, IEE Proc.-Circuits Devices Syst., Vol. 145. No. 2, pp.71-77

[7] Marcus Ritt, Carlos Arthur Lang Lisboa, Luigi Carro, Cristiano Lazzari 2010 “A Cost-Effective Technique for Mapping BLUTs to QLUTs in FPGAs” Proceedings of 2010 International Conference on Field Programmable Logic and Applications IEEE pp.332 – 335

[8] Cristiano Lazzari Paulo Flores, Jose Monteiro 2010 “Voltage-mode Quaternary FPGAs: An Evaluation of Interconnections”, IEEE pp.869-872.

[9] Cristiano Lazzari Paulo Flores, Jose Monteiro 2010 “A New Quaternary FPGA Based on a Voltage-mode Multi-valued Circuit”, Proceedings of *Design, Automation & Test in Europe (DATE 2010)*, pp. 1797 - 1802 .

[10] D.M. Miller and M.A. Thornton, 2008 Mutiple-Valued Logic: Concepts and Representations,(Morgan & Claypool Publishers, San Rafael, CA, ISBN 10-1598291904.)

[11] Soheli Farhana, A.H.M. Zahirul Alam, Sheroz Khan, Md. Ataur Rahman 2011 “Design of a Current Comparator for Quaternary Multi Valued Analog to Digital Converter”, IEEE Regional Symposium on Micro and Nanoelectronics (RSM), 190-194

[12] Sarada Musala;P. Durga Vasavi;B. Spandana;Avireni Srinivasulu;Cristian Ravariu 2022 A Novel 2:1 Multiplexer Based Quaternary Full adder IEEE International Symposium on Smart Electronic Systems (iSES)

[13] Anurag Chauhan;Lokesh Mahor;Piyush Tiwari 2020 Lowpower Quaternary adder Using Cnfet Ieee Vlsi Device Circuit And System (Vlsi Dcs)

[14] Satyendra R. Datla Mitchell A. Thornton Luther Hendrix, Dave Henderson 2009 “Quaternary Addition Circuits Based on SUSLOC Voltage-Mode Cells and Modeling with System Verilog”, 39 th International Symposium on Multiple-Valued logic pp.256-261.

[15] Ifat Jahangir, Dihan Md. Nuruddin Hasan, Nahian Alam Siddiquet , Shajid lslarn', Md. Mehedi “Design of Quaternary Sequential Circuits Using a Newly Proposed Quaternary Algebra” Proceedings of 2009 12th International Conference on Computer and Information Technology (ICCIT 2009), Dhaka, Bangladesh pp. 203 – 208.

[16] Ifat Jahangir 1 , Dihan Md. Nuruddin Hasan, Md. Shamim Reza “Design of Some Quaternary Combinational Logic Blocks Using a New Logic System”, Proceedings of TENCON 2009 IEEE pp.106-113.

[17] Motoi INABA, Koichi TANNO and Okihiko ISHIZUKA “Realization of NMAX and NMIN Functions with Multi-Valued Voltage Comparators”, Proceedings of the 31 st International Symposium on Multiple-Valued Logic 2001 IEEE pp.27 – 32

[18] Sarada Musala;P. Durga Vasavi,"A Novel Quaternary Multiplexer using CNTFET” 6th International Conference on Devices, Circuits and Systems (ICDCS) IEEE 2022