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Analytical Modelling and Performance Characterization of Hybrid SET-MOS

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Abstract: **-** Gordon Moore's "Moore's Law" suggests chip functionality demand doubles every 1.5-2 years, with global semiconductor technology roadmap recommending sub-nanometer ranges for IC production in nano-electronics. The single electron transistor (SET) is a promising nano-scale device that can be co-integrated with CMOS technology to improve performance. The paper explores the tunnelling effect between nanoparticles in single electron transistors (SET), revealing coulomb blockade transactions and resistance increases with reduced bias. It focuses on single electron transistors and pre-terminal devices, discussing IV characteristics, coulomb diamond plots, and metallic quantum dots. This research also explores the hybrid SET-FET based model, focusing on developing a room temperature SET in CMOS comparable technology with a Field Effect Transistor (FET). Prediction models and exploratory studies guide the integration of SET-FET technology. SIMON is a comprehensive simulator designed for single-electron devices and circuits. The output current is not impacted by capacitances up to 1 pF, and FET size in the micron range are appropriate for SET signal amplification up to 4 µA. This research explores the modelling of SET-FET technology in highlighting its ability to mitigate drawbacks in low drive current when combined with a FET. It also explores device variability mitigation in nanoscale array configurations, finding that SET-FET significantly reduces variability in larger arrays, despite the impact of capacitance and resistance.

Keywords: Nano-electronics, Single Electron Transistor, CMOS, Coulomb blockade, Electron tunneling, Transistor Modelling, SIMON.

I. INTRODUCTION

According to "Moore's Law" by Gordon Moore, the demand for chip functionality doubles every 1.5–2 years, a sign of successful semiconductor goods [1]. Due to the scaling of MOSFET technology, CMOS is approaching sub-nanometer ranges. The global semiconductor technology roadmap recommends sub-nanometer ranges for IC production [2]. Research on nanometer-scale materials is driven by Sumio Ijima's discovery of carbon nanotubes and Richard Richard's difficulties to miniaturization [3], [4].

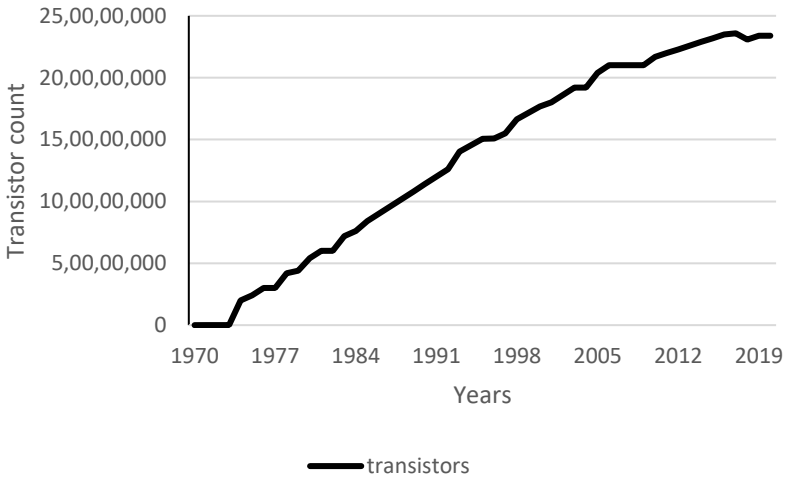

Figure 1. Moore's Law Applied to Technology Trend

Figure 1 shows Moore's law applied to technology trend. Moore's law governs Moore's law governs more than Moore, above and beyond Moore, allowing non-Si CMOS devices to scale IC performance and directing compact

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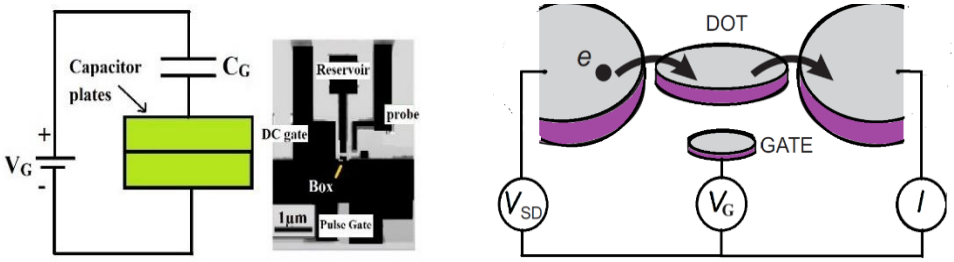
systems [5], [6]. Low power consumption and minimal latency are the goals of integrated circuit (IC) design for logic and memory devices [7]. Technology scalability increases performance but has drawbacks as well [8], [9], [10]. These problems can be solved by innovative nano-electronics devices, opening up new domains for information processing and heterogeneous 3D integration [11].

Three categories exist for MOSFETs: category-1, which integrates with current CMOS technology for lower power dissipation [12], [13]; category-2, which uses alternate channel materials for higher charge carrier velocity and mobility [14], [15]; and category-3, which includes new devices for specialized tasks [16], [17]. A promising nano-scale device that can be co-integrated with CMOS technology to improve performance is the single electron transistor (SET) [18]. The gaps in the previous research are SET are not modelled with FET and its characteristics regarding input are not given. The outline of problem is operating SET circuits at a suitable voltage for input/output (IO) and signal restoration is necessary for integration with nano-CMOS.

The transfer properties of devices such as single electron boxes [19] and single electron transistors, also known as quantum dots (QD) [20], [21]. These devices can be coupled to different voltage sources and can be referred to as single electron (singleton) boxes. A single electron box as shown in figure 2 (a) is a small conducting region that can be capacitively coupled to a voltage source and tunnel coupled to an electron source. The device has tunnel barriers at certain points and gates that are capacitively coupled to the small conducting region. The energetics of a single electron box are determined by the quantum dot being capacitively coupled to a gate. The number of electrons on the quantum dot is discrete, but the gate's charge induces a continuous charge on the QD. The total electrostatic energy of the QD can be calculated using the given expression, Energy of QD,

$$E_{QD} = \frac{(C_G V_G - Ne)2}{2C_\Sigma} \quad (1)$$

In the equation C_G represents gate capacitance, V_G represents gate voltage and N represents number of electrons and C_Σ represents the total gate capacitance. The equation for a parabola represents the charging energy or electrostatic energy of a quantum dot [22], with an effective total charge of $(C_G V_G - Ne)$. It is centered at an e and is represented by a curve as a function of the gate voltage. When the gate voltage is varied, the electrostatic potential of the dot is lowered or raised in a continuous manner, resulting in a parabola. At lower energy states like N or N+1, electrons fill the quantum dot. As the gate voltage increases, the levels in the dot decrease, and at some point, the next level of charging level becomes available, allowing the electron to fill that level. The number of electrons on the island or box is represented by the curve as a function of the gate voltage. At the bottom of the parabola, the energy level is represented by the energy level corresponding to the N electron and N+1 electron. When the gate voltage is varied, the parabola corresponding to the N electron and parabola corresponding to the N+1 electron meet at a degeneracy point. An electron fills the dot equally well with an electron and plus one electron. If the gate voltage is varied further, the dot fills by second electron and another electron. In summary, the electrostatic energy oscillates when two parabolas meet at a degeneracy point, causing an extra electron to be removed. This process is concerned with the drain or source of electrons, as the charging level on the dot is affected by the source of electrons [23], [24]. The single electron box exhibits a step-like behavior in total charge, with each electron charging one at a time [25].



(a) (b)

Figure 2. Schematic (a) Single Electron Box and (b) Single Electron Transistor Circuit

By adding one electron at a time, you can calculate the charge state of the island N, N+1, N+2 and so on. The singleton box has one tunnel junction connected and a capacitor on the other side. Modifying the geometry can lead to an interesting solution. Single Electron Transistor as shown in figure 2 (b) is a crucial and technologically significant device consisting of a conducting region called an island, which is capacitively coupled to a gate, providing source drain voltage and gate voltage. This allows for efficient and accurate operation of electrical systems [26]. When low voltage is applied to a system, the charging level within the energy window is not sufficient to overcome the single electron charging energy known as $\frac{e^2}{C_\Sigma}$, where $\frac{e^2}{2C_\Sigma}$ is used for each junction. When applying more voltage, the current will slowly rise in the opposite direction, blocking the current due to the coulomb repression of an electron. This phenomenon is called coulomb blockade. In situations where the source and drain do not have enough potential difference or the source is not applying enough potential to have an electron on the island and then off the island, the charging effect occurs. In this case, there is enough energy to allow an electron to pass through the system. The electron tunnels through the barrier. The charge state of the island or dot will go from N to N+1, with the next electron or energy state for the accelerator located high up. This requires twice the charging energy to put an electron there. This process is called single electron tunnelling, and it is controlled by source drain and a gate similar to a MOSFET or CMOS [27], [28], [29], [30]. This device operates in a regime where the effect of condensation of the charge or discrete nature of the charge is observed. The transport happens sequentially electron by electrons, one after another.

The effect of not having current flowing through when voltage is low is called coulomb blockade [31]. The quantum dot made up of aluminium. This examines the charging and discharging effect between nanoparticles deposited on aluminium filling, revealing thin transactions on both sides. The resistance increases as the differential resistance ($\frac{dv}{di}$) decreases with reduced gate bias. The derivative of this curve is a curve with an effective temperature, which smooths as temperature increases. The temperature effect contributes to the tunnelling process, with the sharp turn on the curve smoothing with temperature. The high temperature results in a sharp curve, while low temperature leads to a smoother curve. As temperature increases, the curve smooths and becomes faster. This behaviour is a collective behaviour of many nanoparticles, adding smoothness to the curve. The discussion is based on singleton transistors, pre-terminal devices with a source, drain, and gate. The current through the device is analysed as a function of source drain bias.

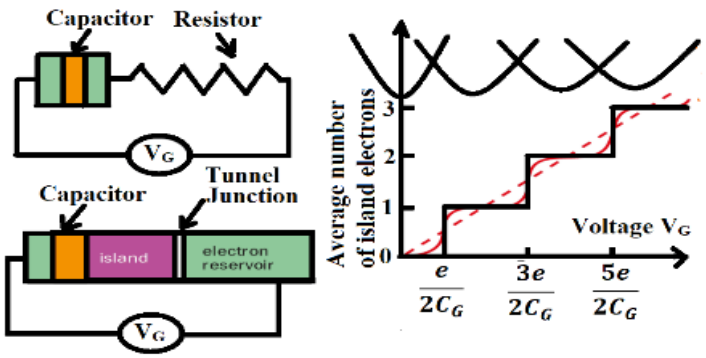


Figure. 3. SET Coulomb Blockade Oscillations

The figure 3 depicts the energy total energy versus gate voltage in a device. At the charge degeneracy point, electrons are favourable for moving on and off, or two charge states with the same energy. This transport occurs at these points, where nearby charge states regenerate. This process involves filling in, taking out, filling in, and taking out electrons from the source to the drain. As the gate voltage increases, electrons move through the parabola, reaching a point with a large energy difference between the two states. At this point, the charge state is locked in that position, preventing any transport of the system. As the gate voltage increases, the current decreases, eventually reaching a point where the two states are degenerate [32]. A periodic array of peaks in the current, known as coulomb blockade oscillation, is observed as a function of the gate voltage. This oscillation is arranged due to the phenomenon of coulomb blockade. Experimental data shows periodic oscillations as a function of gate voltage from a representative device. At this point, the current dies quickly as it moves away from

that point. The speed of driving depends on various factors, such as thermal broadening [33]. Higher temperatures broaden states, causing filled states to populate nearby states and a sharp distribution of states inside dots.

This research examines IV characteristics of devices when gate voltage is varied, focusing on current flow when bias can accommodate a level within its window [34]. Applying gate voltage can push these levels up at the lower bias, enabling the device to turn on at lower voltage. There are two ways to lift the current through a device: applying a large source and bias to overcome charging energy, or applying an extra charge through a gate, known as an induced charge. When applying large social bias, the current will turn on eventually, but pushing the levels into the window by a gate voltage can turn on the device even at lower voltage. Measuring these devices involves a combination of both methods, as this information is crucial for understanding the geometry of the device, known as the charge stability diagram or coulomb diamond plot. A coulomb diamond plot is a two-dimensional plot of current versus source and bias and gate voltage in a pre-terminal device. The current is coloured and varies with source and bias. The graph shows regions with no current flowing through, known as diamond-shaped regions. This is why it is called a coulomb diamond plot [35]. To analyse this plot in more detail, slices through it are taken. The graph shows that the current is a colour, with one axis representing source grain bias and the other axis representing gate voltage. This plot is a useful tool for understanding the behaviour of a device.

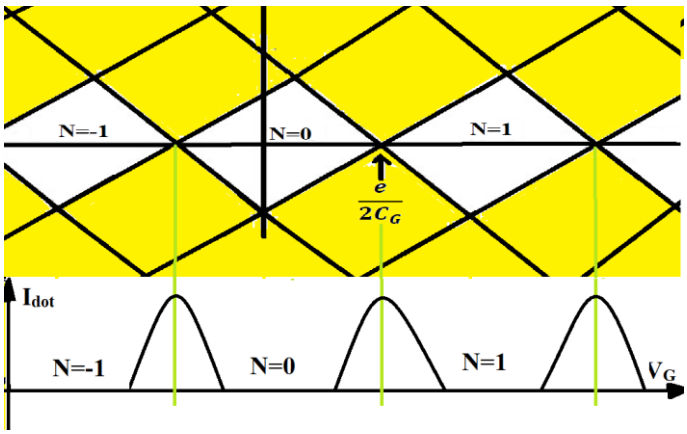


Figure. 4. SET Coulomb Diamond Plot

It found that a process of varying the gate voltage and bias in a circuit, resulting in a series of oscillations. The middle point has a very small bias, and the process is repeated at these points, resulting in a series of oscillations. The energy of two charge states is equal due to the parabolas crossing. A peak in current occurs when these states meet, and if a slightly larger bias is applied, the current can start flowing from there. This results in a broader peak with the same periodicity. Similarly, if slices along the bias voltage direction are taken, a blockade region in the middle will appear. When the charging energy overcomes this, the current turns on. To offset this, a small gate voltage can be applied, reducing the blockade region and turning on the current at a lower bias voltage. The figure 4 illustrates a process of reducing the blockade region in a diamond by applying gate voltage. The maximum blockade is present, but it is not symmetric. To reduce the blockade, start with the maximum voltage and gradually reduce it by applying more gate voltage. This results in a sloppy or triangle behaviour in the two-dimensional plot. When combined, the diamond shape is formed. The geometry of the diamond is the product of the distance from the sender to start the transport or the sender to the onset of transport, which should be the charging energy required to put an electron on the iron around the dot. The periodicity of the diamond should be $\frac{e}{C_G}$. This process helps in understanding the behaviour of the diamond in the process [36].

$$\Delta V_e = E_c = \frac{e^2}{C_\Sigma} \qquad (2)$$

$$\Delta V_G = \frac{e}{C_G} \qquad (3)$$

Diamonds have a stable charge with no transport and a locked resistance. The distance between two diamonds in the y direction equals one electronic charge, which is equivalent to adding one extra electron. The ΔV_G, the width of the diamond's height, is equal to C_G. By measuring the diamond's dimension, the total capacitance (C_Σ) and gate capacitance (C_G) can be obtained. This diagram provides information about the geometry of the dot, and with

many gains, the capacitance of all gates can be obtained by repeating the measurement with various gates. Column diamond acquisition is an important step in confirming the existence of a quantum dot, as it leads to a coulomb diamond. Without a column diamond, a quantum dot is not present. This is a textual measurement that confirms the existence of a well-defined, well-behaved quantum dot in a system. The study proposes a compact analytical model for Hybrid SET-MOS circuit modeling, which is computationally efficient and can improve the low power and high integration density capabilities of SET devices. This paper organized as follows: In section II, the SET modeling review is described. Section III, deals with the characterization and modelling method of SET.

II. SET MODELING REVIEW

Yun Seop Yu's research on single-electron circuit simulation reveals that SPICE macro-modeling can efficiently handle each coulomb island in large interconnections, reducing CPU time [37]. The paper presents a compact, analytical single-electron transistor (SET) model to help with the design and analysis of actual SET circuits. The steady-state master equation approach and correlated single-electron tunneling serve as the foundation for the model. It can accurately simulate MOSFET-based hybrid circuits and compute the properties of SET inverters. According to the model, in a fully symmetric SET, the SET current's gate voltage dependency shifts towards half of the drain voltage as a result of drain voltage [38]. Based on physical events seen in real-world Si SETs, a SPICE model for SETs was created. The model produced a good agreement with accuracy by combining the characteristics of parasitic MOSFETs with SET current. The model validated that hybrid multiple-valued logics (MVLs) based on CMOS/SET are feasible. Real Si SET effects and typical Coulomb oscillation were reproduced in a workable SPICE model. The model's efficacy at high temperatures was demonstrated by its successful application in simulating CMOS/SET hybrid multi-valued logic circuits [39].

Hybrid SET-MOS circuit modeling is suggested using a novel compact analytical model of single electron transistors. For symmetric or asymmetric SETs with one or more gates, the model is valid and takes eleven island states into account. Commercial circuit simulators such as SPICE may be used to implement the concept, which holds true for a wide range of drain to source voltage. The model has been confirmed using the Monte Carlo simulator SIMON and may be expanded for multiple tunnel junction SET (MTJSET). For both symmetric and asymmetric single electron transistors, the model replicates the properties of coulomb blockage and coulomb oscillation. By cross-checking findings using the Monte Carlo simulator SIMON, the correctness of the model is verified. The model may be used in conjunction with the SPICE environment and is created on the Verilog-A language platform [40]. The "ortho-dox theory" of single electron tunneling serves as the foundation for the proposed compact analytical single electron transistor (SET) model. It takes into account the background charge effect and is valid for an infinite drain-to-source voltage. It can also precisely define the drain-to-source current for symmetric or asymmetric devices. The model works well with typical MOS devices and is computationally efficient [41]. The low power and high integration density capabilities of SET can be further enhanced by hybrid SET-FET circuits. The hybrid circuit behavior is influenced by the position of the quantum dot (QD), having the most effects on I_D and SET in single SETs. Changes in QD size have a substantial effect on device variability in SET-FETs and other circuits based on SETs. Smaller tunnel junctions and higher current levels are connected to the significance of the size adjustment [42].

Single-electron transistors (SETs) are constructed from quantum dots (QDs), and the functional performance of these devices is determined by their properties. It is essential to analyze QD dimensions on hybrid SET-FET circuits. To get realistic model parameters, a self-developed SET compact model is employed. According to the research, gate-to-pillar distance has very little effect on output current, whereas QD size has the most impact on overall circuit performance. The circuit's electrical fields are altered by an extra voltage source, which enhances performance. The most important element influencing how a circuit behaves is its operation temperature [43].

The Abdelkrim uses a neural network to illustrate the electrical properties of a single-electron transistor with Aluminum Island, showing how its low energy consumption, fast speed, and simplicity make it suitable for analyzing nanoscale CMOS circuits [44]. The Klupfel has created a small model of a silicon-nanopillar single-electron transistor (SET). The model takes into account the quantum confinement of electrons on the quantum dot and computes tunneling currents using a master equation technique. Its parameters also include material characteristics and device shape. The model was used to mimic a ring oscillator and an inverter using HSPICE. Testing SET circuits under more realistic assumptions is possible thanks to model-based simulations. The model may be used to explore the impact of shape and doping modifications in a silicon-based SET on proposed

application scenarios and has strong quantitative agreement with SPICE simulations. It is possible to create compact models for different SET geometries using the model equations [45]. Using Master Equations and Orthodox theory, Phalguni Singh suggests an enhanced Monte Carlo model of a single electron transistor. The model is adjusted to investigate parasitic factors and how they affect the properties of the transistor. According to simulation results, there is a strong conductance peak and a noticeable Coulomb stair-case at the gate capacitance. Under particular gate capacitance levels, the Monte Carlo SET model is effectively tested, and the result validates the Orthodox theory [46].

III. CHARACTERIZATION AND MODELLING METHOD OF SET

The SET-based design modelling is based on a master equation SET circuit simulator as it allows faster and accurate circuit simulation. This research analyze the impact of operating temperature under appropriate biasing conditions, resistance, and quantum capacitance of SET and its ability to mitigate drawbacks in low drive current when combined with a FET. It also explores the coulomb blockade effect of SET, proving that room temperature operation of SET based on QD arrays is possible. Master equation modeling made simpler by merging it with macro modeling to provide the best possible SET modeling. The implementation of SET logic requires a strong relationship between electrical and physical characteristics. The operating temperature and electrostatic charging energy ($Ec = e^2/2C_S$) are crucial factors. The highest operating frequency and SET inverting voltage gain (C_G/C_j) are also important. To produce a dependable design with the least amount of error at room temperature, the charging energy (E_C) kept high as feasible in relation to thermal energy. The current design considers e^2/C_S = 40kBT, or capacitance between terminals. SET settings for room temperature operation and 0.789 V working voltage are used, with $C_S = C_D = 0.031$ aF, $C_G = 0.045$ aF, $C_B = 0.0532$ aF, and $R_S = R_D = 1.010$ MΩ based on prior research. The model configuration for SET current-voltage characterisation measurements is displayed in Figure 5. The drain to source voltage, control gate to source voltage, and tuning gate to source voltage are represented by the symbols V_{DS}, V_{GS}, and $V_{BS,}$ respectively.

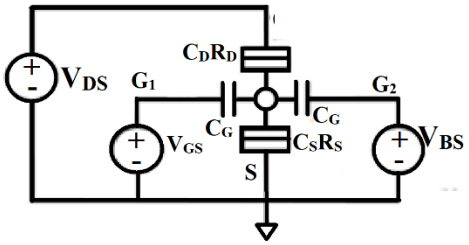


Figure 5. Model set up for current-voltage characterization

3.1 Hybrid SET-FET based Design

In this, a room temperature SET in CMOS comparable technology is explored with the goal of developing a hybrid circuit demonstration for low power electronics, particularly in conjunction with a Field Effect Transistor (FET). The manufacture of FETs is impacted by variables such as output current, pillar integrity, and thermal budget. A $Si/SiO_2/Si$ nanopillar layered with silicon nanodots in the oxide layer is the quantum tunnelling device (SET). Its former cryogenic working range is no longer applicable because of its low Coulomb blockade capacitance, which enables it to run at room temperature for quantum islands smaller than 5 nm. Although SETs have low power consumption and great sensitivity, large-scale manufacturing integration is still difficult. The integration and power consumption of SET and CMOS technologies might be enhanced by their combination. Benefits of FET technology include high input impedance, high voltage gain, and fast speed. Background noise and device instability can be resolved with hybrid SET-FET circuits. The mechanical and electrical robustness of CMOS devices has aided in their technological development. With a thorough grasp of CMOS processing, modeling, and integration, hybrid circuit designs are now feasible. Figure 6 illustrates the construction of a hybrid SET-FET circuit.

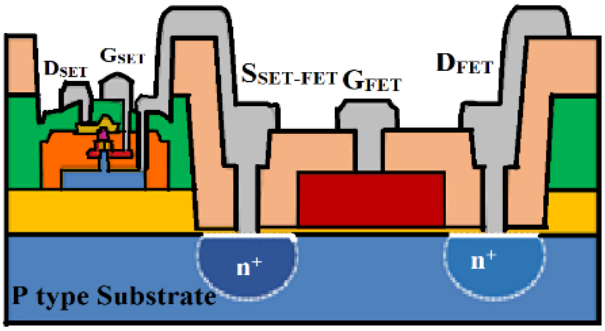


Figure. 6. Sketch for SET-FET hybrid device

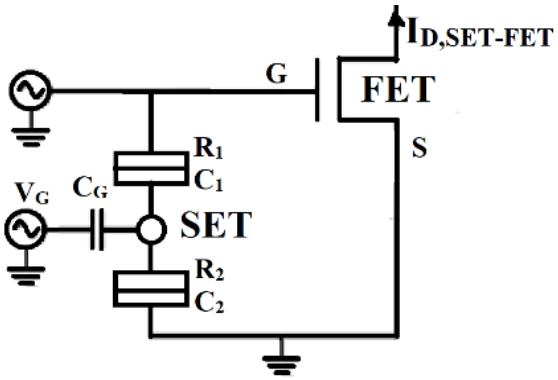


Figure. 7. Circuit for SET-FET hybrid device

Figure 7 shows circuit diagram for SET-FET hybrid circuit. Based on a reference CMOS technology from IMB-CNM, the hybrid SET-FET device represents a unique technological advancement. On the other hand, Nano Dots (NDs) may breakdown under high temperatures, rendering SET inoperable [47]. This results in a limited heat budget during the fabrication of Si NDs, leading to departures from standard parameters throughout the production process. Table 1 shows process specification of the device from the reference CMOS.

Table 1. The specifications of SET-FET model

Sr. No.	Process Specification	FET Compatible SET
1.	Substrate	P type SOI wafers, resistivity 8 – 22 Ω cm
2.	Field Oxide	The SOI buried oxide acts as field oxide
3.	Gate Oxide	Target of 36.5 nm as gate oxide
4.	Channel Implantation	BF3 gas, $1.7X10^{12}$ at/cm2
5.	Polysilicon	Polysilicon deposition by LPCVD
6.	Source/Drain region implantation	Phosphorous and Argon, $4.2X10^{15}$ at/cm2
7.	Metal Routing	Al-Cu deposition by sputtering

3.2 Hybrid SET-FET circuit modelling

SET-FET technology integration is achieved through a proven manufacturing approach, allowing for process parameter modifications and guided by prediction models effective integration. The drawbacks of SET are low drive current can be mitigated when combined with a FET. Figure 8 shows SET-FET small signal equivalent model.

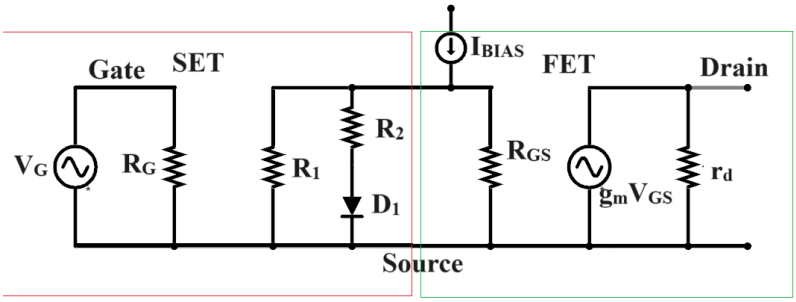


Figure. 8. SET-FET Small Signal Equivalent Model

$$R_1(V_G) = CR_1 + CR_2 \cos(CF_1 \cdot V_G) \quad (4)$$

$$R_2(V_G) = \frac{CV_P}{CI_2 - 2CV_P/R_1(V_G)} \quad (5)$$

From figure 8 the FET detects the gate signal with high input resistance, driving the load at the source, enabling the source potential to follow the gate voltage. The characteristic of the input-output may be written as,

$$\frac{1}{2}u_n C_{OX}\frac{W}{L}(V_{IN} - V_{TH} - V_{OUT})^2 R_S = V_{OUT} \quad (6)$$

One determines the small-signal gain of the circuit by adjusting both sides of (6) in relation to VIN.

$$\frac{1}{2}u_n C_{OX}\frac{W}{L}2(V_{IN} - V_{TH} - V_{OUT})\left(1 - \frac{\partial V_{TH}}{\partial V_{IN}} - \frac{\partial V_{OUT}}{\partial V_{IN}}\right)R_S = \frac{\partial V_{OUT}}{\partial V_{IN}} \quad (7)$$

Since $\frac{\partial V_{TH}}{\partial V_{IN}} = \left(\frac{\partial V_{TH}}{\partial V_{SB}}\right)\left(\frac{\partial V_{SB}}{\partial V_{IN}}\right) = \eta\frac{\partial V_{OUT}}{\partial V_{IN}}$,

$$\frac{\partial V_{OUT}}{\partial V_{IN}} = \frac{u_n C_{OX}\frac{W}{L}(V_{IN} - V_{TH} - V_{OUT})R_S}{1 + u_n C_{OX}\frac{W}{L}(V_{IN} - V_{TH} - V_{OUT})R_S(1+\eta)} \quad (8)$$

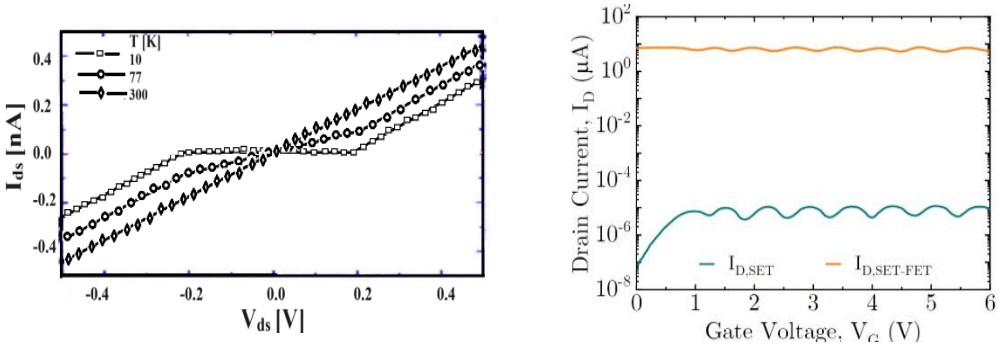
The text also emphasizes that

$$g_m = u_n C_{OX}\frac{W}{L}(V_{IN} - V_{TH} - V_{OUT}) \quad (9)$$

As a result,

$$A_V = \frac{g_m R_S}{1 + (g_m + g_{mb})R_S} \quad (10)$$

Equivalent circuit models consist of input V_G voltage to gate and having input gate resistance of 100 MΩ. Here R_1=300MΩ, R_2=100MΩ and R_{GS}=150Ω. To find input resistance the gate voltage is replaced by short circuit. Hence the resistance combination ($R_G \| R_2$) is 75MΩ. Then the combination (75MΩ+R1) is 375MΩ. Finaly (375MΩ$\|R_{DS}$) is 149Ω. Similarly R_{OUT} value obtained is 6.123MΩ. I_{BIAS} current is kept constant to draw the current $I_{DSET\text{-}FET}$ plot I_D. Measurements of Coulomb oscillations provide a clear definition of the I_{DS}-V_{DS} properties, with the current increasing as V_{DS} increases. The current $I_{DSET\text{-}FET}$ is oscillating, and it can be reduced by adjusting the array configuration as shown in the following example.



(a) (b)

Figure 9. Schematic (a) single electron box and (b) The SET-FET hybrid circuit voltage characteristics

A circuit that achieves low resistance without sacrificing the voltage gain of the SET stage is shown in figure 9 (a), the simulation carried out in SIMON simulator by varying input voltage from 0 V to 6V and the drain current is measured across it. Figure 9 (b) illustrates a SIMON simulation hybrid circuit current passing through the drain terminal of each component. The SET output current clearly shows oscillations related to Coulomb blockade; these oscillations persist beyond the FET and lead to an increase in current level (amplification). Consequently, the amplification factor of the circuit is shown. Peak-to-valley current ratio (h_{ID}), which may be improved with small adjustments to array designs, shows how much SET contributes to hybrid circuit current. This research examines the behaviour of circuits taking into account capacitance and resistance introduced by connections. The output current is not impacted by capacitances up to 1 pF, according to the results, and FET size in the micron range are appropriate for SET signal amplification up to 4 μA.

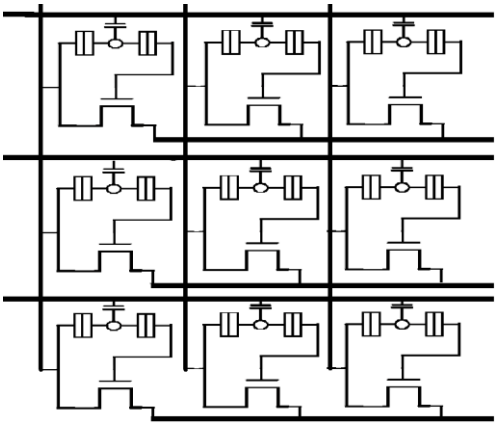


Figure. 10. SET-FET 3X3 array configuration

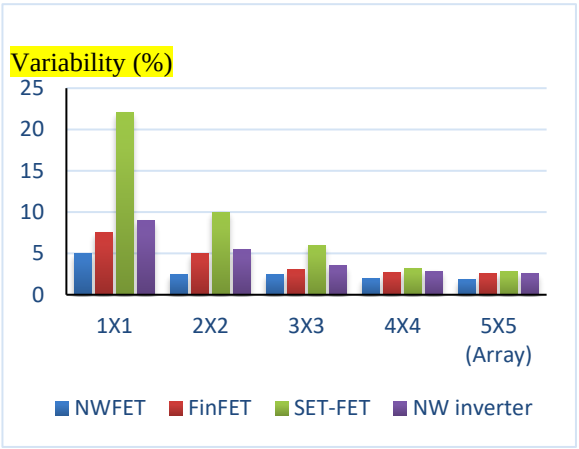


Figure. 11. Device variability has a substantial effect on various circuits with array configuration.

To remove out coulomb blockade oscillations as shown in figure 9 it is possible to connect SET-FET in array configuration. Stacking SET-FET on each other the array configuration can be made from 2X2 to 8X8 and so on. This experiment carried out in SIMON simulator. Simulations show that monolithic production of FETs and SETs significantly enhances the hybrid SET-FET circuit as shown in figure 10 having 3X3 SET-FET array configuration, proving the feasibility of merging planar FETs with vertical nanopillar-based SETs. This explores device variability mitigation in nanoscale array configurations using various architectures as shown in figure 11, revealing that SET-FET significantly reduces variability in larger arrays, indicating potential matrix distributions.

IV.RESULTS AND DISCUSSION

Our findings provide the development of a hybrid circuit for low power electronics, particularly in conjunction with a Field Effect Transistor (FET). The quantum tunnelling device (SET) is a Si/SiO2/Si nanopillar layered with

silicon nanodots in the oxide layer, which can run at room temperature for quantum islands smaller than 5 nm. SETs have low power consumption and great sensitivity, but large-scale manufacturing integration is still difficult. The integration and power consumption of SET and CMOS technologies might be enhanced by their combination. Benefits of FET technology include input impedance, voltage gain, and fast speed. Background noise and device instability can be resolved with hybrid SET-FET circuits. The mechanical and electrical robustness of FET devices has aided in their technological development. The table 2 shows the comparison between FET, SET and SET-FET circuit. The table illustrates that traditional FETs operate at a greater supply voltage of 1V. The SET circuit is a viable substitute as it only requires a supply voltage of 95μV and has a 10–20pA operating range. In this sense, SET-FET is superior to SET as it requires an even lower supply voltage—roughly 100 μV and has a 4 μA operating range.

Table 2. The Comparison between FET, SET and SET-FET circuit

Parameters	FET Circuit	SET Circuit	SET-FET Circuit
Supply Voltage range	100 mV- 1V	95 μV – 100 μV	100 μV – 100 mV
Current range	1-10 μA	10 pA -20 pA	1 μA - 4 μA
Maximum Voltage Gain	5	2.9	3
Operating Temperature	>300°K	<300°K	300°K
Maximum Switching Speed	10 GHz	15 GHz	12 GHz
Power Dissipation	625 mW	1 femtoW	225 mW

A hybrid SET-FET circuit is developed, with preliminary research on design and optimization, and modeling achieved using a proven manufacturing method allowing parameter modifications. The output current remains unaffected by capacitances up to 1 pF, and micron-sized FETs are suitable for SET signal amplification up to 4 μA. This explores device variability mitigation in nanoscale array configurations using array architectures, revealing that SET-FET significantly reduces variability in larger arrays, indicating potential matrix distributions. It shows monolithic production of FETs and SETs significantly improves the hybrid SET-FET circuit, demonstrating the potential of merging planar FETs with vertical nanopillar-based SETs.

V.CONCLUSION

A high-performance SET-FET model examines hybrid circuits integrating SETs with conventional MOSFETs, revealing larger current levels and coulomb blockade oscillations, enhancing circuit stability and demonstrating SET-FET performance at room temperatures. SIMON is a Monte Carlo circuit simulator that accurately simulates SET-FETs using the Master's Equation method, reducing device variability's impact on electric performance. Future research could explore SET-FET's potential for scalability and device integration, potentially driving new generation nano-electronic devices due to improvements in output current and higher integration.

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