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Analytical Modelling and Performance Characterization of Single Electron Transistor

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Abstract: **-** One important component of the present nanotechnology research field is single electron transistor (SET) which has unrealized quality to operate at breakneck speeds with ultralow power consumption. The single electron transistor is a novel nanoscale switching device that can regulate the motion of a single electron in addition to maintaining its scalability down to the atomic level. In this context, scalability refers to the ability of electronic device to function better as their dimensions get smaller. The basic device properties that this single electron transistor (SET) operates on "quantized current-voltage (I-V) characteristic," "single electron tunneling effect," and "Coulomb blockade," are also covered. This study presents some of the key SET-related topics, such as modelling and simulation methods. Simulation of Nanostructures Method (SIMON) is circuit simulator for tunneling device with just a single electron device based on Monte Carlo approach. It enables simulation of any kind of circuits with voltage source, junctions in tunnels and capacitors in quasi stationary mode and transient mode. The most significant feature of SET that is applied in the research work is Coulomb blockade oscillation, so at the conclusion of this paper, a number of simulations utilizing the SIMON simulator are shown. The simulation results show that for gate capacitance CG = 2af, C∑ = 3af, IBIAS = 2nA, tunnel barrier resistance RT > 4.1KΩ and operating temperature T=21K the model reflects real SET characteristic with maximum voltage gain.

Keywords: Coulomb Blockade, Device Modeling, MOS Technology, SIMON, Single Electron Transistor (SET).

I.INTRODUCTION

While a transistor with single electron and a typical transistor are comparable, there are several unique features in the former. A tiny dot becomes substitute for the channel, and it is isolated from the source and drain by a thin insulator. This is an important modification. There will be two junctions where tunneling occurs because electrons move from the source to the dot and subsequently from this dot to the drain. There are two junctions: one from the source to the island, and the other from the island to the drain. These unique characteristics set single-electron transistors apart from traditional MOSFET transistors [1], [2], [3], [4], [5], [6]. Based on the coulomb blockade effect, a SET is a sensitive electrical device [7]. The reason it is named a single SET is that the structure and tunneling are made in such a way that, in most cases, just one electron may cross to this tunnel junction at a time, allowing the electrons to flow in a highly regulated manner one by one [8]. At the electron level, carriers are moved under control. Additionally, this island has an electric potential barrier that prevents carriers from moving from source to drain and from island to island. In a transistor barrier replacement is possible through applied gate voltage. To enable an electron to move from its source to its island, it must first pass through the potential barrier named as the SET tunneling barrier. This potential barrier can be tuned by gate electrode which is capacitively in tandem to this island. The working of the SET depends on coulomb blockade effect. Coulomb Blockade: The coulomb blockade effect can be seen in a quantum dot since it is a nano dot structure with extremely tiny electrons placed inside [9].

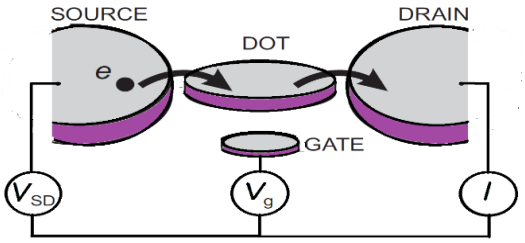

Figure. 1. Coulomb Blockade

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Electrons inside this quantum dot will create a strong coulomb repulsion preventing other electrons to flow. Thus, the device will no longer follow Ohm's Law. Coulomb blockade state says even if increase in potential difference current may not increase because this dot will not allow to come to this place so called coulomb blockade [10]. It is stated that the coulomb energy is

$$E_C = \frac{e^2}{2C} \quad (1)$$

It says that this energy is dependent on the capacitance so to add electron from outside this much energy is needed. Here, e represents the electron's charge and C the sum of the capacitances of the gate capacitor, source, and drain junctions. Since the extent of quantum dot is very small the Ec energy becomes very high [11].

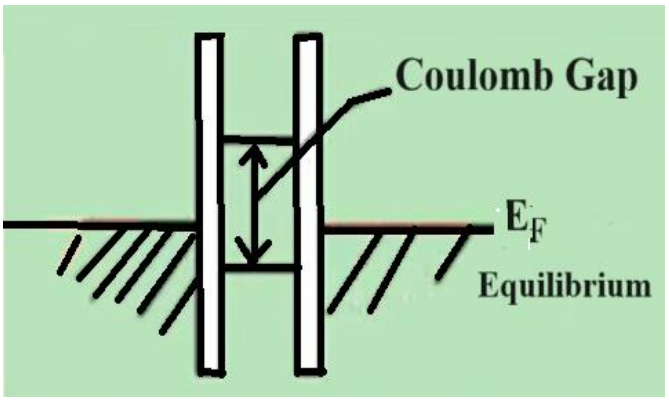

Figure. 2. Coulomb Gap

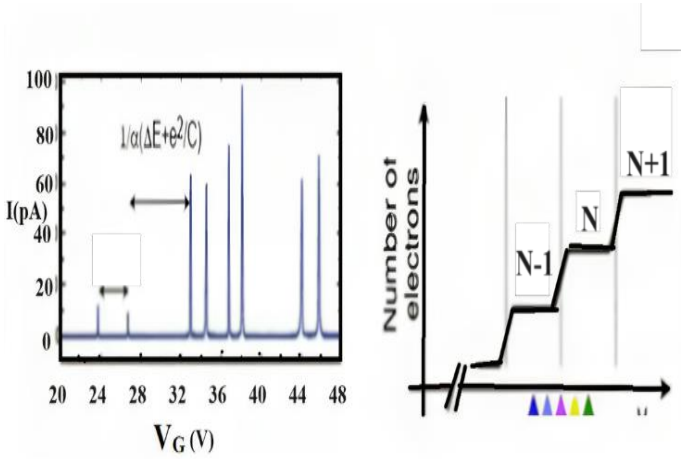

Figure 3. Quantized I-V Characteristic

To add extra electron to quantum dot need excess amount of energy because of quantum effect comes in to the picture the allowed energy states are discrete [12]. Energy states for the source and drain have the look of a continuous prohibition, but in the quantum dot allowed energy states are discrete [13], [14]. If the electron have to move from one side source to other side drain it have to cross this gap only then new electron will get added here. The coulomb gap increases if size of quantum dot decreases. Consider that N number of electrons are present in QD and adding one electron i.e. N+1 electron will go to new higher state. When this energy exceeds the thermal energy then single electron charging can be detected [15]. This means when the thermal energy is low coulomb blockade effect can be observed. At surrounding temperature electrons have 25million eV energy then dimensions should be less than 10nm [16]. Coulomb blockade gives an opportunity to control current by controlling the movement of single electron.

1.1. Quantized IV Characteristic

To add electron from source to dot then we have to supply energy at least equal to coulomb energy ($e^2/2C$). The energy will be applied by applying suitable potential so the energy is quantized. Only for coulomb energy one electron jump from source to QD. Once the movement of an electron is detected the current peak is observed [17]. Further movement is stopped till supply another big jump into the energy. So the current peaks are a discrete peaks at discrete voltage levels [18].

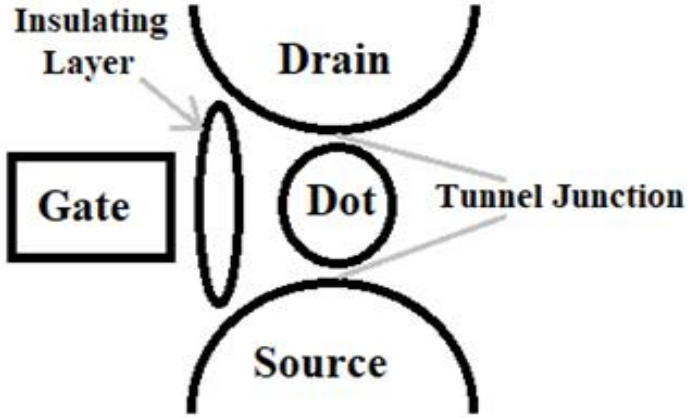

Figure. 4. SET schematic diagram having quantum dot

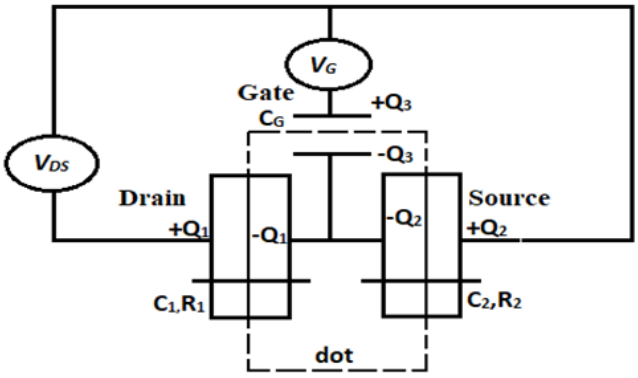

Figure. 5. SET equivalent Diagram with Gate Capacitance

The two possible designs for an SET are: Symmetric SET and Asymmetric SET [19]. In symmetric SET, to thermally decouple both the leads from the environment, the source and drain are made from a very narrow and small volume island. In asymmetric SET, the drain is in line with a bulky electrode while the source is made narrow and small to separate it from the environment [20]. Fig.4 below shows an SET view and Fig.5 shows equivalent circuit. In single island SET, the relation between source-dot (R_2) and dot-drain (R_1) gives its resistance while the total capacitance is characterized as sum of dot-drain capacitance (C_1), source-dot capacitance (C_2), and gate-dot capacitance (C_G) [21]. When no bias is applied, island is in neutral state while Fermi levels of both 'source' and 'drain' are in equilibrium [22]. On applying bias voltages, gate voltage (V_G) and drain-source voltage (V_{DS}), the charge carriers start to tunnel from source to drain through tunnel junction via dot [23], [24]. Thus creating a charged island due to its interaction with gate (Q_3), drain (Q_1) and source (Q_2).

When a carrier is tunneling through junction, the repulsive force between carriers decreases the chance of flow of other charge carriers thus allowing carriers in SET to tunnel one by one. This phenomenon is known as coulomb blockade effect i.e. the energy needed to charge the capacitor is $\frac{e^2}{2}$, the electron transfer will be blocked at sufficiently lower temperature if this energy is not provided [25], [26].

1.2. Requirements for room temperature operation

For quantum mechanical effects the kinetic energy E_k should be taken in to account, then the thermal energy E_a can be given as

$$E_a = E_c + E_k + E_t \quad (2)$$

For the transfer of the energy required for charging a single electron E_c must be greater than thermal energy else without applying energy the electron will transfer to island due to thermal excitation [27]. Hence for room temperature operation following is main requirement,

$$\frac{e^2}{2C} \gg k_B T \quad (3)$$

From Heisenberg's uncertainty principle

$$\Delta E_c \Delta t \geq \frac{h}{2} \quad (4)$$

Where Δt is charging time of tunnel junction, it can also given as R_TC. The R_T is resistance of the tunnel barrier and its obtained value is

$$R_T \geq \frac{h}{e^2} \cong 4.1K\Omega \quad (5)$$

Hence the second requirement for room temperature operation is $R_T \gg 4{,}1K\Omega$ [28].

The study demonstrates that SET acts similarly to FETs, possessing voltage-controlled properties, and can be utilized for designing and analyzing current mirrors, amplifiers, comparators, and oscillators [29]-[33].

The structure of this article is as follows: In Section II, the background work for SET modeling and simulation is explained. Section III provides an explanation of single electron transistor with modeling. Section IV discusses the simulation approach and performance metrics of various SET parameters; Section V delivers the conclusion.

II.REVIEW

Uchida et al.'s SET's first tiny analytical model works well at a wide range of temperatures. For asymmetric and poly-gate SET, it is inappropriate., though, as it ignores the previous back charge impact [34]. This particular model was expanded to include asymmetric devices by Inokawa also by Takahashi [35]. In light of a straightforward analytical model, Lee. created a workable model for silicon SET at initial instance [36]. This model would be very helpful for assessing the execution of realistic SET–MOS hybrid circuits because it was designed in accordance with the realistic SET [37], [36], [37], [38], [39], [40].

Mahapatra et al.'s Mahapatra IB model can be utilized in symmetric or asymmetric, single- or multi-gate devices. The Mahapatra IB model restricted the range of Vds to 3e/CR by integrating unidirectional electron flow and only four island-states (~1, 0, 1, 2). It seems that this range is more than adequate for both analog and digital operation [41], [42]. The above range is insufficient for reliable functioning because high temperatures and strong drain biases increase the presence of incorporating additional charge states [43]. Furthermore, the Mahapatra IB The model does not permit inspection of the staircase-like properties for asymmetric SET.

III.MODELING OF SINGLE ELECTRON TRANSISTOR

To find out input and output parameter of SET we need to model SET. Fig.6 shows single electron transistor internal electrical components and Fig.7 shows equivalent circuit of SET. The output characteristic between drain and source terminal has composed of two branches, each branch composed of resistances, voltage sources and diodes. These are represented as R_2, V_p, D_2 and R_3, $-V_p$, D_3 respectively. During $+V_{DS}$ bias voltage and $-V_{DS}$ bias voltage, there always adequate current flowing through the branch. The charging energy E_c is acquired on frequent intervals using cosine of the gate bias with R_1, R_2, and R_3.

$$R_1(V_G) = C_1R_1 + C_2R_2\,cos(C_1 \cdot V_G) \quad (6)$$

$$R_2(V_G) = R_3(V_G) = \frac{CV_p}{C_2 - 2C_2V_p/R_1(V_G)} \quad (7)$$

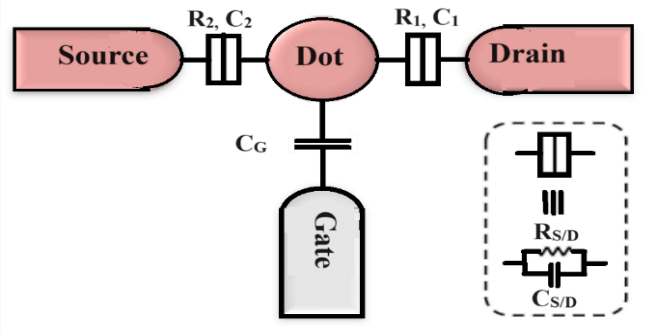

Figure 6. Single electron transistor internal electrical components

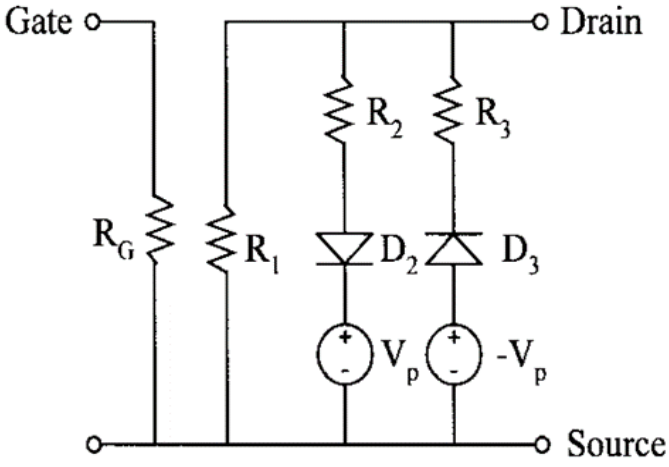

Figure. 7. Equivalent circuit of single electron transistor

Derivation of the Model:

Using the steady-state master equation approach and the "orthodox" theory as our foundation, we derive the model of analysis for a double-junction SET [44], [45], [46]. The steady-state master equations be computed with accuracy using the above-described assumptions. As a outcome, the behavior of SET current through voltage with current tunneling or next tunneling electrons in its island are given by,

$$I = \frac{e}{2R_T C_T} \frac{(V_{GS,n}{}^2 - V_{DS}{}^2) sinh(V_{DS}/T_{TOTAL})}{sinh\left(\frac{V_{GS,n}}{T}\right) - V_{DS}\, sinh\left(\frac{(V_{DS,n}}{T}\right)} \quad (8)$$

where

$$V_{GS,n} = \frac{2C_G}{e} - \frac{(C_G + C_S - C_D)V_{DS}}{e} - 1 - 2n \quad (9)$$

$$V_{DS} = \frac{C_\Sigma V_{DS}}{e} \quad (10)$$

$$T_{TOTAL} = \frac{2k_B T C_\Sigma}{e^2} \quad (11)$$

and R_T=R_1+R_2. Notably, the dependency of current I on V_{GS} exhibits a symmetrical hump structure peaking at $V_{GS,n}$=0. Thus; it makes sense to assume that I equals one period of Coulomb oscillations. As a result, by adding $V_{GS,n}$=0 to equation (2), we ascertain the gate voltage corresponding to the peak of the Coulomb oscillation as,

$$V_{GS} = \frac{e}{2C_G} + \frac{ne}{C_G} + \frac{(C_G + C_S - C_D)V_{DS}}{2C_G} \quad (12)$$

With the Coulomb oscillation period, $\frac{e}{C_G}$, we can determine the gate terminal voltage V_{GS} range where the model current In remains consistent as,

$$\frac{ne}{C_G} + \frac{(C_G+C_S-C_D)V_{DS}}{2C_G} < V_{GS} < \frac{(n+1)e}{C_G} + \frac{(C_G+C_S-C_D)V_{DS}}{2C_G} \quad (13)$$

which is equal to -1 < $V_{GS,n}$ < 1.the current I over a desired voltage gate range gives the Coulomb oscillations as shown in Fig.8.

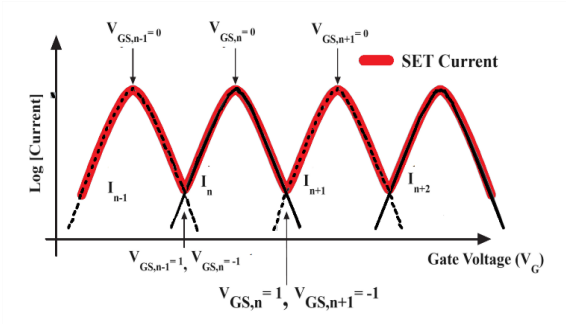

Figure. 8. Diagram showing the SET current (the gray line) and the model current (the dotted line). Current I characterize a single coulomb oscillation period. Coulomb oscillations are produced by adding the values of I over a chosen gate voltage range.

In fabrication atomic force microscope oxidizes GaAs/AlGaAs heterostructure surface layers, forming tunnelling barriers. The height of these barriers can be tuned, allowing for the fabrication of a side-gated single-electron transistor [47], [48], [49], [50].

1.3. SET implementation

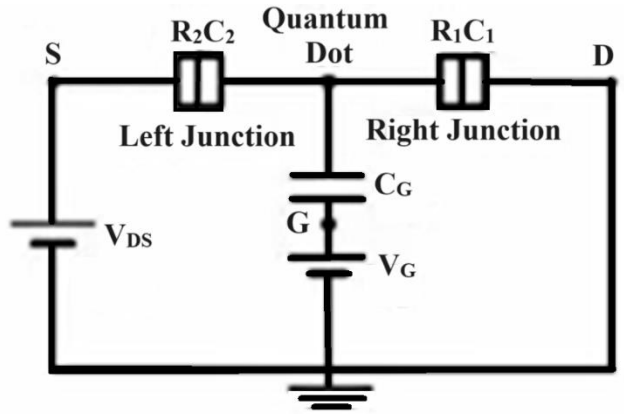

Figure 9. SET Transistor Implementation

SET transistor implementation has QD separated from source and drain by insulating layer capacitance that is source capacitance and gate capacitance respectively. The gate terminal introduces gate capacitance. SET can electrostatically be controlled via the C_G gate capacitance. Thus the total capacitance of the island is given by,

$$C_T = C_G + C_D + C_S \quad (1)$$

The potential energy needed to move electron from source to drain through this island that potential can be modified with the help of gate terminal. As the C_T is addition of source capacitance, drain capacitance and gate capacitance E_C (Forbidden gap energy) required to move electron decreases.

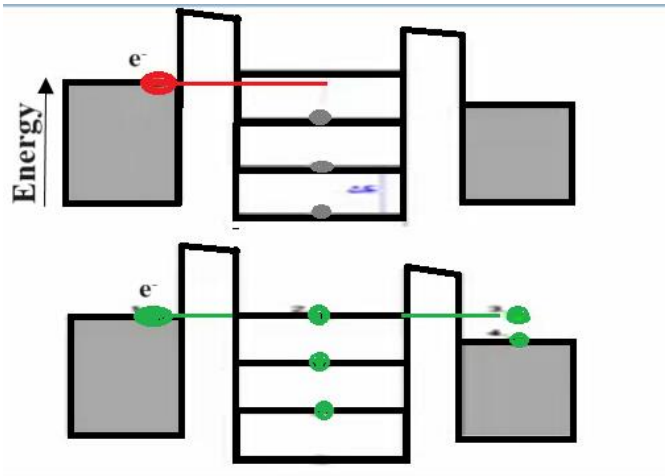

Figure. 10. Forbidden gap energy diagram of SET.

The Forbidden gap energy diagram shows source, quantum dot and drain in energy level form. Amid the source and QD it has insulating energy level, the dot have quantized energy levels. The gaps of QD depend on its size and capacitance. If size is less gap will be more. When some voltage is applied on gate terminal bending of forbidden energy gap in downward direction for a certain voltage. The forbidden energy gap aligned in such a manner that the electron can easily move from source to drain.

IV.SINGLE ELECTRON TRANSISTOR SIMON SIMULATION

There are three main methods for simulating single electron circuits: SPICE macro-modeling, Monte Carlo based, and Master Equation based, each with its own unique approach to the simulation process. SPICE, a faster single-electron simulator, can model the IV characteristic of single-electron transistors, but lacks Coulomb interaction, which can be resolved with pre-processing steps[51], [52], [53].

The Monte Carlo approach simulates electron transport through networks by calculating probabilities and randomly selecting events, compared to the traditional single-electron theory's tunnel rate equation [39].

The Master Equation is a matrix exponential equation system, but its numerical evaluation is challenging due to infinite states and unknown states. Adaptive schemes offer advantages for small circuits [54].

SIMON is simulation tool used to simulate single electron transistor [55]. As rapid growth in electronics industry there is need to understand fabrication of nanoscale transistors. SIMON gives simulation of quantum dot with coulomb blockade effect. Employing Monte Carlo approach. Any circuit with input terminal, air gap, electron storage, potential barrier and different voltage sources as like linear, nonlinear and constant. The dependent, and voltage controlled—can be temporarily or permanently simulated with it.

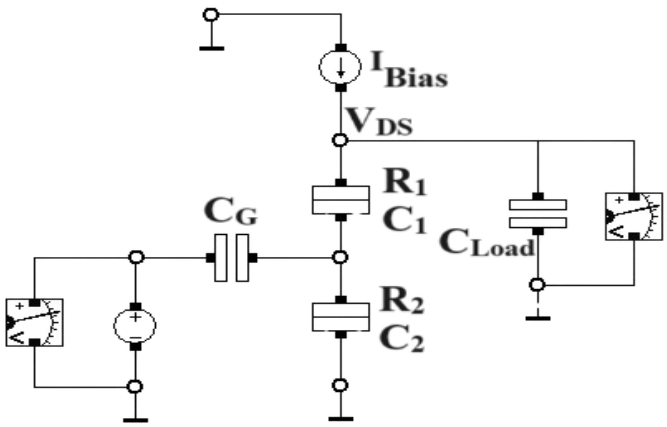

Figure. 11. Schematic diagram of SET-SIMON model

The figure 1 shows SET includes extra capacitor C_{Load} circuit for SIMON simulation. Given parameters as per table 1.

Table 1. Simulation Parameters of SET

Sr. No.	Parameter	Values
1	Junction Resistance R_1=R_2	1MΩ
2	Junction Capacitance C_1=C_2	1af
3	Gate Capacitance C_G	2af
4	Biasing Current I_{BIAS}	2nA
5	Loading Capacitance C_{Load}	100af
6	Operating Temperature	1K
7	Background Charge	0
8	Gate to Source Voltage (Range)	0 to 80mV

V.RESULTS AND DISCUSSION

We can observe that by changing every one of the subsequent parameters one at a time:

5.1 Effect of Loading Capacitance

The loading capacitance values are C_{Load} =1aF, 10aF, 100aF and 1fF respectively. For four different loading capacitance four V_{DS} oscillations obtained as shown in figure. 12.

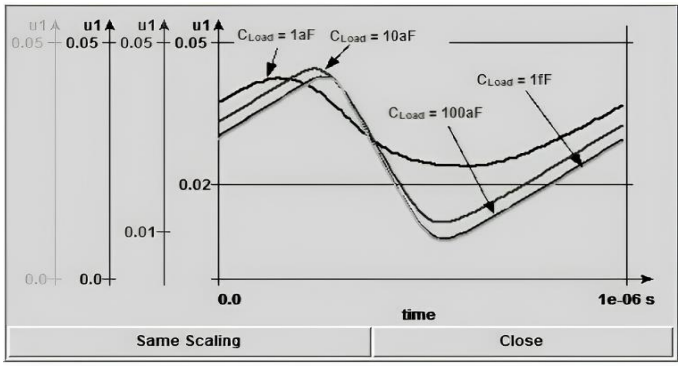

Figure. 12. CLoad impact on VDS oscillation, where loading capacitance values are C_{Load} =1aF, 10aF, 100aF and 1aF respectively

It's been noted the V_{DS} oscillation is impacted by modest C_{Loads}, or less than 10aF. The true SET characteristic may be seen in the V_{DS} oscillation when the C_{Load} is more than 100aF. This suggests that interconnected SETs will influence one another as we construct big SET-based circuits. A sizable grounded C_G >100af must attached for counteract this effect.

5.2 Effect of biasing current:

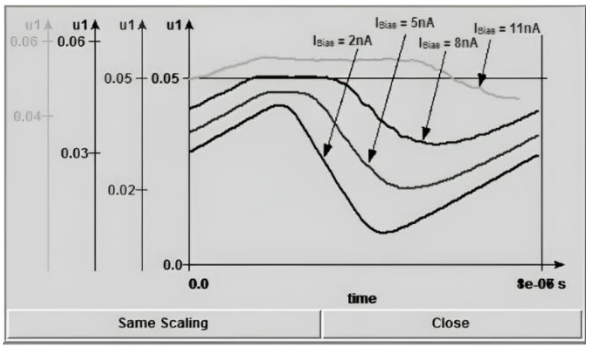

Figure. 13. I_{Bias} and V_{DS} curve

Four V_{DS} oscillations are accumulated with I_{Bias} increasing in steps of 3nA, from 2nA to 11nA (Figure 13). While the amplitude of V_{DS} reduces I_{Bias} increases. I_{Bias} for this cannot be greater than 10nA to maintain Coulomb oscillation. I_{Bias} can reach few hundred nA if device capacitance and junction resistance are further decreased.

5.3 Implications of the device's overall capacitance (C_Σ)

Three V_{DS} oscillations are obtained as per Figure 14.

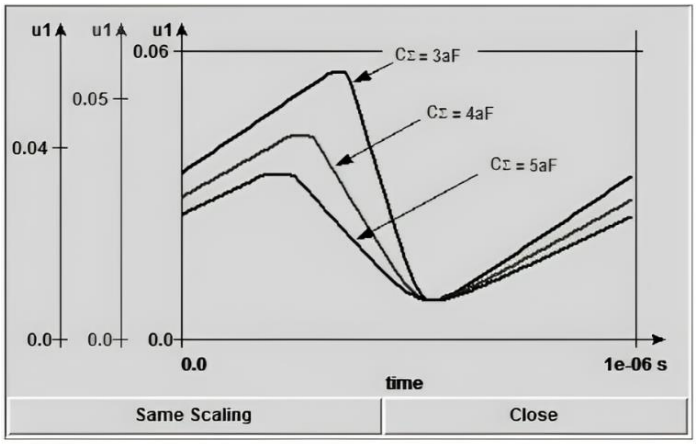

Figure. 14. Effect of C_Σ on V_{DS}

Amplitude of V_{DS} diminish with an increase in C_Σ; that is, the lowest V_{DS} stays constant but the maximum V_{DS} drops. At almost absolute temperature, the $V_{DS}\ \alpha\ \frac{1}{C_\Sigma}$ represented as $\frac{e}{C_\Sigma}$.

5.4 Impact of capacitance in the input gate (C_G)

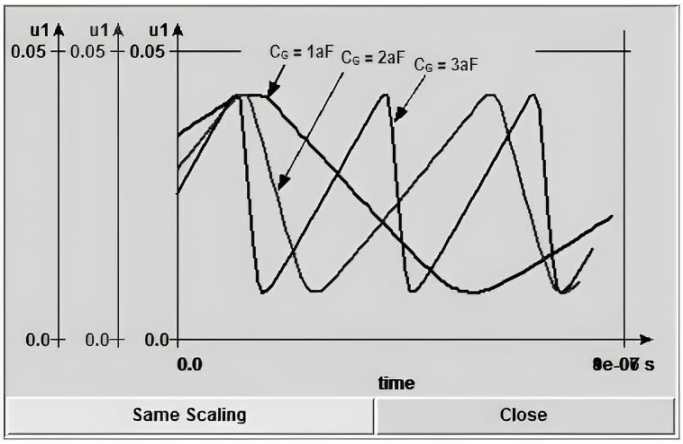

Figure. 15. C_G vs V_{DS}

As seen in Figure 15, we obtain three V_{DS} oscillations with C_G. It is discovered that periodicity of the V_{DS} oscillation reduces with increasing C_G. The $V_{DS}\ \alpha\ \frac{1}{C_G}$ is represented as $\frac{e}{C_G}$.

5.5 Impact of Temperature

In the model simulation of SET, it shows that as temperature increases the V_{DS} starts to decrease as shown in figure 16. For proper operation of SET the temperature should not exceed beyond 100K. The perfect operating temperature for SET is 15K. It also shows that if total capacitance i.e. C_Σ<3af the SET can properly work at room temperature.

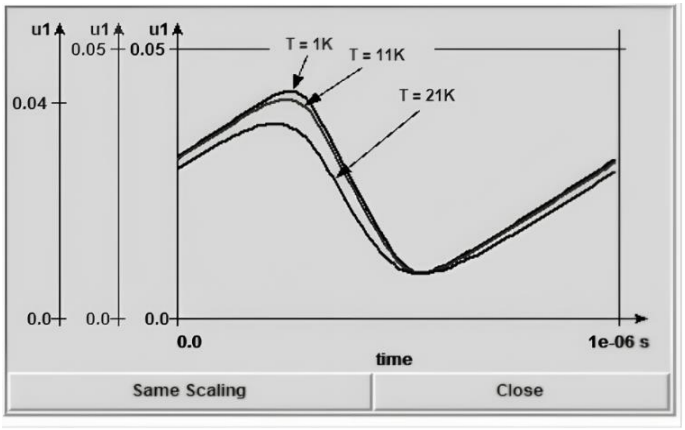

Figure. 16. Effect of temperature on SET operation

Table 2. Simulation Results reflects the real SET characteristic

Sr. No.	Parameter	Values
1	Loading Capacitance C_{Load}	100af
2	Biasing Current I_{BIAS}	2nA
3	Device's overall capacitance	3af
4	Gate Capacitance C_G	2af
5	Maximum voltage gain	K_v=6.5

VI.CONCLUSION

This research evaluates SET model by taking into account different SET parameters. The SET model's parameters are evaluated using SIMON simulation. The analytical model in SIMON simulation is created using a steady-state SET master equation method. The study uses the SIMON simulator to study Coulomb blockade oscillation in SET, revealing that VDS oscillation amplitude decreases with increasing device capacitance and input gate capacitance.

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