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A LVDS Transmitter with Low-jitter PLL and Pre-emphasis for Serial Link

A high-speed low-voltage differential signal (LVDS) transmitter adopts an improved feedback structure to stabilize the output current and the common-mode voltage of the differential signal. Meanwhile, a conventional VCO and pre-emphasis circuit is improved to reduce jitter and inter-symbol interference in the transmission line. The transmitter is implemented in 0.13□m standard 1P8M CMOS process and integrated into a high speed SERDES (Serial and De-serial) chip. The test results of the SERDES show that the differential swing voltage and common-mode voltage of LVDS are 450mv and 1.2V, respectively. The pre-emphasis compensates enough channel loss at 1.5 Gb/s. The total power consumption of the transmitter is 80mW at 1.5Gb/s.

Keywords: Transmitter, PLL, SERDES, differential signal, LVDS.

1. INTRODUCTION

With continuous improvement of the integrated circuit technology, the demand for higher data throughput in electric system is increasing rapidly. As a solution, low-voltage differential signal (LVDS) transmitter has been widely investigated [1, 2]. LVDS transmission technology is a current signal transmission technology, with the logic level determinate the current direction (clockwise or counterclockwise) in the loop[3]. In LVDS transmitter, a clock generator produces high speed sampling clock signal to serialize the parallel input data. The serialized data is then driven by the LVDS driver. To lower the jitter of the output signal, the LVDS transmitter needs a low-jitter clock generator and a LVDS driver that can keep the output current stable. In addition, as high-speed data is being transmitted, the transmission line behaves as a low-pass filter. The high-frequency components of the waveform of the data sequence are filtered, which smooth the bit transition edges and lead to inter-symbol interference (ISI)[4,5,6]. To reduce ISI, a common practice is to adopt the pre-emphasis technology that can reduce the attenuation of the high frequency components of the differential signal [2, 7, 8].

In this paper, a traditional voltage feedback method of the differential signal transmitter is improved to keep the output signal stable [2, 9, 10]. Furthermore, the improved pre-emphasis circuit is designed to overcome the loss of the high-frequency components of the differential signal, and a novel cross-couple VCO is proposed to reduce the clock jitter.

This paper is organized as follows. In section 2, the transmitter circuit structure and its principle are described. In section 3, the details of the transmitter are presented and analyzed. The test results of the transmitter are presented and analyzed in section 4. Finally, the conclusions are drawn.

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2. LVDS TRANSMITTER SYSTEM BLOCK DIAGRAM

The LVDS transmitter system block diagram is shown in Fig.1. It is mainly composed of the clock generator, the serializer and the driver. The transmitter uses high-speed clocks (CLK and CLK_B) that are generated by clock generator serialized parallel data (P_TX) and sent it to the driver. The LVDS driver converts the digital CMOS logic signal into LVDS and provides sufficient current to drive a coaxial cable with 50 Ohm characteristic impedance.

The clock generator is implemented with a self-biased PLL to achieve high process tolerance and low-jitter performance [11]; it includes phase and frequency detector (PFD), charge pump (CP), bias-voltage generator (BG), voltage-controlled oscillator (VCO) and the divider. The system reference frequency is 75MHz and the divider factor is 10, output clock (CLK and CLK_B) frequency of the PLL is 750MHz

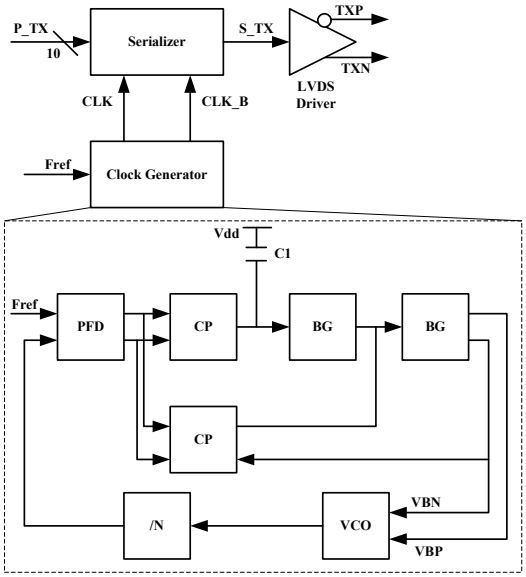

Figure. 1 Transmitter system block diagram

3 LVDS TRANSMITTER CIRCUIT DESIGN

3.1 PLL design

In differential signal transmission system, bit error rate (BER) is relative with the jitter of the system closely. Therefore, a low-jitter self-biased PLL is employed in this paper. As the self-biased PLL be concerned, $\zeta \propto \sqrt{C_B / C_1}$ and $\omega_N / \omega_{REF} \propto \sqrt{C_B / C_1}$ show that the parameters of the PLL can be adjusted thought C_1 [7, 8], where $\zeta, \omega_N, \omega_{REF}, C_B$ and C_1 are damping factor, loop bandwidth, input reference frequency, the total capacitance of the output node of the VCO and loop filter capacitor, respectively.

The phase detector (PD), charge pump (CP), bias-voltage generator (BG) of the self-biased PLL are described in paper [11]. VCO is a pivotal circuit and shall be designed carefully.

According to the VCO jitter theory [12], the jitter variance σ_j is presented by

$$\sigma_j^2 = \frac{2kT}{C \ln 2 \, dV_{od}/dt}[\gamma(3/4V_{effd} + 1/V_{efft}) + 1/V_{op}] \quad (1)$$

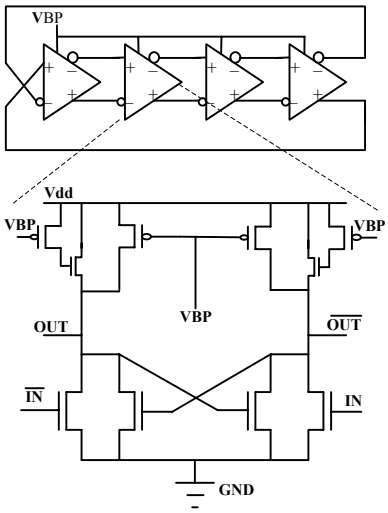

Figure. 2 The circuit schematic of VCO

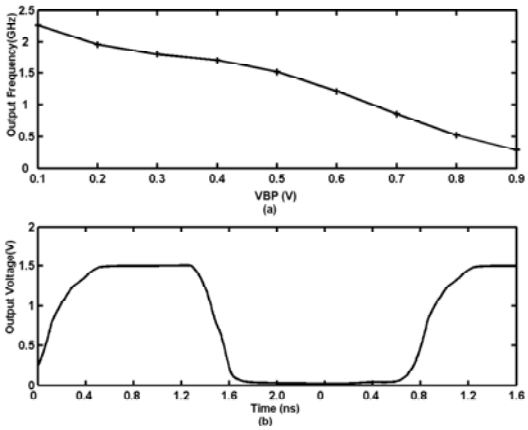

Figure.3 (a) The tuning sensitivity of VCO (b) The transient simulation waveform of the VCO

where V_{od} , γ , V_{effd} , V_{efft} and V_{op} , are differential output voltage swing, noise factor, the effective gate voltage on the differential pair, the effective gate voltage on the tail current source and differential peak output voltage swing, respectively. From equation (1), the jitter of the VCO is related with the output voltage swing. On the other hand, voltage swing is decreased with the power supply reduced. It is also shown that only when the ring VCO has a fully-swing output and high efficiency of current switching capability, its jitter performance could reach that of LC-tank oscillators [13]. For the reason mention above, the cross-couple VCO are researched before [14,15]. Unfortunately, the voltage tuning range of the VCO that proposed in [14] is too narrow to be suitable for applications that need wide voltage tuning. To overcome that drawbacks, an improved fully-swing differential VCO is

designed, which adopt cross-couple active inductors load to get low-jitter performances, as shown in Fig.2. When the power supply is 1.5V, the tuning sensitivity and the transient simulation results are shown in Fig.3.

3.2 The LVDS driver design

The LVDS driver converted the CMOS logic signal into LVDS; it must have stable drive current to drive the coaxial cable. Meanwhile, the common-mode output voltage must be kept in some range to ensure the LVDS receiver can receive it correctly. To decrease the jitter of the output signal and stabilize the common-mode voltage of the differential signal, the driver adopts an improved voltage feedback structure. As shown in Fig.4 (a), the constant current source provides the output current I_c. Transistors (M7-M16) make up of the current pre-emphasis circuit.

As shown in Fig.4 (a), the voltage fluctuation status of the node VF_N (or VF_P) is feed back through the transistors MP and MN. Therefore, the voltage of node Vo is clamped at a relatively stable value. By setting the voltage of the reference node (Vref_N), the voltage of the node Vo can keep constant to stabilize common-mode voltage of the output differential signal and the output current of the LVDS driver.

High-speed data-communication suffers from Signal Integrity [6, 16]. In practice, edge-current enhancement is a valid technology for high-frequency component compensation [17]. It is to apply a finite-impulse response (FIR) filter to the original sequence x(k) in order to produce a new transmitted sequence, named y(k) . The common FIR filter with two coefficients (a_1, a_2) writes by [18]

$$y(k) = a_1 x(k) + a_2 x(k-1) \tag{2}$$

whose frequency response is

$$H(\omega) = a_1 + a_2 \exp(-jwT) \tag{3}$$

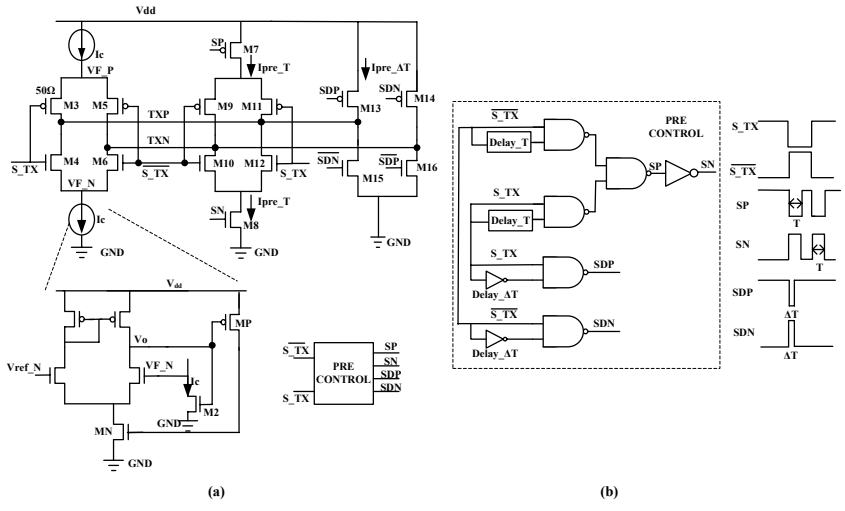

Figure.4 The circuit schematic of the LVDS driver (a) The schematic of the LVDS driver (b) Pre-emphasis control circuit and its signal waveform

where T is the unit interval of the x(k). It's noted that the system, which frequency response is same as equation (3), cannot detect the edge state of the sequence such as "010101…". To solve this drawback, an improved pre-emphasis circuit is designed.

Pre-emphasis circuit includes control circuit (PRE-CONTROL) and current density enhanced circuit. As shown in Fig.4 (a), the improved pre-emphasis circuit with three coefficients (a_1, a_2, a_3) and the new transmitted sequence can be wrote by

$$y(k) = a_1 x(k) + a_2 x(k-1) + a_3 x(k-\varsigma) \tag{4}$$

where $\varsigma \in (0,1)$ is the ratio of the delay to the unit interval of the x(k), a1, a2, a3 are coefficients respectively.

According to Fig.4 (a), the output current of the driver is presented by

$$I_{out} = I_c \cdot S\_TX + I_{pre\_T} \cdot \overline{SP} \cdot SN + I_{pre\_\Delta T}(\overline{SDP} + SDN) \tag{5}$$

where I_c, I_{pre_T} and $I_{pre\_\Delta T}$ are the output current of the current source, the pre-emphasis current, respectively, S_TX is the serial CMOS data, and SP, SN, SDP, SDN are the control signal of the pre-emphasis circuit.

Pre-emphasis control circuit first determine the transition edge of the input data valid or not, then drive the control signal (SP, SN, SDP & SDN) into current pre-emphasis circuit and add additional output current. Transition edge checking circuit and its waveform are shown in Fig. 4 (b); it can detect the transition edge of the CMOS logic signal. By using this method, the pre-emphasis circuit can detect the transition edges of signal and enhance transition current density of differential signal.

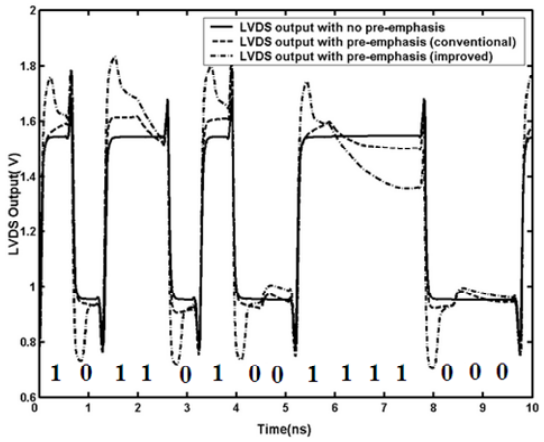

Figure.5 The simulation results of the LVDS output

The simulation results of the differential output signal of the driver are received and shown in Fig.5 by using HSPICE simulator. The drive current of the current source is designed as 5mA. Because the LVDS deriver is designed a 100Ω differential load, the differential signal swing is 500mv and the common voltage of the signal is1.2V. The current in the edge of the differential signal is increased obviously compared with conventional pre-emphasis scheme, which resulting in higher loss compensation. Pre-emphasis comes into effect only when the signal bit makes transition from one state to another.

4 TEST RESULTS OF THE TRANSMITTER

The transmitter is designed by using 0.13μm 1P8M CMOS process, the supply voltage of driver is 3.3V and the supply voltage of PLL is 1.5V. The die micrograph of the transmitter is shown in Fig.6.

The test instrument is DSO91304A by AGILENT TECHNOLOGIES. As shown in Fig.7, the transmission rate of the data is 1.5Gb/s, the swing of LVDS is 450mV, and common-mode voltage of LVDS is 1.2V. Pre-emphasis circuit emphasizes the current density in data transition. In the test system, the RG-58/U coaxial cable loss at 750MHz is 13dB [19], and the total channel loss is approximately 16dB including additional parasitic losses in the path from chip to coaxial cable (probes, bonding wire, package and connectors). The eye diagram of the LVDS with conventional pre-emphasis is shown in Fig.8; and the Fig.9 illustrates the eye diagram of the LVDS with improved pre-emphasis. From the clearly open eye diagrams it can be concluded that the pre-emphasis compensates enough channel loss at 1.5 Gb/s.

In the transmitter, the sampling frequency of the parallel data is 750MHz. The spectrum of the output clock that recovered from the LVDS can be observed with spectrum analyzer, as shown in Fig.10. The total power consumption of the transmitter is 80mW at 1.5Gb/s, among that the power consumption of the driver is 50mW. In Table 1, a comparison of some test results with other published work is given.

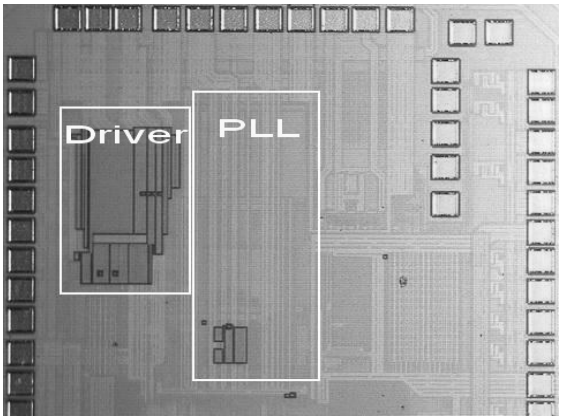

Figure.6 The die micrograph of the transmitter

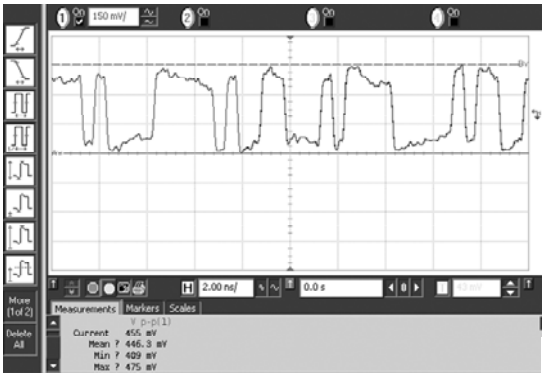

Figure.7 The waveform of the LVDS with improved pre-emphasis at 1.5Gb/s

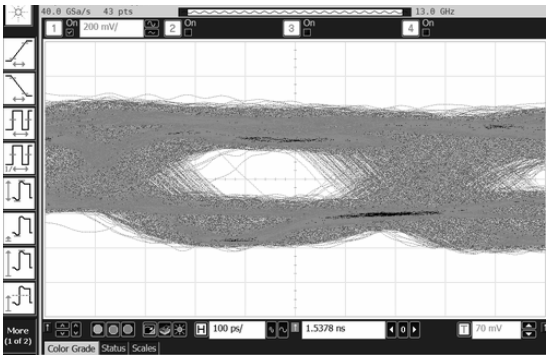

Figure.8 The eye diagram of the LVDS with conventional pre-emphasis at 1.5Gb/s(Horizontal axis = 100ps/div, vertical axis=100mV/div）

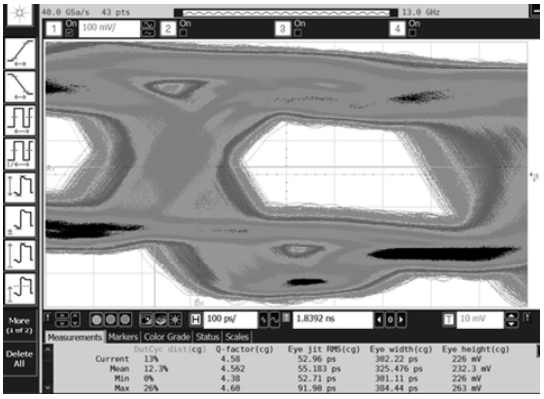

Figure.9 The eye diagram of the LVDS with improved pre-emphasis at 1.5Gb/s（Horizontal axis = 100ps/div, vertical axis=100mV/div）.

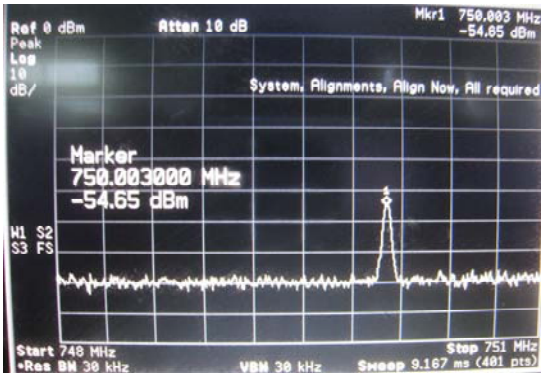

Figure.10 The spectrum of the recovery clock

Table 1 Comparison with other work

	[6]	[20]	This work
Power Supply(V)	1.8	3.3/2.5	3.3/1.5
Power Consumption(mW)	95	240	80
Chip Size (mm^2)	1.33×0.78	4.2×4.2	0.7×0.8
Differential Voltage Swing (mV)	540	---	450
Transmitter data (Gb/s)	1.5	1.25	1.5

5 CONCLUSIONS

An improved low-voltage differential signal transmitter is implemented in 0.13μm 1P8M CMOS process. In the LVDS transmitter, a novel VCO and an improved pre-emphasis circuit are designed to reduce inter-symbol interference (ISI). Test results shows that the transmitter can transmit serial data at a speed from 0.5Gb/s to 1.5Gb/s. It possesses stable common-mode voltage and differential swing voltage. The improved pre-emphasis circuit compensates enough channel loss at 1.5 Gb/s. The total power consumption of the transmitter (driver + PLL) is 80mW at 1.5Gb/s, and the recovery clock from the data also keeps good phase noise performance.

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