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J. Electrical Systems 15-2 (2019): 249-263

A new Trans-Impedance Mode biquad filter employing single DVCCTA

Journal of Electrical Systems

In this study a new topology realizing the biquad filtering functions based on only single DVCCTA as active element is proposed which consists of four grounded passive elements too and canonical in structure as it consists of two grounded capacitors. By applying only the single current input signal at appropriate node, the proposed biquad realizes various types of four voltage filtering responses, simultaneously, each at different node of the circuit. Thus, the proposed filter is behaving as current input voltage output circuit and hence, called trans-impedance-mode (TIM) biquad filter. Besides, it enjoys with reasonable low power consumption and low components sensitivities. Moreover, the center pole frequency (ω_0) can be independent tuned to quality factor (Q_0) through biasing current control of active element. Moreover, the PSPICE simulated results in 0.18˜m CMOS technology are also shown in the study which can verify the validity of the circuit.

Keywords: Trans-impedance, DVCCTA, Filter, Biquad.

Article history: Received 7 January 2019, Accepted 10 May 2019

1. Introduction

With the advancements in electronics over the period of time, numerous number of sophisticated basic current-mode (CM) active blocks have been reported and have gained considerable research attention for implementation of analog circuits used for the number of analog signal processing applications [1]. Among them, current conveyors and their various improved variants such as DVCCII, DDCCII, FDCCII and DXCCII etc., were few which achieved significant popularity and hence, discussed broadly in the existing literature work [2-8]. However, these elements are not capable to offer the electronic tuning feature to the implemented circuits which is essentially required to compensate the possible deviations occurred in circuit parameters due to the presence of parasitic, temperature variations, process tolerance and aging in the components etc., [9]. Therefore, later on, more number of active elements which offering the feature of electronic tunability, were also reported in the literature. Examples of these elements are OTA, CCCII, CCTA, CDTA, CFTA, CCCCTA, CCCDTA, DDCCTA, VDTA, DVCCTA, etc., [10-22]. The reviews of these current-mode elements along with detailed properties are well discussed and summarized in the review paper [23].

The DVCCTA is a newly incepted active element introduced by A. Jantakun [19] and after its inception, it has received considerable attention as suitable CM active block for designing of number of analog signal processing building blocks such as voltage mode (VM) filter circuits [24-25], CM filter circuit [24], TAM filter circuit [20, 26], oscillators [27], Chua's oscillator [28], floating simulator [29], versatile modulator [30], memristor emulator [31]etc.

Unfortunately, the TIM type filter circuit using DVCCTA is being missed in the available literature. The TIM filter circuits are found useful in many applications such as conversion of the voltage input signal to the current output signal or current input signal to the voltage output signal directly. Thus, it reduces the requirement of any extra hardware which is required for the conversion of output signal further from voltage to current or from

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current to voltage after the filtering action. These circuits are also found in ADC/ DAC circuits, receiver baseband blocks (RBBB) and modern radio receiver systems, etc. [18].

Although, quite a few filter configurations of TIM type consisting of current-mode elements except DVCCTA are reported in the literature [18, 32-45]. Among them, the biquads presented in Refs. [32-37, 39-43,45] are single input multiple output (SIMO) types which realizes simultaneous filtering responses by using a single current input whereas biquad filter presented in Refs. [18, 38, 44] realize one output at a time after the selection of multiple inputs. However multiple inputs may further requires extra hardware.

Moreover, each of the TIM filters presented in Refs. [32-37, 39-43] realize at most three filtering responses simultaneously by using of only single current input signal. Moreover, these circuits comprise of at least three or more active elements (six OP-AMPs and OTAs [40], five OP-AMPs and OTAs [32], four CCIIs [43], three DVCFAs [37], three CDBAs [33, 42] three DVCCs [41], three CCCCTAs [36,39] and additionally excessive number of passive elements (five [32, 37, 42], six [43], seven [32]) for the filtering implementation. However, most of the TIM circuits are lacking with the feature of electronic tunability [31, 32, 37, 40-43]. Besides, few of the circuits [32, 37, 42- 43] employ one or more passive elements as floating which is not suitable for IC integration point of view. Moreover, none of the aforesaid circuits except [45] has been realized using single active element. However, none of the filter output in Ref. [45] are obtained at low impedence level. In addition, in Ref [45] no discuusion has been made on layout design and area calculation of the filter.

So after reviewing the survey of trans-impedance filter, a new circuit based on single DVCCTA is proposed which can realize four filtering functions in the trans-impedance mode, without any matching conditions. These filtering functions are LP, HP, BP, and BR. Furthermore, each of TIM realization associated with the proposed circuit uses only single input signal. The proposed circuit is designed with single active element along with four grounded passive elements (two capacitors and two resistors), which is helpful in the simpler IC fabrication point of view.

Apart from this, the circuit exhibit some desirable features such as orthogonal electronic tunability between filter parameters such as ω_0 and Q_0, low active and passive element sensitivities, low power consumption, and no requirement of scaled and /or inverted type input. In addition, the functionality and validity of the circuit is also proven by PSPICE simulation results and mathematical analysis.

2. Notation :

Indexes

g_m	Transconductance
ω_0	Pole Frequency
Q_0	Quality Factor
BW	Band Width
V_{LP}	Low Pass Voltage Output
V_{BP}	Band Pass Voltage Output
V_{HP}	High Pass Voltage Output
V_{BR}	Band Reject Voltage Output

3. DVCCTA description:

The symbolic diagram representation of DVCCTA is depicted in Figure 1. As depicted in Figure 1, it contains two high impedance input terminals (Y_1, Y_2) suitable for voltage sensing and one low input impedance terminal (X) suitable for current sensing. In addition, it also consists of two or more high impedance trans-conductance outputs (O+, O-) and one

high impedance auxiliary output terminal (Z) mostly loaded with impedance. Through the trans-conductance parameter (g_m), the trans-conductance stage transforms the voltage across Z into current at its high impedance output terminals (O+ and O-) as I_{O+} and I_{O-}. The trans-conductance parameter (g_m) of DVCCTA can be electronically adjustable via external biasing current I_B. This property makes DVCCTA suitable for the synthesis of electronically tunable analog circuits. Furthermore, the current through low impedance X terminal is conveyed to the high impedance Z terminal.

The mathematical relations of various ports associated with DVCCTA can be characterized by matrix Eqn (1) [27]. The CMOS realization of DVCCTA is also depicted in Figure 2 which consists of only twenty six transistors including both NMOS and PMOS where the NMOS transistors M_1 to M_4, M_{10} to M_{13} and PMOS transistors M_{16} to M_{19} form a DVCCII, whereas NMOS transistors M_5 to M_9, M_{14} to M_{15} and PMOS transistors M_{20} to M_{26} form the desired trans-conductance stage.

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_{O\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{bmatrix} \quad (1)$$

The value of trans-conductance parameter (g_m) dependent on I_B, can be determined from the expression defined in Eqn (2) [30]. Here, C_{ox} is the value of capacitance per unit area of gate oxide and μ_n is effective electron mobility for each nMOS transistors in the circuit of Figure 2. Besides, the $(W/L)_{M14\text{-}M15}$ stand for aspect ratio of M_{14} and M_{15} transistors in the same circuit (Figure 2).

Thereafter, the layout of MOS implemented DVCCTA in Figure 2 based on λ based design rule is also designed and shown in Figure 3. In designing the layout W/L ratio are determined and used as given in Table 1. In addition, the validity of layout has also been evaluated through the processes of error checking and nets mismatching between schematic and layout by the use of designated tools i.e. DRC and LVS.

$$g_m = \sqrt{\beta_n I_B}$$

where

$$\beta_n = \mu_n C_{ox} \left(\frac{W}{L} \right) \quad (2)$$

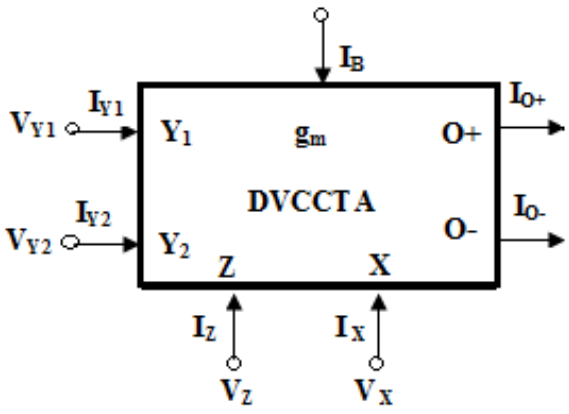


Figure 1: Block diagram representation of DVCCTA

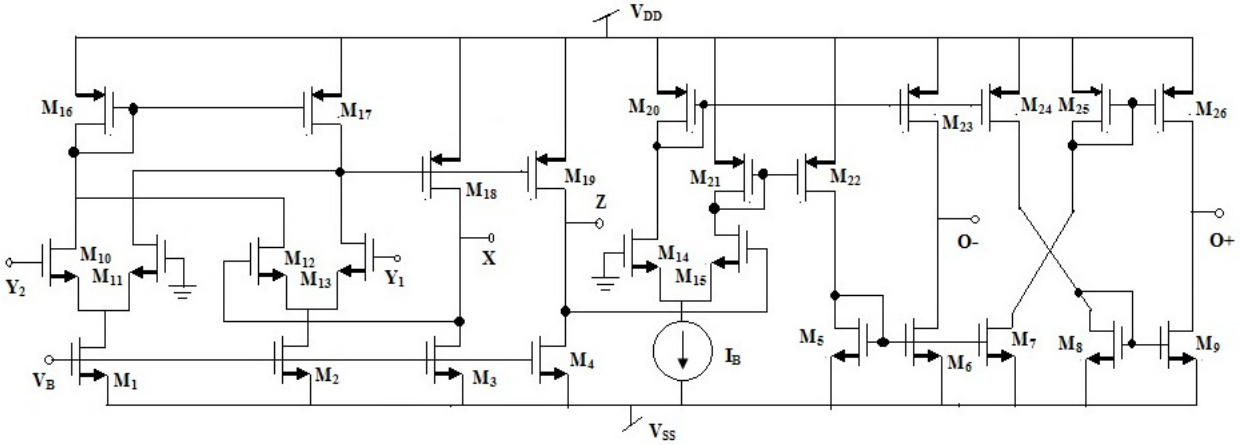


Figure 2: CMOS model representation of DVCCTA

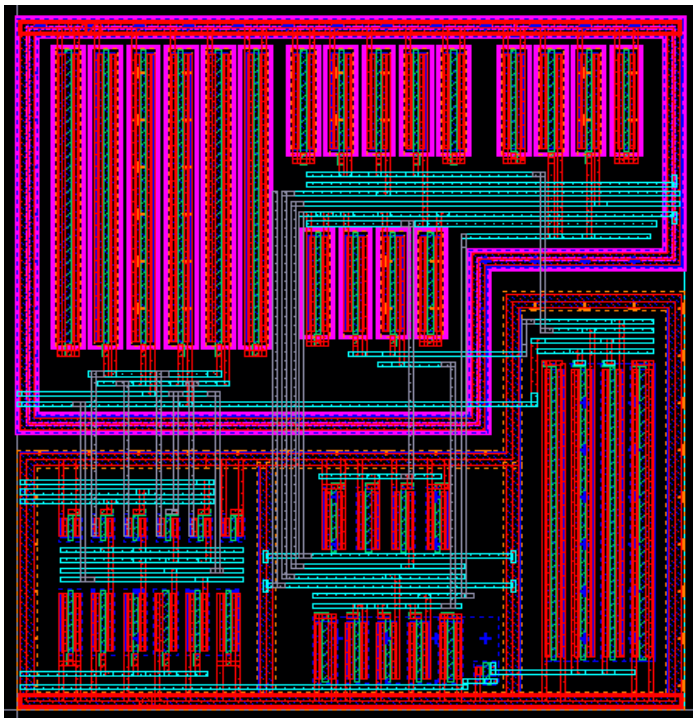


Figure 3: Layout design of DVCCTA of Figure 2

Table 1. W/L of each transistors of DVCCTA in Figure 2

Transistors	W(µm)/L(µm)
M1-M9 (NMOS)	4.32 µm/0.36 µm
M10-M13 (NMOS)	1.44 µm/0.36 µm
M14-M15 (NMOS)	21.6 µm/0.36 µm
M16-M19 (PMOS)	21.6 µm/0.36 µm
M20-M26 (PMOS)	7.2 µm/0.36 µm

Furthermore, the performance of the CMOS based realization of DVCCTA is also measured by simulating it in 0.18µm model parameters from TSMC. The DVCCTA is biased with supply voltage supply of V_{DD} = -V_{SS} = 1.4V and V_B = -0.5 V. Each of MOS transistor dimensions was used as given in Table 1. The area of MOS implemented DVCCTA layout without pads is found to be 2.62 nm^2 which is an optimum value and suitable for monolithic integration point of view. Figure 4 depicts the variation in trans-

conductance (g_m) parameter of DVCCTA for different values of external biasing current (I_B) while allowing the current (I_B) to be vary from 0 to 2000µA which conclude that the simulation result showing variation of g_m relative to the current I_B is as per Eq. (2) and confirms a wide range electronic tunability of the DVCCTA. Next, the DC current transfer characteristic in which I_Z versus I_X plots for different values of V_B as -0.5V, -0.6V, -0.7V and -0.8V is depicted in Figure 5. The results obtained in Figure 5 confirm that the wide range of linearity exists between I_Z and I_X of the DVCCTA. Subsequently, in order to determine the -3dB bandwidth of DVCCTA, the frequency responses of current gain (I_Z/I_X), voltage gains (V_X/V_{Y1}, V_X/V_{Y2}), and trans-conductance gain (I_{O+}/V_Z) of DVCCTA at I_B = 130 µA were obtained and also shown in Figure 6. From the frequency responses in Figure 6, the -3dB bandwidth of I_Z/I_X, V_X/V_{Y1}, V_X/V_{Y2}, and I_{O+}/V_Z were determined as 1.74 GHz, 1.35 GHz, 1.33 GHz, and 722 MHz, respectively, which shows the wide bandwidth of various gain stages of DVCCTA.

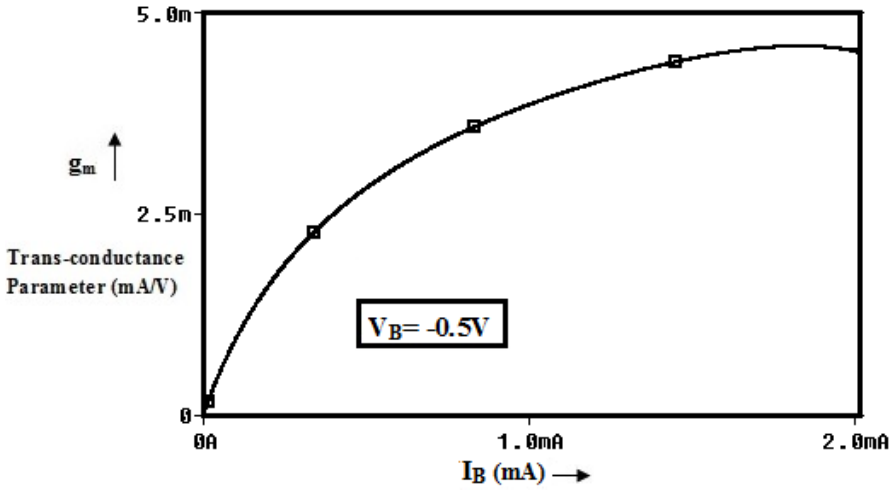


Figure 4: Variation in trans-conductance parameter (g_m) with respect to I_B for the DVCCTA in Figure 2

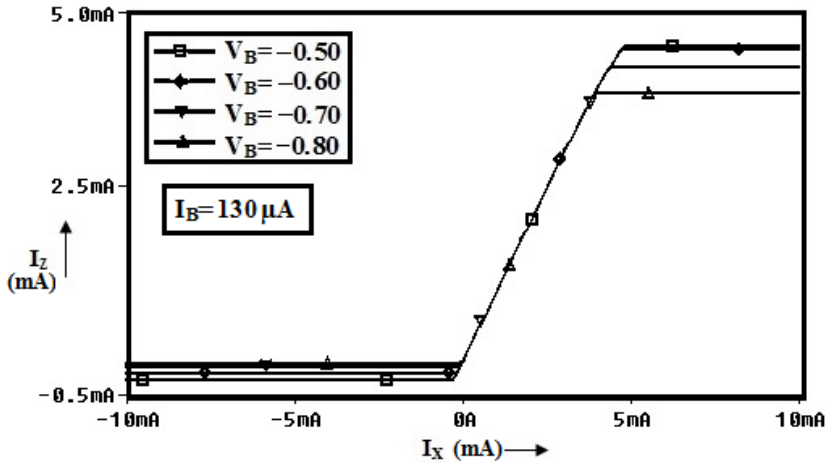


Figure 5: DC current transfer characteristic of I_Z versus I_X for the DVCCTA in Figure 2

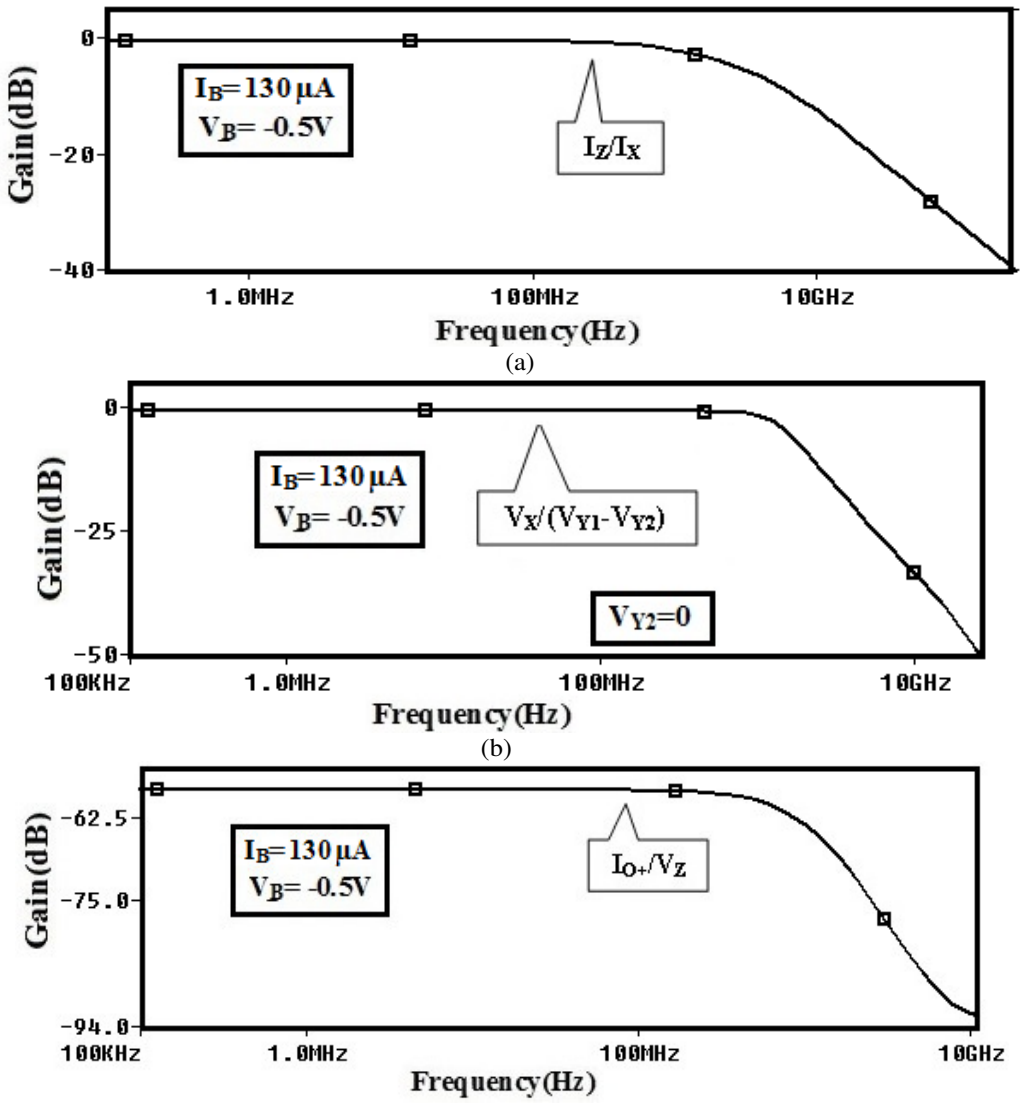


Figure 6: Frequency response of DVCCTA of Figure. 2 (a) current gain (I_Z/I_X) (b) voltage gain ($V_X/(V_{Y1}-V_{Y2})$) (c) trans-conductance gain (I_{O+}/V_Z)

4. Description and analysis of proposed filter:

The proposed trans-impedance mode (TIM) biquad filter employing single DVCCTA is shown in Figure 7 that also consists of two capacitors (C_1 and C_2) as well as two resistors (R_1 and R_2). Each of the passive elements in the circuit is grounded. Apart from this, the circuit uses a single current input signal as I_{in} and the corresponding voltage outputs have been taken as V_{LP}, V_{BP}, V_{HP}, and V_{BR} across four different nodes, respectively. Thus, the trans-impedance mode filter is a single input four output (SIFO) type topology. The mathematical analysis of Figure 7, yields the following transfer functions:

$$\frac{V_{LP}}{I_{in}} = \frac{g_m R_1 / R_2 C_1 C_2}{D(s)} \tag{3}$$

$$\frac{V_{HP}}{I_{in}} = \frac{s^2 R_1}{D(s)} \tag{4}$$

$$\frac{V_{BP}}{I_{in}} = \frac{sR_1 / R_2 C_2}{D(s)} \tag{5}$$

$$\frac{V_{BR}}{I_{in}} = \frac{\left(s^2 + g_m / C_1C_2R_2\right)R_1}{D(s)} \tag{6}$$

where,
$$D(s) = \left[s^2 + \frac{sg_mR_1}{C_2R_2} + \frac{g_m}{C_1C_2R_2} \right] \tag{7}$$

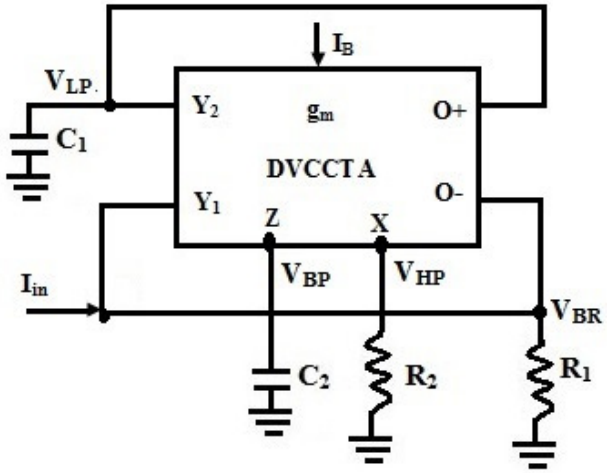


Figure 7. Block diagram of proposed TIM biquad filter

The equations (Eqs. (3) to (7)), can conclude that circuit in Figure 7 has a capability of realizing four trans-impedance mode filtering responses, simultaneously. These responses are LP, HP, BP, and BR at voltage nodes V_{LP}, V_{HP}, V_{BP} and V_{BR}, respectively.

From characteristic equation of the proposed filter (Eq.(7)), the following filtering parameters can be expressed as:

$$\omega_0 = \sqrt{\frac{g_m}{C_1C_2R_2}} = \sqrt{\frac{(\beta_n I_B)^{1/2}}{C_1C_2R_2}} \tag{8}$$

$$Q_0 = \frac{1}{R_1}\sqrt{\frac{C_2R_2}{C_1g_m}} = \frac{1}{R_1}\sqrt{\frac{C_2R_2}{C_1(\beta_n I_B)^{1/2}}} \tag{9}$$

$$BW = \frac{g_mR_1}{C_2R_2} = \frac{R_1(\beta_n I_B)^{1/2}}{C_2R_2} \tag{10}$$

where ω_0, and Q_0 are called centre frequency and quality factor, respectively, while BW is called bandwidth of the filter. It can also be deduced from Eq. (8) that, the ω_0 can be varied independent to Q_0 by electronic means (changing the value of g_m) and maintaining the condition as: $R_1 = R_2 = 1/g_m$.

Similarly, the Q_0 can be varied independently from ω_0 (refer Eq.(9)) too by varying the resistor R_1 only, where grounded resistor can be realized as electronic tunable, simply by using two NMOS transistors [45].

5. Consideration of non idealities and sensitivities calculation:

The mathematical analysis and study of the proposed filter done in previous section is based on the assumption of ideal form of DVCCTA as described in Eqn (1). Now the various non-idealities associated with CMOS DVCCTA due to the mismatching of the transistors is considered in this section which may influence the performance of proposed filter. By taking all nonidealities associated with CMOS DVCCTA into consideration, the properties of ideal form of DVCCTA described in Eqn (1) can be further modified as:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_{o\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & \beta_1 & -\beta_2 & 0 \\ \alpha & 0 & 0 & 0 \\ 0 & 0 & 0 & \gamma g_m \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{bmatrix} \tag{11}$$

In Eqn. (11), β_1 and β_2 are the voltage transfer gains from Y_1 to X and Y_2 to X, respectively. The current transfer gain α stand for the current pathway from X to Z terminal. Similarly, γ is trans-conductance imprecision factor between Z to O+ as well as Z to O- terminals, respectively. The value of α, β_1, β_2, and γ associated with CMOS DVCCTA in Figure 2 are also measured using simulation results shown in Figure 6 and found to be 0.991, 0.99, 0.987, and 0.985, respectively which is very closed to the unity.

If we further analyze the proposed filter by using Eqn (11), the transfer functions of each filtering responses can be derived as:

$$\frac{V'_{LP}}{I_{in}} = \frac{\alpha\beta_1\gamma g_m R_1 \big/ R_2 C_1 C_2}{D'(s)} \tag{12}$$

$$\frac{V'_{HP}}{I_{in}} = \frac{s^2\beta_1 R_1}{D'(s)} \tag{13}$$

$$\frac{V'_{BP}}{I_{in}} = \frac{s\alpha\beta_1 R_1 \big/ R_2 C_2}{D'(s)} \tag{14}$$

$$\frac{V'_{BR}}{I_{in}} = \frac{\left(s^2 + \alpha\beta_2\gamma g_m \big/ C_1 C_2 R_2\right) R_1}{D'(s)} \tag{15}$$

where
$$D'(s) = \left[s^2 + \frac{s\alpha\beta_1\gamma g_m R_1}{C_2 R_2} + \frac{\alpha\beta_2\gamma g_m}{C_1 C_2 R_2} \right] \tag{16}$$

and hence, the expressions for ω_0, Q_0, and BW of the filter as obviously modified as:

$$\omega'_0 = \sqrt{\frac{\alpha\beta_2\gamma g_m}{C_1 C_2 R_2}} \tag{17}$$

$$Q'_0 = \frac{1}{\beta_1 R_1}\sqrt{\frac{\beta_2 C_2 R_2}{\alpha\gamma C_1 g_m}} \tag{18}$$

$$BW' = \frac{\alpha\beta_1\gamma g_m R_1}{C_2 R_2} \tag{19}$$

From Eqs. (12) - (19), it can be clearly observed that all above filter parameters including pass-band gains may slightly deviate from their actual values due to the presence of these non-idealities. However, the slight changes occurring due to finite non-idealities associated with DVCCTA can be reduced and hence, negligible because non-ideal gains (α, β_1, β_2, and γ) can be obtained approaching to unity at the operating frequency. Apart from this, the active and passive sensitivity of ω_0 and Q_0 are also calculated and mentioned in Eqs. (20) - (21). As per the calculation mentioned in Eqs. (20)- (21), all the component sensitivities of

circuit parameters are showed low (maximum magnitude is one) which ensuring good sensitivity performance.

$$S_{\alpha,\beta_2,\gamma,g_m}^{\omega_0} = \frac{1}{2}, S_{R_2,C_1,C_2}^{\omega_0} = -\frac{1}{2}, S_{R_1,\beta_1}^{\omega_0} = 0 \tag{20}$$

$$S_{\alpha,\gamma,g_m,C_1}^{\omega_0} = -\frac{1}{2}, S_{\beta_2,C_2,R_2}^{\omega_0} = \frac{1}{2}, S_{\beta_1,R_1}^{\omega_0} - 1 \tag{21}$$

6. Influences of parasitic elements:

Now the effects on the performance of the proposed TIM circuit of Figure 7 due to the presence of ports parasitic associated with DVCCTA are studied. Taking ports parasitic into consideration, the circuit shown in Figure 7 can be transformed to Figure 8. In Figure 8, the parasitic appears as R_X at port X, $C_{P1}||R_{P1}$ combinedly at ports Y_2 & O+, $C_{P2}||R_{P2}$ at port Z, and $C_{P3}||$ R_{P3} combinedly at ports Y_1 & O-. Since the practical value of parasitic resistance R_X appearing at terminal X connected in series with external resistance R_2 is low and within the range of few ohms. Therefore, the effect of R_X can be neglected by choosing a comparatively large value of R_2 as compared to R_X in the design. Further, to convenient, the parasitic resistors at high impedance ports as well as the external resistors are represented in term of the conductance such as: $R_{Pi} = 1/G_{Pi}$ (i = 1 to 3), $R_1 = 1/G_1$, and $R_2 = 1/G_2$, respectively. As the parasitic capacitances C_{Pi} are found generally in the fraction of pico farads range or even lesser depending upon MOS technology used, so external capacitances C_1 and C_2 employed in the design are expected to be much greater than parasitic ones to minimize the effects of parasitic capacitances and therefore, min (C_1, C_2) >> (C_{P1}, C_{P2}, C_{P3}) can be assumed. Similarly, the value of G_{Pi} (i =1, 2, 3) are less than 10 micro mho as these appear across high impedance port. So, the external conductances (G_1, G_2) can also be chosen much greater than the parasitic conductances G_{Pi} (i = 1, 2, 3). Therefore, min (G_1, G_2) >> (G_{P1}, G_{P2}, G_{P3}).

To know the effects of all parasitic resistances and capacitances on circuit performance, the described circuit including parasitic as shown in Figure 8 is analysed again. By considering the above assumptions, the circuit analysis of Figure 8 leads to the following TIM transfer functions:

$$\frac{V''_{LP}}{I_{in}} = \frac{g_m \dfrac{G_2}{G_1 C_1 C_2}}{\left(1+\dfrac{G_{P1}}{sC_1}\right)\left(1+\dfrac{G_{P2}}{sC_2}\right)D''(s)} \tag{22}$$

$$\frac{V''_{BP}(s)}{I_{in}} = \frac{s\dfrac{G_2}{G_1 C_2}}{\left(1+\dfrac{G_{P2}}{sC_2}\right)D''(s)} \tag{23}$$

$$\frac{V''_{HP}(s)}{I_{in}} = \frac{s^2}{G_1 D''(s)} \tag{24}$$

$$\frac{V''_{BR}(s)}{I_{in}} = \frac{\left[s^2\left(1+\dfrac{sC_{P3}}{G_1}\right)+\dfrac{g_m G_2}{C_1 C_2}\right]}{G_1\left(1+\dfrac{sC_{P3}}{G_1}\right)D''(s)} \tag{25}$$

where, $$D''(s) = \left[s^2\left(1+\frac{sC_{P3}}{G_1}\right)+\frac{sg_mG_2}{C_2G_1}+\frac{g_mG_2}{C_1C_2}\right] \quad (26)$$

Moreover, the expressions of filter parameters are also modified to:

$$\omega_0'' = \omega_0\sqrt{\frac{1}{\left(1+\frac{sC_{P3}}{G_1}\right)}} \quad (27)$$

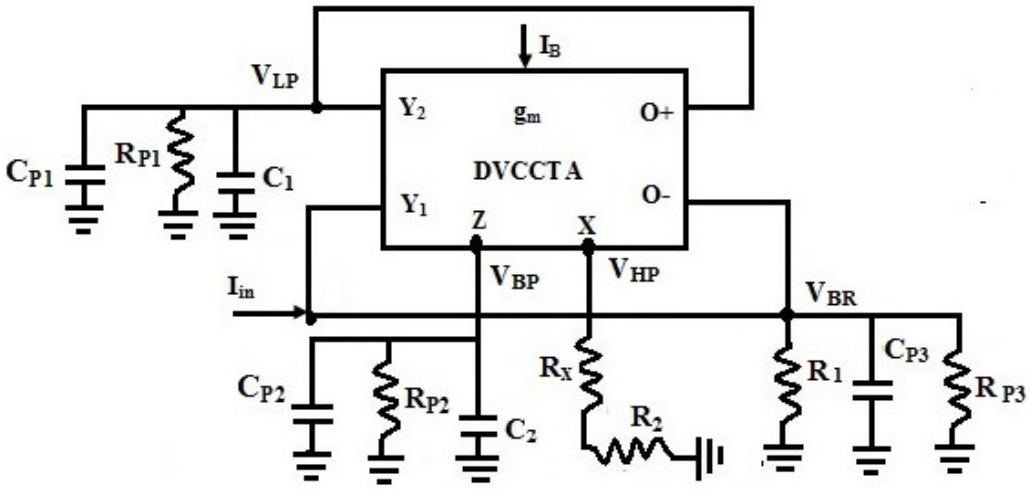


Figure 8. TIM biquad including the ports parasitic

$$Q_0'' = Q_0\sqrt{\left(1+\frac{sC_{P3}}{G_1}\right)} \quad (28)$$

It can be observed from Eqs. (22) – (28) that while considering the presence of parasitic elements, additional first order pole(s) or zero(s) are introduced in the transfer functions and filter parameters which may cause to change the pass band gain, ω_0 and Q_0 , undesirably. However, these undesirable changes can be reduced or minimized if the frequency of operation of the circuit while designing is chosen as follows:

$$\max\left(\frac{G_{P2}}{C_2},\frac{G_{P1}}{C_1}\right) << \omega << \min\left(\frac{G_1}{C_{P3}}\right) \quad (29)$$

7. Simulation results:

Now in this section, the validity of the proposed circuit shown in Figure 7, has been verified using 0.18μm CMOS technology from TSMC in PSPICE software. The circuit was biased with power supply voltages of V_{DD}= -V_{SS} = 1.4 V and V_B= -0.5V. The active and passive components values were determined as I_B = 130μA (g_m≈1175 μA/V), C_1 = C_2 = 10 pF, and R_1 = 1.3 KΩ, R_2 = 2 KΩ to design the filter having the pole frequency of 12.4 MHz. The λ-based layout design of described filter in Figure 7 is also developed and shown in Figure 9. The corresponding layout area and power consumption are found to be 13.7 nm^2 and 4.31 mW, respectively. In addition, the theoretical as well as PSPICE simulated gain responses of all four filtering functions are shown in Figure 10. From the simulated results, the f_0 ($\omega_0/2\pi$) is measured as 12.3 MHz which is nearly the same as the theoretical value or ideal value of 12.4MHz. It is also noted from the same simulated results that the behaviour of the proposed circuit agrees with theoretical presumptions very well.

Thereafter, the circuit of Figure 7 is gone for the further simulation to show its tuning feature of circuit parameters. The simulation results of BP responses showing tuning feature

are shown in Figure 11. Figure 11(a) shows the electronic tuning capability of f_0 ($\omega_0/2\pi$) independent of Q_0 in which different values of f_0 as 4.25MHz, 6.3MHz, 10.4MHz, and 18.3MHz, at constant $Q_0 = 1$ are obtained by maintaining the condition of $R_1 = R_2 = 1/g_m$ (for example, g_m =236 µA/V (I_B=20µA), 342 µA/V (I_B=30µA), 627.5 µA/V (I_B=60µA), 1045 µA/V (I_B=120µA) and $R_1 = R_2$= 4.23 KΩ, 2.92 KΩ, 1.59 Ω, 920 Ω, respectively). Besides, Figure 11(b) shows the tuning feature of Q_0 independent of ω_0 in which different values of Q_0 are obtained as 12.9, 6.4, 2.7, 1.01, and 0.44 by varying R_1 as 100 Ω, 200 Ω, 500 Ω, 1.3 KΩ, and 3.0 KΩ, which can be further varied electronically by implementing it by MOSFET realization.

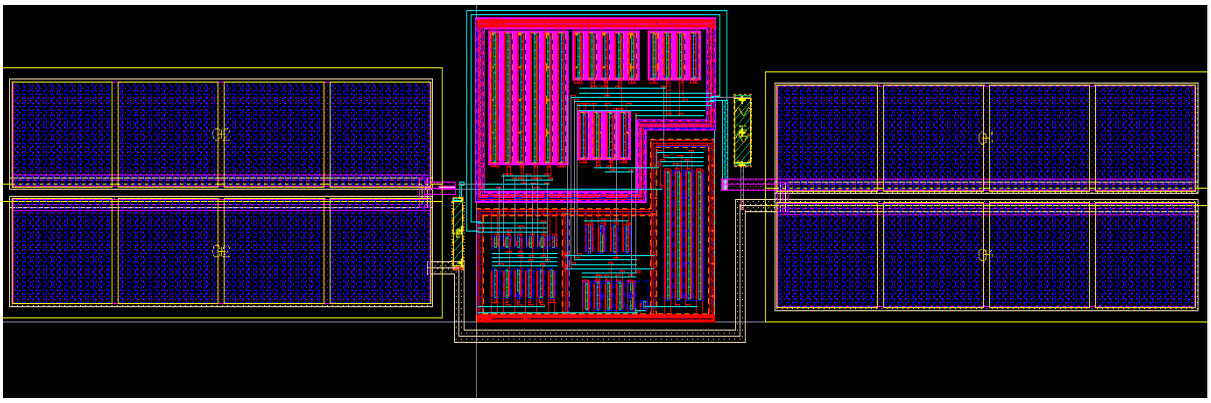


Figure 9: Layout design of proposed biquad filter

Further, the circuit was also tested to check its transient behaviour with respect to applied time domain sinusoidal current input signal of 5MHz frequency and 100 µA (p-p) amplitude. The TIM LP filter is selected for the demonstration purpose and the corresponding TIM LP filtering output is depicted in Figure 12 which shows that the circuit behaviour performs well for large signal input.

Next, the proposed TIM filter of Figure 7 was again simulated to examine for THDs produce by the circuit. In this study, sinusoidal input signals of 100µA (p-p) amplitude and varying frequency in the range of 500 KHz to 13 MHz are applied and the LP output of circuit is selected for the presentation of THD analysis. The THD results at amplitude of 100µA (p-p) are shown in Figure 13 which conclude that the THD figures are within moderate and acceptable range of 2.8% [21].

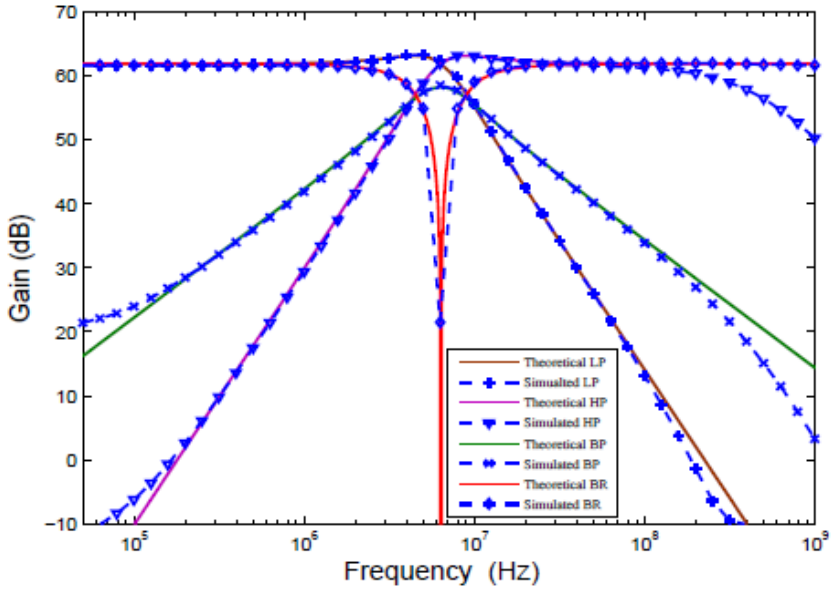


Figure 10. Simulated and Theoretical gain responses of BP, LP, HP, and BR TIM Filter

Furthermore, Monte-Carlo simulation was also carried out to evaluate the impact of capacitive deviations and mismatching on filter's performance. In this study, the BP output of TIM filter is selected for the presentation of Monte-Carlo simulation results. The simulation was performed by taking 10% Gaussian deviation in $C_1 = C_2 = 10$ pF. After the 500 concurrently runs, the corresponding simulation results are depict in Figure 14. In Figure 14 (a), the variation in gain response of BP output with respect to deviation in capacitors value are shown whereas Figure 14 (b) shows the statistical results in the form of histograms of pole frequency which measure the simulated mean, standard deviation and median, as 13.37 MHz, 545.1 KHz, and 13.35 MHz, respectively. It is implied from the results shown in Figure 14 that the proposed filter is reasonably less sensitive toward the capacitive tolerances around the simulated ω_0 of 12.3 MHz and thus, offers reasonable passive sensitivity characteristics.

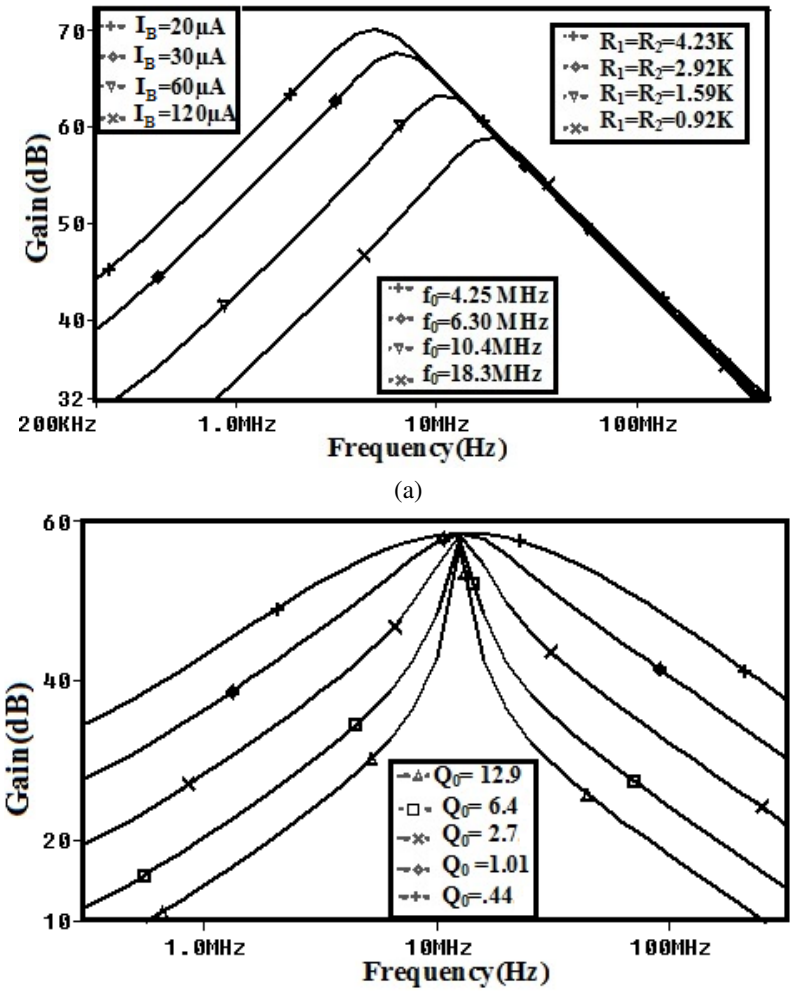


Figure 11. Tunability results showing (a) f_0 independent of Q_0 (b) Q_0 independent of f_0 for TIM BP response

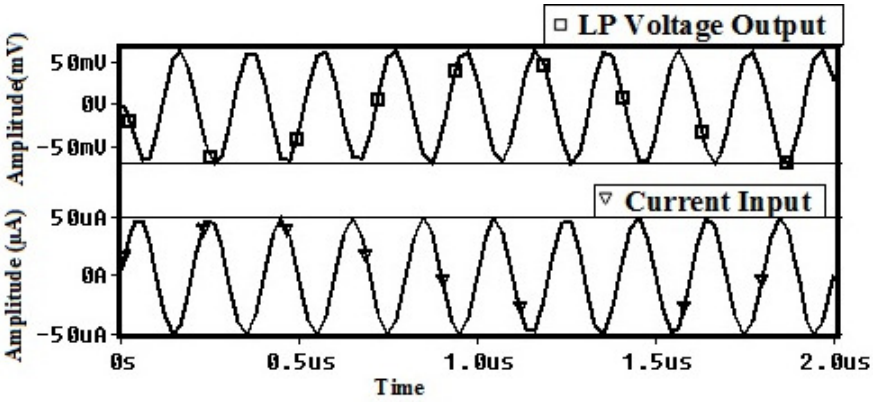


Figure 12. Transient output of TIM LP response of the filter

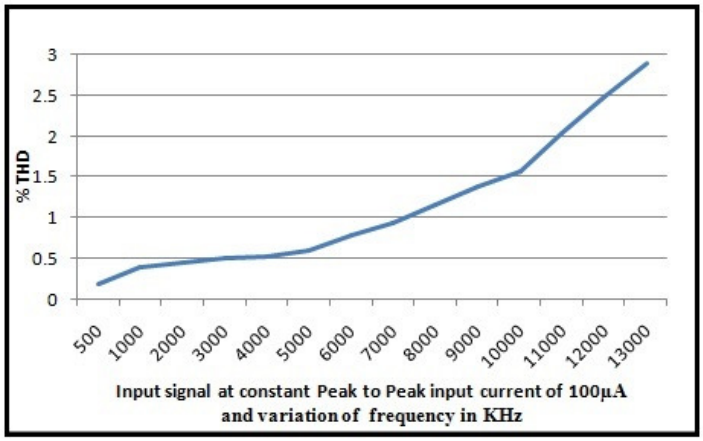
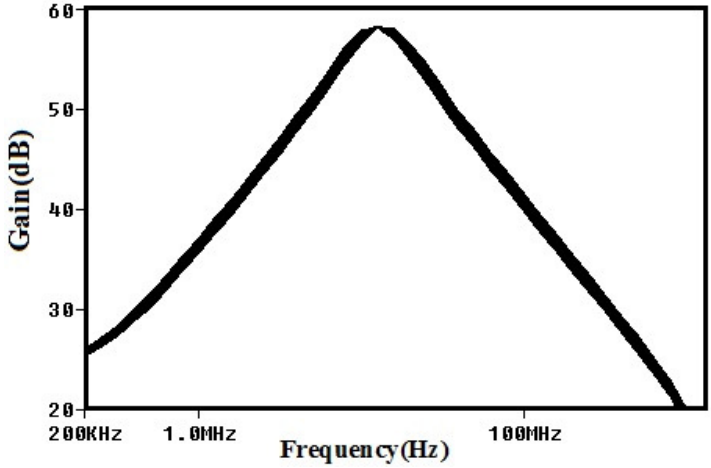


Figure 13. % THD analysis for LP response of the filter circuit

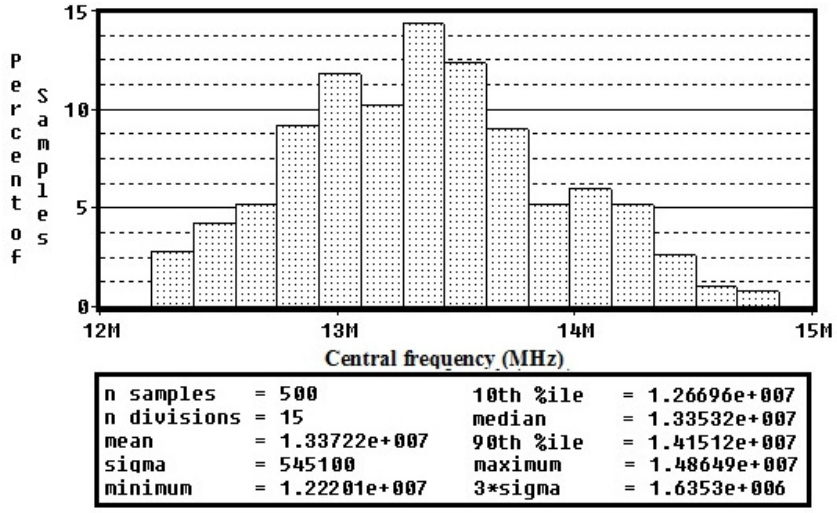


(a)

Conclusion:

In this paper, a noble TIM biquad filter has been proposed and studied in detail. The topology is based on only using single DVCCTA as active element which consists of four grounded passive elements too and also canonical in structure as it consists of two grounded capacitors. In addition, the proposed topology realizes LP, HP, BP and BR responses, simultaneously, each at different node of the circuit. The functionality of filter was also discussed with respect to different mathematical analysis such as parasitic analysis, non ideal and sensitivity analysis etc. Moreover, the circuit exhibit some desirable features such as low active and passive sensitivities, independent electronic tunability of filter parameters, canonical structure, no requirement of scaled and /or inverted type input(s), no matching condition(s), and consuming less power. In spite of this, the PSPICE

simulation results in term of frequency responses, transient analysis, THD analysis, etc., for the proposed filter circuits have been included and studied which agree quite satisfactory with theoretical one as expected. Apart from this, the layout of the circuit has also been designed and the corresponding layout area is found to be 13.7 nm^2.



(b)

Figure 14. Monte Carlo analysis of BP output (a) gain response (b) histogram response of pole frequency

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