R. Uthirasamy [1,*], V. Kumar Chinnaiyan[2], J.Karpagam[3], V. J Vijayalakshmi[4]

J. Electrical Systems 13-3 (2017): 558-567

Regular paper

Design and Analysis of Stepped DC Link Hybrid Converter for Solar PV Systems

A structure of single phase DC Link Multilevel H-Bridge Inverter (DCLMLHBI) is proposed for symmetrical Photo Voltaic (PV) systems. Voltage stress across the inverter switches, Power Spectral Density (PSD), voltage and current harmonics are reduced in the proposed configuration. Compared with conventional 13-level Cascaded Multilevel Inverter (CMLI) configuration, the proposed system configuration is structured with less number of series connected power switches and gate drive circuits. None of the passive components are utilized in the proposed inverter configuration, which highlight the significance of the proposed system. The performance parameters are investigated through Phase Opposition Pulse Width Modulation (POD-PWM) switching scheme and its results are validated with computer simulation and prototype hardware models.

Keywords: Stepped DC link module; Space vector modulation; Total harmonic distortion; power spectral density.

Article history: Received 20 November 2016, Accepted 9 June 2017

1. Introduction

Different configurations of power converters are developed to interface the renewable resources for lower, medium and high power applications [1], [2], [3], [4], [5]. Power electronic converters have the accountability to achieve these tasks with high efficiency. Multilevel Inverter (MLI) topologies generate output voltages with lower distortion. MLI is not only used for achieving reduced harmonic content but also facilitates the use of renewable energy sources such as PV, wind and fuel cells [6], [7], [8], [9], [10]. The three different topologies of MLI are Diode Clamped Multilevel Inverter (DCMLI), Flying Capacitor Multilevel Inverter (FCMLI) and Cascaded Multilevel Inverter (CMLI).Voltage imbalance is a major problem in both DCMLI and FCMLI configurations. CMLI topology is introduced to overcome the limitations of DCMLI and FCMLI. The most important practical challenges in CMLI topology are more power switch and its gate drive circuit requirements. To overcome the existing challenges, modified inverter system is proposed [11], [12], [13], [14]. To obtain better quality of power (with reduced harmonic content), Sinusoidal Pulse Width Modulation (SPWM) and SVPWM switching strategies are developed respectively for single and three-phase DC link switches of the proposed systems [15], [16], [17], [19], [20], [21], [22]. The equivalent circuit of PV systems is integrated with solar panels and charge controllers. Detailed analysis of PV systems is already

* Corresponding author: [1]Dr.R.Uthirasamy, Associate Professor, Department of Electrical and Electronics Engineering, KPR Institute of Engineering and Technology, Coimbatore 641 407, India, E-mail: rusamy83@gmail.com

[2] Dr.V.Kumar Chinnaiyan, Prof & Head, Department of Electrical and Electronics Engineering, KPR Institute of Engineering and Technology, Coimbatore 641 407, India

[3] Dr.J.Karpagam, Professor, Department of Electronics and Communication Engineering, KPR Institute of Engineering and Technology, Coimbatore 641 407, India

[4]Prof.V.J.Vijayalakshmi, Asst Prof(Sr.G), Department of Electrical and Electronics Engineering, KPR Institute of Engineering and Technology, Coimbatore 641 407, India

discussed in existing literatures. The motivation of the proposed work is to enhance 13-level DCLMLHBI for efficient utilization of solar power. Also, the intention is to reduce the harmonic content and filter components, through the implementation of SPWM for single inverter systems. This paper is organized into six sections. Introduction and motivation of the proposed configuration are addressed in section 1. Section 2 described the structure of single 13-level DCLMLHBI for PV systems. Modulation schemes are addressed in section 3. Hardware model of 13-level DCLMLHBI systems is reviewed in section 4. Results and analysis are presented in Section 5 and Section 6 concludes the paper.

2. Structure of 13-Level DCLMLHBI Topology for single Systems

Output power of the solar panels are effectively utilized by the proposed high power DCLMLHBI configurations. For single phase DCLMLHBI system, symmetrical PV panel is operated for 54 V each, and hence the DCLMLHBI system generates the maximum output voltage of 325 V through the SPWM switching of DC link switches and H-bridge inverter. The equivalent structure of single-phase 13-level PV system fed DCLMLHBI is shown in Fig. 1.

Output voltage levels of the proposed DCLMLHBI system is derived using equation (1)

$$N_{level} = 2Q + 1 \tag{1}$$

Number of controlled switches utilized in the single phase 13-level proposed DCLMLHBI is written as

$$N_{switch} = (2Q + 4p) \tag{2}$$

where, p is the number of load end H-Bridges, Q is the number of PV panels.

Some of the DC link switches of 13-level DCLMLHBI are bidirectional and others are unidirectional. For a thirteen level system, each sub-multilevel stage consists of three DC voltage sources and five switches, out of which one is a bidirectional switch. S_{21}, S'_{21}, S''_{21}, S_{23}, S'_{23}, S''_{23} are the bidirectional switches and consists of two IGBT's with the common emitter topology. The proposed inverter can be operated for 6 modes

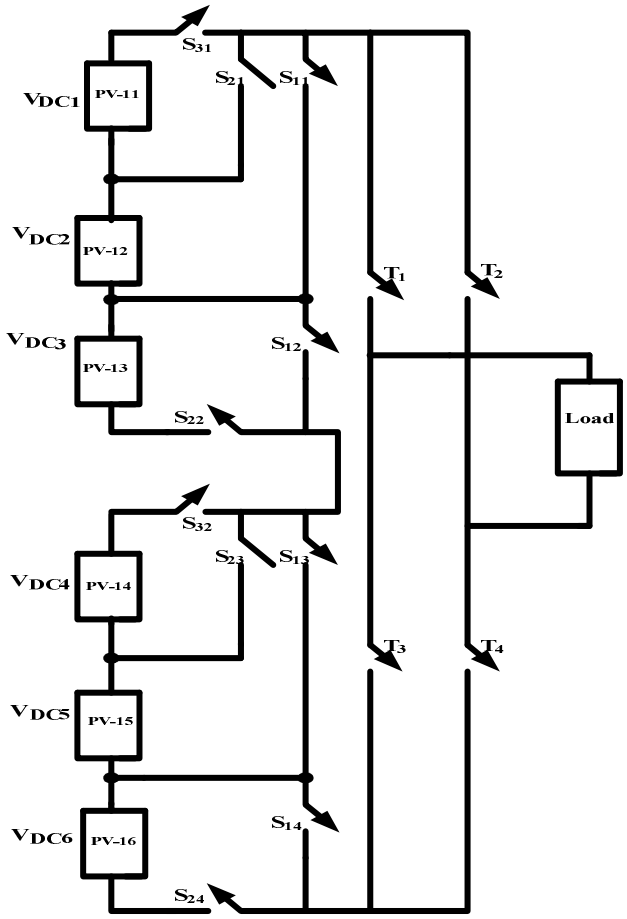

Fig. 1. Equivalent Structure of Single Phase PV system fed 13-level DCLMLHBI

3. Modulation Schemes

3.1 Sinusoidal Pulse Width Modulation for Single Phase DCLMLHBI

Sinusoidal Pulse Width Modulation (SPWM) scheme is adopted for single phase DCLMLHBI systems. For SPWM pulse generation, sinusoidal signal acts as reference and triangular signals act as carrier. For synthesizing 13-level AC output from the PV systems, (n-1)/2 carrier triangular signals are needed. The switching frequency of the carrier signals are considered to be 20 kHz for both single and three-phase converters. Also, both the converter systems are analyzed for various amplitude modulation indices (M_a).

Sinusoidal reference signal is expressed using equation (3)

$$V_{ref} = V_m \sin \omega t \tag{3}$$

SPWM pulses are generated using the logical equations (4) to (11)

$$P_{S11} = \overline{P_1 > V^*_{ref}} \tag{4}$$

$$P_{S21} = \overline{P_2 > V^*_{ref}} * P_2 > V^*_{ref} * V^*_{ref} < 3 \tag{5}$$

$$P_{S'21} = P_3 > V^*_{ref} \tag{6}$$

$$P_{S31} = P_2 > V^*_{ref} \tag{7}$$

$$P_{S12} = \overline{P_4 > V^*_{ref}} \tag{8}$$

$$P_{S22} = \overline{P_7 > V^*_{ref}} * P_4 > V^*_{ref} * V^*_{ref} < 6 \quad (9)$$

$$P_{S'22} = P_5 > V^*_{ref} \quad (10)$$

$$P_{S'32} = P_6 > V^*_{ref} \quad (11)$$

Triangular carrier signals are developed based on the consideration of the lookup table expressed in equations (12) and (13)

$$P_1 = [0\ 1\ 0] \quad (12)$$

$$P_i = [x+1\ y+1\ z+1];\ i = 2, 3, 4, 5, 6;\ x=0, y=1, z=0 \quad (13)$$

4. Experimentation of 13-level DCLMLHBI System

Carrier signals are generated by the signal modulator in PIC 16F877A and compared with the corresponding positive sequence reference signals (S_1, S_2 and S_3). The switching patterns are developed based on the logic equations (18) to (64). These logic equations are promoted in the inbuilt logic operators of the SPWM IC. The hardware specification of the DCLMLHBI are indicated as; Symmetrical DC source (V_{dc}) = 50 V, Switching frequency (f_s) = 20 kHz, Gate drive IC; IR2110, Switch MOSFET; IRF840 and Opto-coupler; MCT2E. Table 1 shows comparative analysis of required power switches for conventional CMLI and proposed DCLMLHBI system. From the analysis, it is inferred that the proposed DCLMLHBI system has 33.33% lesser power switches than conventional CMLI system.

Table 1. Power Switch Count Analysis

Levels	Single Phase System		Three-Phase System	
	Conventional CMLI	**Proposed DCLMLHBI**	**Conventional CMLI**	**Proposed DCLMLHBI**
7	12	10	36	30
13	**24**	**13**	**72**	**39**

5. Results and Discussion

5.1 Simulation Results and Discussion of Single Phase DCLMLHBI system

The single phase DCLMLHBI output voltage (V_m= 311 V) and load current (I_m= 2.9 A) waveforms are shown in Fig.2 and Fig. 3 respectively. From the output voltage waveform, it is inferred that the output voltage is synthesized with 13-levels of DC voltages.

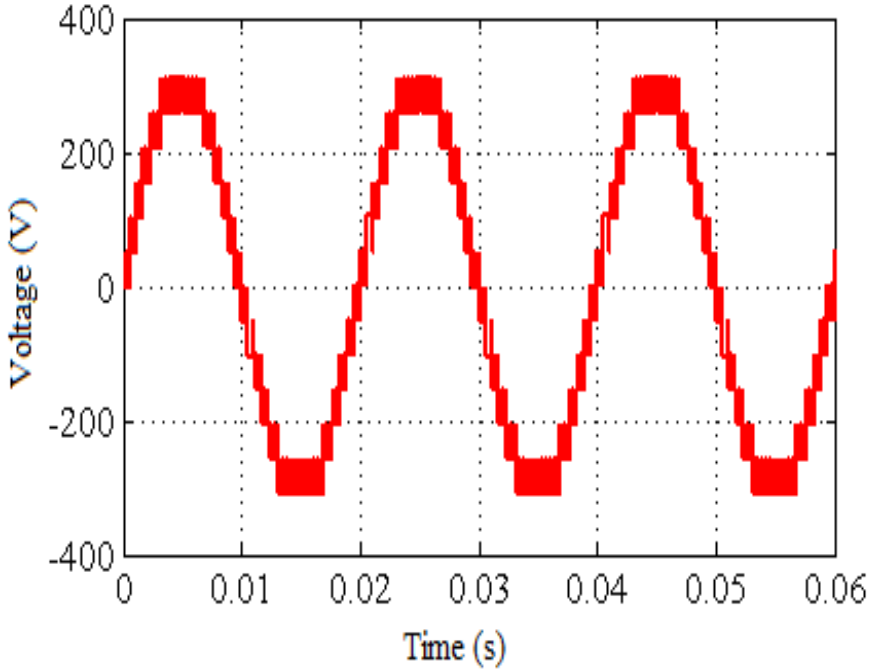

Fig. 2. Inverter Output Voltage of Single Phase DCLMLHBI System

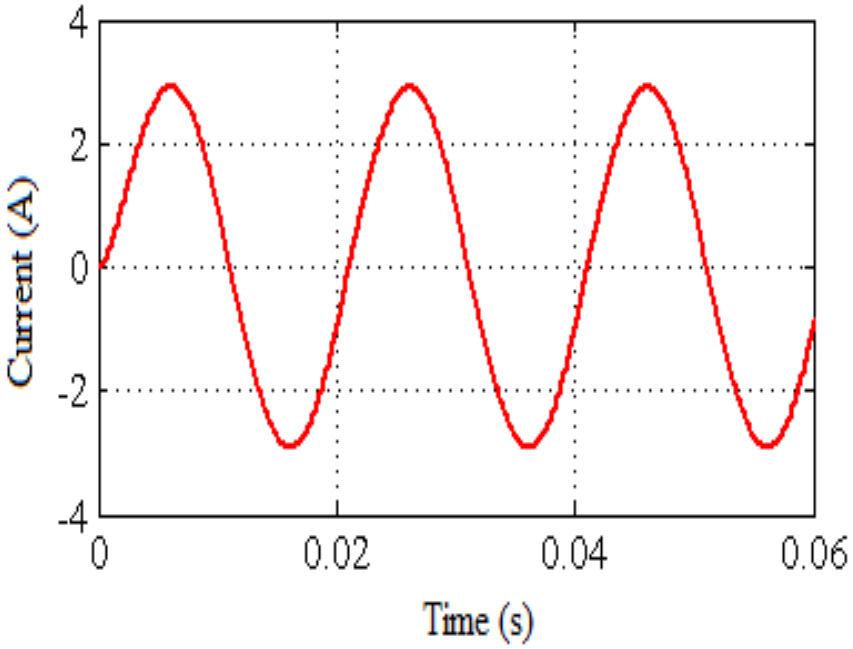

Fig. 3. Load Current (Single Phase)

The THD spectrum of the single phase inverter output voltage is shown in Fig.4. From the spectrum it is observed that the inverter generates the output voltage with the THD of 4.48%. Individual order voltage harmonics of the proposed inverter is shown in Fig.5. From the analysis, it is understood that the inverter synthesis the output voltage with reduced lower order harmonics.

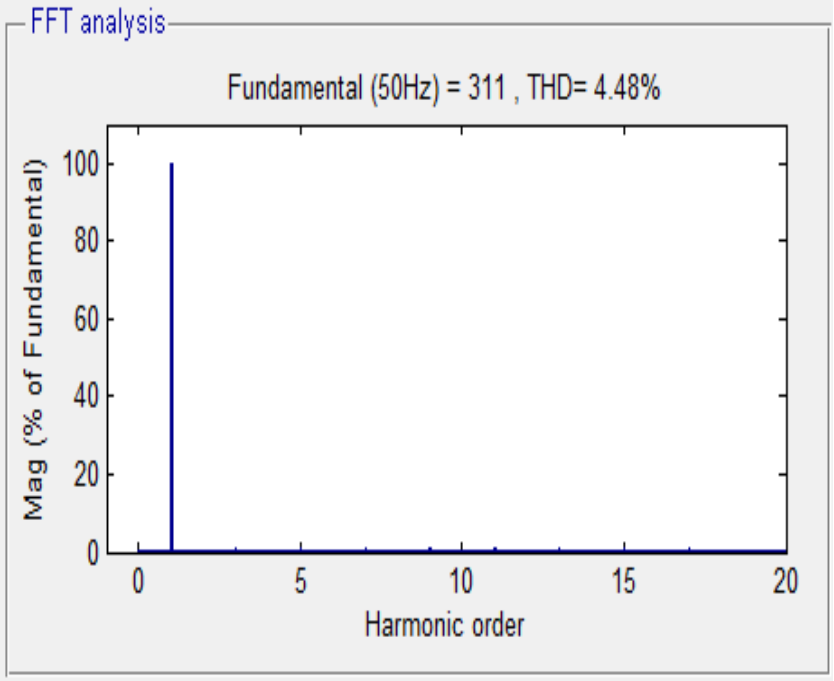

Fig. 4. Output Voltage THD Spectrum (Single Phase)

The PSD analysis for the single phase inverter output voltage is shown in Fig.6. Proposed inverter switching frequency is considered to be 20 kHz. In principle, the density of power in the multiples of switching frequency is the root cause for voltage stress and switching loss. The attained 13-level output voltage power density values in the multiples of switching frequency are 4 dB/Hz, -8 dB/Hz, 16 dB/Hz, 20 dB/Hz and 21 dB/Hz for 20 kHz, 40 kHz, 60 kHz, 80 kHz and 100 kHz respectively. From the analysis, it is clear that the proposed system generates the output voltage with reduced voltage stress.

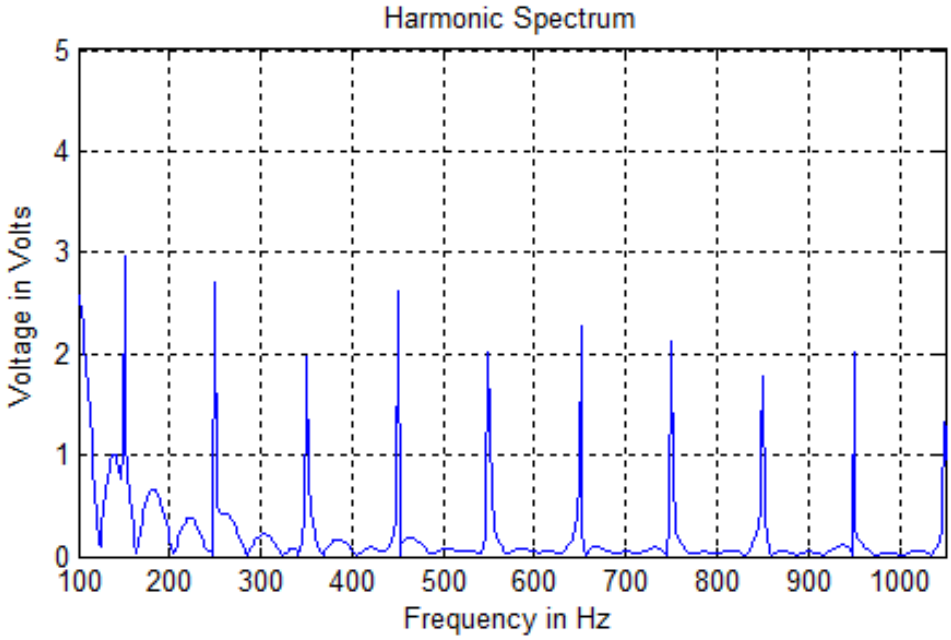

Fig. 5. Individual Order Voltage Harmonic Analysis (Single Phase)

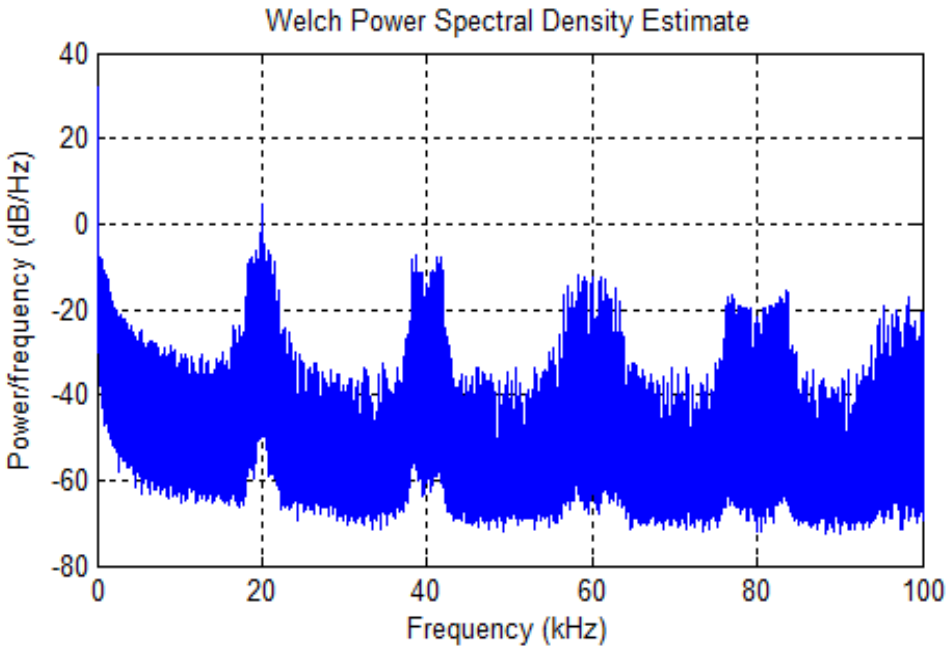

Fig. 6. Output Voltage Power Density Spectrum (Single Phase)

5.2 Hardware Results and Discussion

Fig. 7 shows the driver circuit output SPWM pulses to DC link MOSFET power switch S_{11}. From the result, it is observed that the magnitude and switching frequency of the SPWM pulses are 15 V and 20 kHz respectively. Fig. 8 shows the experimental source voltage (V_{DC1}= 48 V) of single phase 13-1evel DCLMLHBI system.

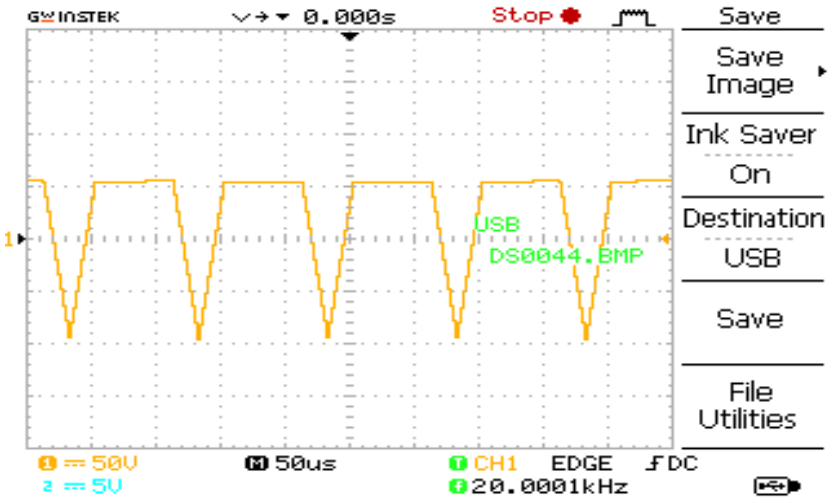

Fig. 7. SPWM Pulse to S_{11}

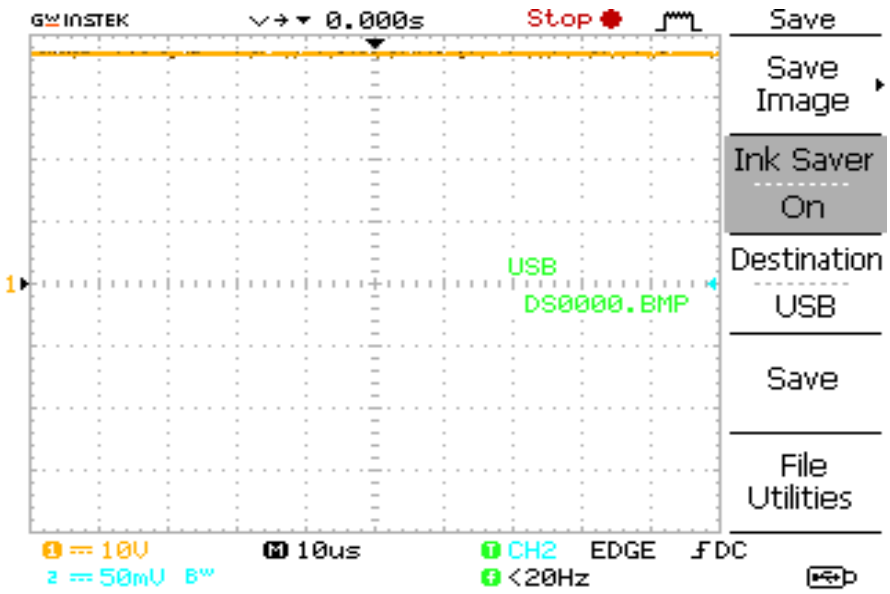

Fig. 8. Experimental Source Voltage (V_{DC1})

Fig. 9 shows the experimental output voltage waveform of single phase 13-1evel DCLMLHBI system. The proposed system consists of six symmetrical DC sources with the voltage rating of 48 V. The maximum output voltage of 288 V (V_{rms}= 203.6 V) is developed from the symmetrical DC sources.

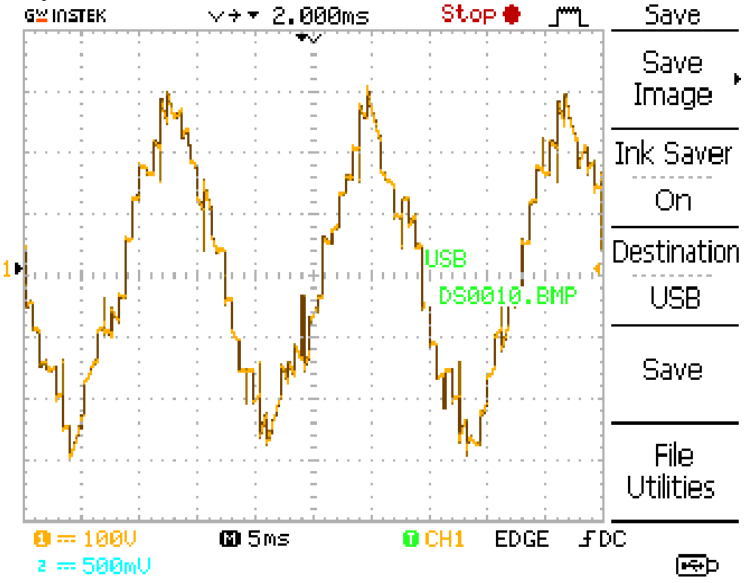

Fig. 9. Experimented Output Voltage of DCLMLHBI

The experimental voltage FFT spectrum of DCLMLHBI is shown in Fig. 10. From the spectrum it is inferred that the 13-level DCLMLHBI system has reduced voltage stress in the multiples of switching frequency (voltage values are negative). The entire system is assembled in a single board and experimented for single phase AC voltage. The experimental setup of the proposed system is shown in Fig. 10. The experimental setup is developed using six rectifier units, DC link units, H-Bridge inverter unit and controller unit.

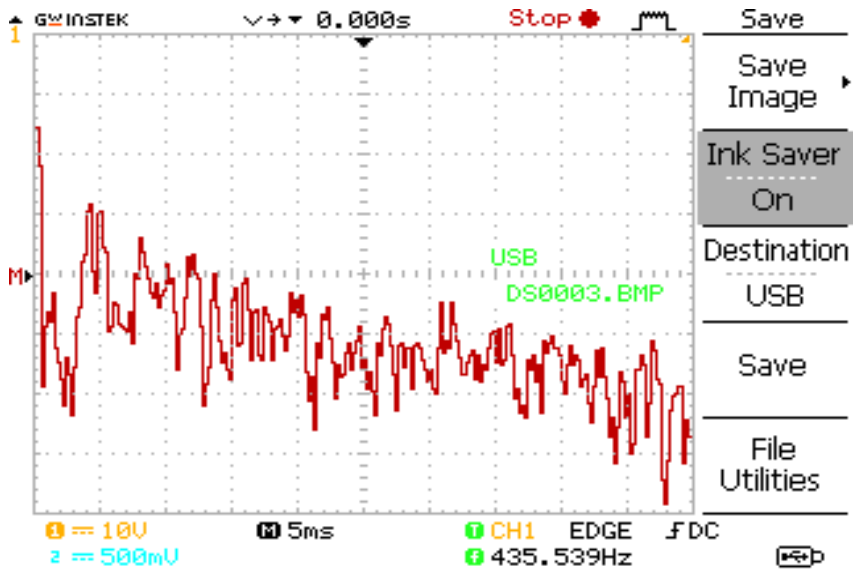

Fig. 10. Output voltage FFT analysis of single-phase DCLMLHBI

6. Conclusion

Individual harmonics, THD and PSD in the multiples of switching frequency are reduced in the proposed inverter through its modulation schemes. Compared to conventional CMLI topology, the proposed 13-level DCLMLHBI required 33.33 % reduced power switches and its gate drive circuits. From the harmonic analysis, it is clear that the output voltage and load current harmonics profile of the 13-level DCLMLHBI meet the terms with IEEE standard 519:2014. The proposed inverter has reduced voltage stress across the inverter switches and consider more suitable for propionate solar power applications.

References

[1] Ilhami Colak, Ersan Kabalci, Ramazan Bayindir: 'Review of multilevel voltage source inverter topologies and control schemes', International Journal of Energy Conversion Management, 2010, **9**, pp. 1-15.

[2] Lai, JS, Peng, FZ: 'Multilevel converters-A new breed of power converters', IEEE Trans. Ind. Applicat., 1996, **6** (32), pp. 509-517.

[3] Rodriguez, J, Lai, JS, Peng, FZ. Multilevel inverters: 'A survey of topologies, controls, and applications', IEEE Trans. Ind. Electron., 2002, **8**, (49), pp. 724-738.

[4] Liu, Y., Hong, H., Huang, A. Q.: 'Real-time algorithm for minimizing THD in multilevel inverters with unequal or varying voltage steps under staircase modulation', IEEE Trans. Ind. Electron., 2009, **6**, (56), pp. 2249-2258.

[5] Rodriguez, J, Bernet,S, Pontt, JO, Kouro, S: 'Multilevel voltage source converter topologies for industrial medium voltage drives', IEEE Trans. Ind. Electron., 2007, **6**, (54), pp. 724-738.

[6] Dzung Nguyen, and Brad Lehman: 'An adaptive solar photovoltaic array using model-based reconfiguration algorithm', IEEE Trans. Ind. Electron., 2008, **7**, (55), pp. 2644-2654.

[7] Oscar Lopez-Lapena, Maria Teresa Penella, and Manel Gasulla: 'A new MPPT method for low-power solar energy harvesting,' IEEE Trans. Ind. Electron., 2010, 9, (57), pp. 3129-3138.

[8] Sachin Jain and Vivek Agarwal: 'Single-stage grid connected inverter topology for solar PV systems with maximum power point tracking,' IEEE Trans. Power Electron., 2007, **5**, (55), pp. 1928-1940

[9] Jeyraj Selvaraj and Nasrudin A. Rahim: 'Multilevel Inverter For Grid-Connected PV System Employing Digital PI Controller', IEEE Trans. Ind. Electron., 2009, **1**, (56), pp.149-158.

[10] N.A. Rahim, K. Chaniago, J. Selvaraj: 'Single-Phase Seven-Level Grid Connected Inverter for Photovoltaic System', IEEE Trans. Ind. Electron., 2011, **6**, (58), pp. 2435-2443.

[11] S.J. Park, F.S. Kang, M.H. Lee, C.U. Kim: 'A New Single-Phase Five-Level PWM Inverter Employing a Deadbeat Control Scheme,' IEEE Trans. Power Electron., 2003, **3**, (18), pp. 831-843.

[12] Kangarlu, MK, Babaei, E: 'A generalized cascaded multilevel inverter using series connection of sub multilevel inverters', IEEE Trans. Power Electron., 2013, **2**, (28), pp. 625–636.

[13] Babaei, E.: 'A cascade multilevel converter topology with reduced number of switches', IEEE Trans. Power Electron., 2008, **11**, (23), pp. 2657-2664.
[14] Ramasami Uthirasamy, Uthandipalayam Subramaniyam Ragupathy, Venkatachalam Kumar Chinnaiyan: Structure of boost DC-link cascaded multilevel inverter for uninterrupted power supply applications', IET Power Electronics, 2015, **8**, (11), pp.2085-2096.
[15] Amit Kumar Gupta, and Ashwin M. Khambadkone: 'A Space Vector PWM Scheme for Multilevel Inverters Based on Two-Level Space Vector PWM" IEEE Trans. Ind. Applicat., 2006, **5** (53), pp. 1631-1639.
[16] Charles I. Odeh, Vincent N. Agu, Nentawe Goshwe: 'Cascaded three-phase pulse-width modulated switched voltage source inverter', IET Power Electronics, 2014, **7**, (7), pp. 1925-1983.
[17] Gupta,AK, Khambadkone, AM.: 'A general space vector PWM algorithm for multilevel inverters, including operation in over modulation range. , IEEE Trans. Power Electron, 2007, **(2)** 22, pp. 517 –526.
[18] Aneesh Mohamed, AS, Gopinath, A, Baiju, MR: 'A simple space vector PWM generation scheme for any general n-level inverter', IEEE Trans. Ind. Electron., 2009, **5**, (56), pp. 1649-1656.
[19] Kang, DW, Lee,YN, Suh, BS, Choi, CH, Hyun, DS: 'An improved carrier-based SVPWM method using leg voltage redundancies in generalized cascaded multilevel inverter topology,' IEEE Trans. Power Electron, 2003, **(1)** 18, pp. 180–187.
[20] Brendan Peter McGrath, Donald Grahame Holmes: 'Multicarrier PWM strategies for multilevel inverters', IEEE Trans. Ind. Electron., 2002, **8**, (49), pp. 858-867.
[21] Charles I. Odeh, Vincent N. Agu, Nentawe Goshwe: 'Cascaded three-phase pulse-width modulated switched voltage source inverter', IET Power Electronics, 2014, **7**, (7), pp. 1925-1983.
[22] Wenxi Yao, Haibing Hu, Zhengyu Lu: 'Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter', IEEE Trans. Power Electron., 2008, **1**, (23), pp. 45-51.