High performance synchronization method is critical for grid connected power converter. For single-phase system, power based phase-locked loop (pPLL) uses a multiplier as phase detector (PD). As single-phase grid voltage is distorted, the phase error information contains ac disturbances oscillating at integer multiples of fundamental frequency which lead to detection error. This paper presents a new scheme based on moving average filter (MAF) applied in-loop of pPLL. The signal characteristic of phase error is discussed in detail. A predictive rule is adopted to compensate the delay induced by MAF, thus achieving fast dynamic response. In the case of frequency deviate from nominal, estimated frequency is fed back to adjust the filter window length of MAF and buffer size of predictive rule. Simulation and experimental results show that proposed PLL achieves good performance under adverse grid conditions.

Keywords: Phase-locked loop; Fictitious Power; Moving Average Filter; Frequency Adaptive; Digital Signal Processor.

Article history: Received 12 March 2015, Accepted 1 March 2017

1. Introduction

Grid connected power converters requires precise detection of the voltage phase angle for synchronization. Among different techniques, Phase-Locked Loop (PLL) is widely used in industry [1]. Essentially, PLL is a closed-loop control system and consists of three major parts, as shown in Fig.1. The first part is the Phase Detector (PD), which detects the phase error between the input signal $u_i$ and the output signal $u_o$. Secondly, Loop Filter (LF) eliminates the high-frequency components of the phase error. The phase angle is acquired by Voltage-Controlled Oscillator (VCO). Since continuous closed-loop adjustment, the output $u_o$ tracks the input $u_i$ till the phase error maintains to zero.

![Fig. 1. Typical structure of PLL](image)

The most popular PLL scheme is Synchronous Reference Frame Phase-Locked Loop (SRF-PLL) [2], which uses Park transform as PD for three-phase system. For single-phase system, the known signal is the grid voltage. If a signal quadrature with the grid voltage is constructed, the SRF-PLL can be easily applied to single-phase system. Hence, the...
quadrature signal generator (QSG) is the key unit [3]–[7]. As the single-phase voltage is clean, SRF-PLL with QSG works well not only with zero steady phase error but also with fast dynamic response. In fact, power utility always suffers all kinds of faults and disturbances. As a result, single-phase voltage may be harmonic distorted, sag/swell, notch, noise, frequency deviation and other types of abnormal state. Under such conditions, the aim of the synchronization is to track the phase angle of the fundamental component. Thus, additional filter should be set in front of PD to extract the fundamental [8]. The computational burden of these pre-filter methods is high, which is complicated to realize.

Power based PLL uses fictitious power as PD. Phase error information is gotten by a multiplier [9]. As the single-phase voltage is distorted, the multiplier based PD contains disturbances. It causes phase error information inaccurate, leading phase detection error. The filter places within the closed control loop to conceal these disturbances, always before the LF. Notch filter has been proposed to cancel the second-order disturbance appeared in PD high efficiently when grid voltage is clean [10]. However, it is not suitable for the serious distorted condition. The high order low-pass filter can attenuate most disturbances in PD, but the time constant is larger. Because of longer time delay introduced inevitable, the bandwidth of PLL should be tuned as high as possible. Moving Average Filter (MAF) is an attractive solution [11]-[13]. It is efficient to conceal the in-loop disturbances while single-phase grid voltage is distorted seriously. More specifically, MAF is a low-pass filter with multi-point notch attenuation that blocking disturbances completely only leaving dc component as fundamental phase error signal.

This paper provides a detailed analysis and digital implementation of MAF applied in-loop of pPLL. The scheme obtains zero detected error under adverse grid conditions. It is organized as follows. The signal characteristic of phase error under adverse conditions by pPLL is explained firstly. The basis theory of the proposed MAF-pPLL is presented, including the delay analysis, frequency adaptive technique, small signal model and guidelines for key parameter design. Finally, simulation results are shown and experimental results based on TMS320F28377s are obtained to verify the effectiveness.

2. Power Based Phase Error Detector Under Distorted Condition

A single-phase system grid voltage with the dc offset and harmonics distorted can be expressed as

\[
u = U_{dc} + U_1 \cos(\omega_1 t + \phi_1) + \sum_{n=2}^{\infty} U_n \cos(n\omega_1 t + \phi_n) = U_{dc} + U_1 \cos(\theta_1) + f(2\omega_1, 3\omega_1, 4\omega_1, \cdots)\]

(1)

where \(U_{dc}\) represents the amplitude of grid voltage dc components in V, \(U_n\) represents the amplitude of \(n\)th harmonic in V, \(\omega_1=2\pi f_1=2\pi 50\) rad/s is the fundamental frequency, \(\phi_n\) represents the initial phase angle of \(n\)th harmonic in rad, and \(\theta_1\) represents the phase angle of fundamental component in rad.

A feedback signal denotes \(i\) as

\[
i = \sin \hat{\theta}_1 = \sin(\omega_1 t + \hat{\phi}_1)\]

(2)

where \(\hat{\theta}_1\) represents the detected value of \(\theta_1\), \(\hat{\phi}_1\) represents the detected value of \(\omega_1\).

A fictitious power can be defined as
\[ p = ui \]
\[ = [U_{dc} + U_I \cos(\omega t + \phi_I) + f(2\omega, 3\omega, 4\omega \cdots)] \times \sin(\hat{\omega}t + \hat{\phi}_I) \]
\[ = U_{dc} \sin(\hat{\omega}t + \hat{\phi}_I) + U_I \cos(\omega t + \phi_I) \sin(\hat{\omega}t + \hat{\phi}_I) + f(2\omega, 3\omega, 4\omega \cdots) \sin(\hat{\omega}t + \hat{\phi}_I). \quad (3) \]
\[ = U_{dc} \sin(\hat{\omega}t + \hat{\phi}_I) \]
\[ + \frac{1}{2} U_I \{ \sin((\omega t + \phi_I + (\hat{\omega}t + \hat{\phi}_I)) - \sin((\omega t + \phi_I) - (\hat{\omega}t + \hat{\phi}_I)) \}
\[ + f(2\omega, 3\omega, 4\omega \cdots) \sin(\hat{\omega}t + \hat{\phi}_I) \]

Suppose \( \hat{\omega}_I = \omega_I \), then we have
\[ p = U_{dc} \sin(\hat{\omega}t + \hat{\phi}_I) + \frac{1}{2} U_I \{ \sin(2\omega t + \phi_I + \hat{\phi}_I) - \sin(\theta_I - \hat{\theta}_I) \}
\[ + f(2\omega, 3\omega, 4\omega \cdots) \sin(\hat{\omega}t + \hat{\phi}_I). \quad (4) \]

It is clear from (4) that \( n \)th harmonic of input voltage appears \((n \pm 1)\)th ac component in \( p \). Specifically, the fundamental component of input voltage appears a dc term and a double-frequency oscillating disturbance in \( p \). Hence, the phase error information of fundamental is reflected by the dc term in \( p \). Taking fictitious power as PD, the dc term should be kept whereas all the other ac disturbances should be filtered out, as shown below
\[ p = -\frac{1}{2} U_I \sin(\theta_I - \hat{\theta}_I) = -\frac{1}{2} U_I (\theta_I - \hat{\theta}_I). \quad (5) \]

Based on classic closed loop PLL, the block diagram of power based pPLL is shown in Fig.2. The filter unit should block all of the high order disturbances in (4).

**3. Moving Average Filter**

Moving Average Filter is considered as follows [12]
\[ \bar{x}(t) = \frac{1}{T_w} \int_{t-T_w}^{t} x(\tau) d\tau \]
where \( T_w \) is the filter window length, \( x(t) \) is the signal to be filtered, and \( \bar{x}(t) \) is the output.

The transfer function of (6) is given by
\[ G_{MAF}(s) = \frac{\bar{x}(s)}{x(s)} = \frac{1-e^{-T_w s}}{T_w s}. \quad (7) \]

The Bode of (7) is shown in Fig. 3, and \( T_w = 0.02s \). It can be implied that MAF is a low-pass filter with multi-point notch attenuation at frequencies \( f_d = n/T_w \quad (n = 1, 2, 3 \ldots) \) in Hz. MAF blocks these disturbances while with unity gain for dc component. If proper filter window length is selected, the notch adjusts to integer multiples of fundamental frequency.
Equation (8) shows that MAF is a Finite Impulse Response filter with linear phase, thus the steady state delay could be compensated for real time control. To meet ac disturbances in (4), $T_w$ should be selected as

$$T_w = NT_s$$  \hspace{1cm} (9)$$

$$N = \frac{T_w}{T_s} = \frac{1}{T_s f_d}$$  \hspace{1cm} (10)$$

where $f_d$ is the fundamental frequency of disturbances in (4), always 50Hz. In consideration of $T_s$ is fixed, $T_w$ can be adjusted by changing $N$ according to the grid frequency.

Considering the computation accuracy, the equation (8) can be rewritten as

$$\bar{x}(t) = \frac{1}{T_w} \int_{T_{i-1}}^{t} x(\tau) d\tau = \bar{x}(k)$$

$$\approx \frac{T_s}{T_w} \left\{ \sum_{i=0}^{N_r} x(k-i) + \Delta \cdot [(1-\Delta) \cdot x(k-N_r-1) + \Delta \cdot x(k-N_r)] \right\}$$ \hspace{1cm} (11)$$

where

$$\Delta = \frac{T_w - N_r T_s}{T_s}$$ \hspace{1cm} (12)$$

$$N_r = \text{int} \left( \frac{T_w}{T_s} \right) = \text{int} \left( \frac{1}{T_s f_d} \right)$$ \hspace{1cm} (13)$$

$N_r$ is round down of (13).

It has been proved in [12] that the linear interpolation method (11) can improve MAF performance dramatically. The method is depicted in Fig.4.

As explained, the time constant of MAF is...
\[ \tau_d = T_w / 2 \]  

Fig. 5 illustrates step response of MAF. In order to compensate the delay, a predictive method has been presented in [10]. To explain the method, the PD output in Fig. 2 is always a linear value in steady state.

\[ d_w T = \tau \]

Fig. 4. Linear interpolation method

The dc term of PD can be expressed
\[ \bar{p}(k+1) = \bar{p}(k) + mT_s \]
\[ = \bar{p}(k) + m \frac{1}{f_s} \]  

where \( \bar{p}(k) \) represents current sample of \( \bar{p}(t) \), \( f_s \) represents the sample frequency, \( m \) represents the slope of \( \bar{p}(t) \).

In the same way
\[ \overline{p}(k + 2) = \overline{p}(k + 1) + mT_s \]
\[ = \overline{p}(k + 1) + m \frac{1}{f_s}. \quad (16) \]

A predictive equation can be derived from (16) and (17)
\[ \overline{p}(k + 2) = 2\overline{p}(k + 1) - \overline{p}(k). \quad (17) \]

As mentioned before, the delay time of MAF can be digitalized
\[ N' = \frac{1}{2} \frac{T_w}{T_s} = \frac{1}{2} N. \quad (18) \]

Applying (18) to (17), got
\[ \overline{p}(k + N') = 2\overline{p}(k + N' - 1) - \overline{p}(k + N' - 2) \]
\[ = (N' + 1)\overline{p}(k) - N'\overline{p}(k - 1). \quad (19) \]

Equation (19) is a predictive rule, implying that the future output of \( N' \) can be predicted by current output \( \overline{p}(k) \) and previous output \( \overline{p}(k - 1) \). Fig.6 deserves slope response of MAF with delay compensation (19). It should be noted that the steady state delay was compensated completely.

![Fig. 6. Slope response of MAF with delay compensation](image)

**4. MAF-pPLL**

As aforementioned, MAF can be applied to filter out the ac disturbances of PD, especially effective for distorted grid voltage. MAF-pPLL block diagram is shown in Fig.7.
In the case of grid voltage frequency deviation, the ac disturbances fundamental frequency of PD varies. In view of this fact, the detected frequency is fed back to update the MAF filter window length $T_w$ and $N'$ in (19) online.

An approximate small signal linear control model of MAF-pPLL is available in Fig. 8. The amplitude of fundamental $U_1$ is a gain in forward path. The dynamic response of PLL will be affected by $U_1$. This drawback can be eliminated by normalized input voltage.

The LF using PI regulator as follow

$$K_f(s) = k_p + \frac{k_i}{s}$$

where $k_p$ represents proportion gain, $k_i$ represents integral gain.

The transfer function of MAF can be approximate with following

$$G_{MAF}(s) = \frac{1 - e^{-T_w s}}{T_w s} \approx \frac{1 - \frac{T_w s / 2}{1 + T_w s / 2}}{T_w s / 2} = \frac{1}{1 + T_w s / 2}.$$  \hspace{1cm} (21)

Then, the open-loop transfer function of Fig.8 can be given by

$$H_{ol}(s) = \frac{U_1}{2} \left( k_p + \frac{k_i}{s} \right) G_{MAF}(s) \frac{1}{s}$$

$$= \frac{U_1}{2} \left( k_p s + k_i \right) \frac{1}{s} \frac{1}{1 + T_w s / 2} \frac{1}{s}$$

$$= \frac{U_1}{2} \frac{2/T_w \cdot (k_p s + k_i)}{s^2 (s + 2/T_w)}.$$  \hspace{1cm} (22)

Equation (22) is a typical second order system, where
\[
\begin{align*}
\omega_p &= \omega_c / b \\
k_p &= 2 \omega_c / U_1 \\
k_i &= 2 \omega_c^2 / b U_1
\end{align*}
\]  
(23)

\(b\) is a constant which is a tradeoff between dynamic and steady state characteristics.

\[
\begin{align*}
\omega_c &= 2 / T_w b \\
k_p &= 4 / U_1 T_w b \\
k_i &= 8 / U_1 T_w^2 b^3
\end{align*}
\]  
(24)

In general symmetrical optimum method [2],[14],[15], LF parameters can be determined as follows

\[
\begin{align*}
k_p &= 4 / V_1^* T_w b \\
k_i &= 8 / V_1^* T_w^2 b^3
\end{align*}
\]  
(25)

where \(T_w=0.02s\), \(U_1=1\), and \(b\) can be set to 2.4, to make a tradeoff between rapidly and stability.

5. Simulation Results

To demonstrate the effectiveness of the MAF-pPLL, this method was simulated by Matlab/Simulink. The results are shown in Figs.9-15 for different scenarios. Each test scenarios presents four graphics (from top to bottom) input voltage\((u_i)\), detected phase angle\((\hat{\theta})\), detected frequency\((\hat{f})\), and phase error\((\hat{\theta} - \hat{\theta})\).

A. Amplitude Step

Fig.9 shows the simulation results of input voltage amplitude step. The amplitude of input voltage steps down from 1pu to 0.4pu at 0.25s. At 0.4s, it returns to nominal. At 0.5s, it steps up to 1.6pu and then back to nominal at 0.6s. It can be observed that the steady-state error of both phase angle and frequency are zero. The overshoot of phase angle is no more than 10 degrees, while peak frequency error is less than 5 Hz. As mentioned earlier, the amplitude of input voltage is a gain in the forward path. Since the amplitude of phase is small, the dynamic response becomes slower. This point can be implied from first transition process of phase error profile. The process is longer than other three.
Fig. 9. Simulation results of a sag or step up of 60% in input voltage

**B. Phase Jump**

Phase jump is a common perturbation in power supply grid. Fig. 10 displays the simulation results of this condition. At 0.25s, Phase angle jump is occurring with 60 degrees. At 0.4s, Phase angle jumps 15 degrees, and 90 degrees at 0.55s. The MAF-pPLL tracks phase angle correctly since the steady-state error for both the phase angle and frequency are zero.

Fig. 10. Simulation results of phase jump in input voltage
C. Distorted

Simulation results are presented in Fig.11 when the input voltage is distorted. From 0.25s to 0.4s, 0.3pu of 3rd harmonic is injected based on the fundamental component. At 0.4s, 0.2pu of 5th harmonic is added. At 0.6s, 0.3pu of 7th harmonic is added yet. The PLL exhibits zero steady-state error for all kind of harmonics. The overshoot of phase angle is no more than 1 degree. MAF-pPLL is very suitable for distorted input as shown.

![Fig. 11. Simulation results of distortion input voltage](image)

D. Frequency deviation

Fig.12 illustrates the simulation results of frequency deviation in input voltage with frequency adaptive technique. The frequency steps up from 50Hz to 55Hz at 0.03s, and back to 50Hz at 0.35s. At 0.55s, the frequency steps down to 45Hz. Because the filter window length of MAF is adjusting online with respect to the input, the disturbances of PD were totally filtered out. Thus, the steady-state error of both the detected phase angle and frequency are zero. As it can be seen, without the frequency adaptive technique, the comparison results are illustrated in Fig .13. Both the detected phase error and frequency show steady-state ripples. Comparison diagram of phase error is displayed in Fig.14 between 0.65s and 0.7s. Notice that the peak-to-peak phase error without frequency adaptive technique is about 1 degree.
Menxi Xie et al: Power Based Phase-Locked Loop Under Adverse Conditions ...

Fig. 12. Simulation results of frequency deviation in input voltage

Fig. 13. Simulation results of frequency deviation in input voltage without frequency adaptive technique

Fig. 14. Comparison of steady phase error with or without frequency adaptive technique

E. *DC Offset*

Fig. 15 shows the simulation results of input voltage with dc offset. Specifically, the input voltage amplitude experiences a step of 0.1pu dc offset at 0.255s. Then, it returns to nominal at 0.4s. Finally, it experiences another step of 0.3pu dc offset at 0.51s.

The steady-state error of both the detected phase angle and frequency are zero. The overshoot of phase angle error is no more than 10 degrees, while frequency overshoot is less than 5 Hz.
6. Experimental Results

An experimental platform has been set up with floating point digital signal processor TMS320F28377S. The input voltage signal is generated by DSP software internal. The on-chip 12 bits AD module captures the input as voltage signal. The sample frequency is 10 KHz, and the MAF-pPLL algorithm is executed every 0.0001s in an interrupt routine. For trigonometric computation, the routine calls TI's optimized floating point library directly. In order to minimize high-speed accumulated computing error, the integration is implemented by discrete back Euler method, and PI regulator uses incremental structure. The interesting internal variables were sent to the on chip digital-to-analog module for oscilloscope display. The experimental tests are set to agree with simulation scenarios.

Fig.16 displays experimental results of amplitude step, where it can be seen that the response is fast. Fig.17 depicts experimental results of phase angle jump, and the transition process only takes 2 cycles.
Fig. 16 Experimental results of amplitude step in input voltage

Fig. 17 Experimental results of phase angle jump in input voltage
Fig. 18 Experimental results of frequency step from 50 to 55 Hz in input voltage with frequency adaptive technique

Fig. 19 Experimental results of frequency step from 50 to 55 Hz in input voltage without frequency adaptive technique

The comparison results obtained with or without MAF frequency adaptive technique under the frequency step are shown, in Fig.18 and Fig.19 respectively. The detected frequency error exists clearly in Fig.19, which is oscillated at double of input frequency without frequency adaptive technique.

Fig. 20 illustrates experimental results for the scenario with harmonic distortion in input voltage, and the harmonic contents are as same as the simulation. The measured ripples for
both the frequency and phase error are zero, which are in agreement with the simulation results.

Fig. 20 Experimental results of harmonic distorted in input voltage

Fig. 21 Experimental results for the scenario with DC offset in the input voltage. It shows that the dynamic response is rather fast. Furthermore, the DC rejection ability by setting MAF window 0.02s brings zero phase error.

Fig. 21 Experimental results of dc offset in input voltage
7. Conclusion

Synchronization is of great importance for grid-connected power converter since precise phase angle information of the converter control. This paper presents a detailed research for MAF-pPLL of for single-phase system. The method can be realized easily in digital form, and the computing burden is small. The simulation and experimental results verify the effectiveness of the method, and it exhibits excellent performance under adverse conditions.

8. Acknowledgement

This work is supported by the National Natural Science Foundation of China (under Grant No. 51307113 and 51407124), the Natural Science Foundation of Jiangsu Province (under Grant No. BK20130307).

References