Ahmed Zama[1*], Seddik Bacha [1,2], Abdelkrim Benchaib [1], David Frey[1,2] and Sebastien Silvant[1]

J. Electrical Systems 12-4 (2016): 649-659

Journal of Electrical Systems

Regular paper

A novel modular multilevel converter modelling technique based on semi-analytical models for HVDC application

Thanks to scalability, performance and efficiency, the Modular Multilevel Converter (MMC), since its invention, becomes an attractive topology in industrial applications such as high voltage direct current (HVDC) transmission system. However, modelling challenges related to the high number of switching elements in the MMC are highlighted when such systems are integrated into large simulated networks for stability or protection algorithms testing. In this work, a novel dynamic models for MMC is proposed. The proposed models are intended to simplify modeling challenges related to the high number of switching elements in the MMC. The models can be easily used to simulate the converter for stability analysis or protection algorithms for HVDC grids.

Keywords: HVDC transmission; modular multilevel converter (MMC); full order model, reduced order model.

Article history: Received 20 April 2016, Accepted 11 August 2016

1. Introduction

Renewable energy generation, in form of offshore windfarms, is rapidly growing. The power generated has to be transmitted in order to make a connection to an AC network. In [1, 2], it has been proved that the optimal solution for such energy transmission is the High Voltage Direct Current (HVDC) technology. With the development of voltage source converter (VSC), the concept of connecting several off-shore wind farms with several onshore AC grids based on VSCs has become conceivable and can provide more flexibility in integration of renewable energy [3,4].

Compared with classical two level Voltage Source Converters (VSC), HVDC systems based on Modular Multilevel Converter (MMC) offer significant advantages. Regarding these advantages, straightforward voltage balancing, possibility of imbalanced operation, harmonic reduction…, it has been proved [1] that all the future HVDC developments will be based on such devices.

This topology, invented by [5], helps reducing converter losses by using low switching frequency. In addition, filter requirements are mitigated by using a significant number of submodules (SMs) per phase. However, the large number of SM in the MMC introduces modelling challenges. For instance, in the electromagnetic transient (EMT) simulation programs, the switching operation is modelled by admittance matrix; the dimension of this matrix is given by the converters state variables number. This matrix must be inverted at each switching operation. Therefore, regarding the high dimension of the system and without an appropriate model according to this type of study, it is practically impossible to simulate, with accuracy, HVDC systems containing MMC converters on EMT-type

[*] Corresponding author: A. Zama, SuperGrid Institute SAS, 130 Leon Blum, BP 1321, 69611 Villeurbanne, France, E-mail: ahmedislam.zama@supergrid-institute.com

[1] SuperGrid Institute SAS, 130 Leon Blum, BP 1321, 69611 Villeurbanne, France.

2 Grenoble Alpes University - G2Elab, 38031 Grenoble, France.

simulation programs [6, 7]. To solve this issue, different models have been developed for studying the normal operation of MMC: Detailed model, Equivalent model and Averaged model [8, 9]. Another challenge of MMC modelling is to model the blocking state of SMs which is required to develop a protection strategies for HVDC system. The mathematical formulation has been already demonstrated but the proposed solution consists in switching between two circuit models (controlled and blocked) by using a numerical solution to achieve this transition between circuits. This paper presents an innovative solution for full order MMC type models: Detailed, Equivalent and Averaged based on a semi-analytical model for MMC arm in order to have the both states in the same model and accelerates the simulation. This contribution is based on an idea given by [10] applied to the reduced order averaged model of the MMC which is improved in this paper.

The outline of this article is as follows. In *Section 2*, the basic operating principles of MMC are presented. In *Section 3*, different MMC models are discussed. The Semi-Analytical model for reduced order model is introduced in *Section 4*. The proposed full order MMC models with associated semi-analytical equations are presented in *Section 5*. To compare between these MMC models, some simulations and results are proposed in *Section 6*.

2. MMC operation and principle

The topology of a typical three-phase half bridge MMC is shown in *Fig 1-(a)*, every leg of the converter has two arms; each one has *N* identical SMs connected in series. Each SM has two power switches (two IGBTs with anti-parallel diodes) and one capacitor *C* connected as shown in *Fig 1-(b)*. The SM can provide two different voltage levels, when S1 is ON and S2 is OFF. The SM provides voltage *Vc* when the capacitor can be charged or discharged depending on the current direction. When S2 is ON and S1 is OFF, the capacitor is bypassed by S2 and the SM has zero output voltage. In the blocked state: S1 and S2 are off, the capacitor may charge through S1 and cannot discharge.

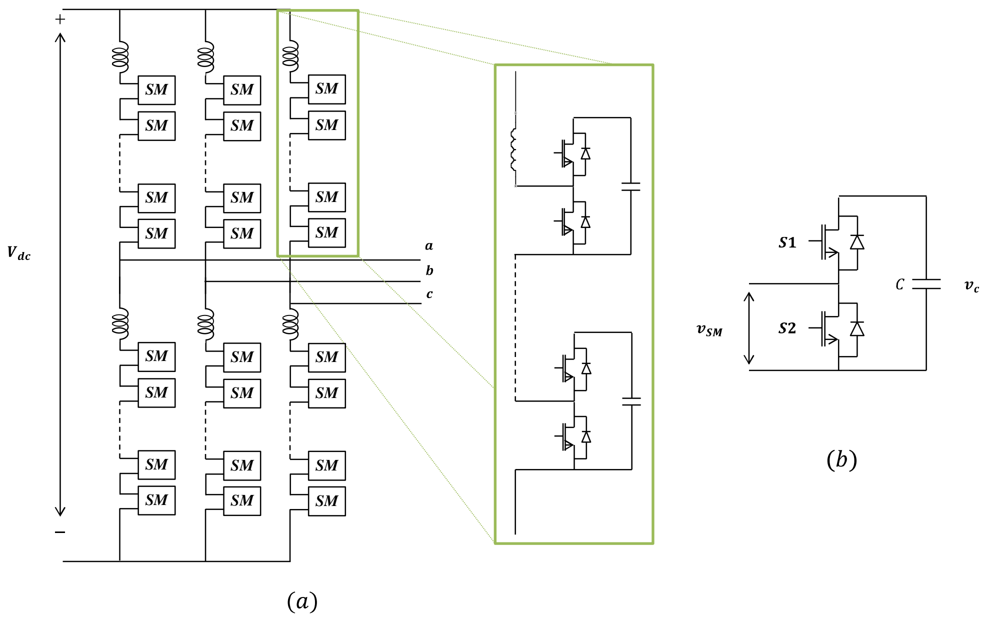

Fig. 1. (a) Three-phase half bridge MMC topology, (b) Half bridge submodule

$$N_U + N_L = N \quad (1)$$

Unlike a classical VSC, the MMC has a reactor in each arm. The converter reactors have two functions: Limitation of arm-current harmonics and fault currents. The applied modulation process is arranged to ensure the condition (1) of operation and to produce the desired (N+1) different levels for AC output voltage) where N_U and N_L are respectively upper and lower inserted SMs numbers.

3. MMC modeling

The main families of MMC models are represented by the full order detailed continuous model, the full order sampled model and the reduced order averaged one. For more details, all these models are well documented in [11].

3.1 Type 1: Full Order Detailed Model.

The knowledge based model is close to physical system, it is named usually as the detailed model or the topological one. The switches model is simplified to a resistance which has two values: R_{on} ON-state (mΩ) and R_{off} OFF-state (MΩ) (See *Fig.2-Type1*) [12]. For more accurate studies, for example study of current distributions and losses calculations, the switches models are completed by a nonlinear representation of IGBTs. For our considered purposes, stability analysis and protection algorithms, the model presented in *Fig. 1* is regarded as our Benchmark Model. The main drawback of this model (circuit based) is the needed computation time.

3.2 Type 2: Full Order Equivalent Model.

In order to decrease computational times, a new simplified model was proposed in [12]. This model can be achieved by reducing the number of electrical nodes in the converter representation and keeping the "same order" as the real structure. With the trapezoidal integration rule and by using Thevenin Equivalent Circuit, each submodule capacitor is replaced by an equivalent voltage history source $V_{c\_eq}(t - \Delta T)$ in series with an impedance $R_c = \frac{\Delta T}{2C}$ where ΔT is the numerical integral time-step (see *Fig. 2-Type2*). The associated simulation time is still long but less than the type 1. It is worth noting that this model is suitable for the design of low level controllers as well as average models validation.

3.3 Type 3: Reduced Order Averaged Model.

In this model, the whole set of SMs of one arm is reduced to an equivalent unique SM which is represented by an average equivalent voltage source. The main taken hypothesis is concerning the SMs capacitor voltage which is supposed to be perfect. Consequently, each MMC arm is reduced to equivalent boost-buck converter circuit (See *Fig. 2-Type3*) [*8*]. The main advantage of this reduced order average model is the calculation time for simulations; it is hundreds time faster than the full order models. Generally, it is used to design and tune high level control when phenomena at the time scale of low level control are neglected. The main drawback is that all SMs have to be treated as a single unit in the model.

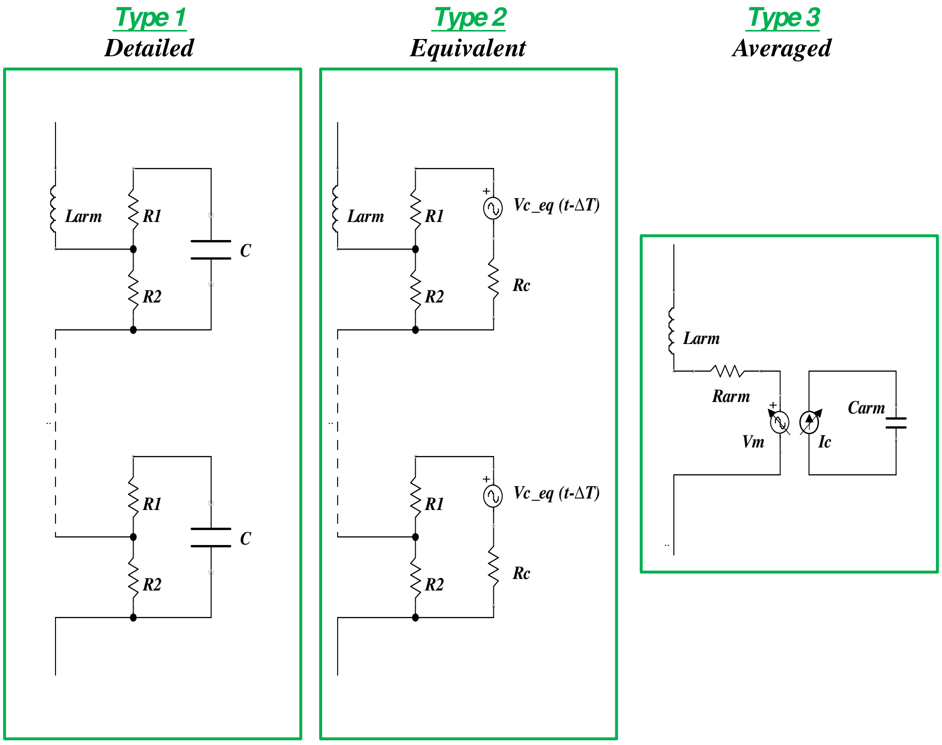

Fig. 2. Different MMC arm models presented in literature: Type1, Type 2 and Type 3

4. Semi-Analytical MMC models

The semi-analytical MMC models are obtained by simplifying each arm of the converter to: two controlled voltage sources, two diodes, an inductance and a resistor connected as shown in *Fig. 3.* L_{arm} Inductance is the equivalent arm inductance and the resistor R_{arm} is used to model the losses in the arm. The voltage sources are controlled by a bloc which contains the equations. The inputs and outputs of this bloc changes according to the type of MMC models presented in previous section. The controlled source v_{m_c} represents the controlled state when the IGBTs are controlled and the controlled source the v_{m_b} represents the blocked state when the IGBTs are blocked.

This modelling technique is already developed for the reduced order averaged model presented in [10]. In this type of model, instead of having a gate signals for SM, a new parameter is introduced called modulation m index which represents the ratio between the number of inserted SM and the total number of SM (N). Since all SMs are treated as a single unit (reduced order model), the blocked signals of SMs become a common signal to block all the arm. The semi-analytical model can be written as follows:

$$
\begin{gathered}
i_{c_{arm}} = m\, i_{arm}(1 - u_{bloc}) + i_c u_{bloc} \\
v_{c_{arm}} = \int \frac{i_{c_{arm}}}{C_{arm}} \qquad with \qquad C_{arm} = \frac{C}{N} \\
v_{m_c} = m\, v_{c_{arm}}(1 - u_{bloc}) \\
v_{m_b} = v_{c_{arm}} u_{bloc}
\end{gathered}
\tag{2}
$$

Blocking all SMs arm can be regarded as a drawback since in the full order models there is the possibility to bloc some SMs and keep others in the controlled state. The first contribution of the proposed work is to improve the averaged model by adding this function to the reduced order averaged model presented in [10]. To do this, a new parameter n which represents the ratio between the number of blocked SM and the total number of SM (N). The semi-analytical model can be written as follows:

$$
\begin{aligned}
i_{c_{arm}} &= m\, i_{arm} + n\, i_c && when \quad m+n \le N \\
i_{c_{arm}} &= (1-n)\, i_{arm} + n\, i_c && when \quad m+n > N \\
v_{c_{arm}} &= \int \frac{i_{c_{arm}}}{C_{arm}} && with \quad C_{arm} = \frac{C}{N} \\
v_{m_c} &= m\, v_{c_{arm}} && when \quad m+n \le N \\
v_{m_c} &= (1-n)\, v_{c_{arm}} && when \quad m+n > N \\
v_{m_b} &= n\, v_{c_{arm}}
\end{aligned}
\tag{3}
$$

The second contribution is to extend this modelling technique to the ***Detailed and Equivalent full order MMC models***. This contribution leads to accelerate the simulation time and to provide a unique model for controlled and blocked states instead of the solution proposed in [8] which consists in switching between controlled and blocked models.

5. Proposed full order MMC models

5.1 Type 1: Full Order Detailed Model.

The inputs of semi-analytical model are: Gate u_g signals (1 to insert and 0 to u_b bypass the SMs), Blocked signals (1 to block and 0 to control the SMs), i_{arm} i_c Arm current and Capacitor current.

The outputs are: SM voltages $v_{c_{sm}}$, Equivalent arm $v_{c_{arm}}$ voltage and Modulated arm v_{m_c} voltages: for controlled v_{m_b} state and for blocked state. For N+1 MMC levels (N SM per arm), the semi-analytical model is given by:

$$for\ i = 1,2,3 \ldots, N$$

$$
\begin{aligned}
v_{c_{sm_i}} &= \int \frac{1}{C}\left[i_{arm} u_{g_i}\left(1-u_{bloc_i}\right) + i_c u_{bloc_i}\right] \\
v_{c_{arm}} &= \sum_{i=1}^{N} V_{c_{sm_i}} \\
v_{m_c} &= \sum_{i=1}^{N} V_{c_{sm_i}} u_{g_i}\left(1-u_{bloc_i}\right) \\
v_{m_b} &= \sum_{i=1}^{N} V_{c_{sm_i}} u_{bloc_i}
\end{aligned}
\tag{4}
$$

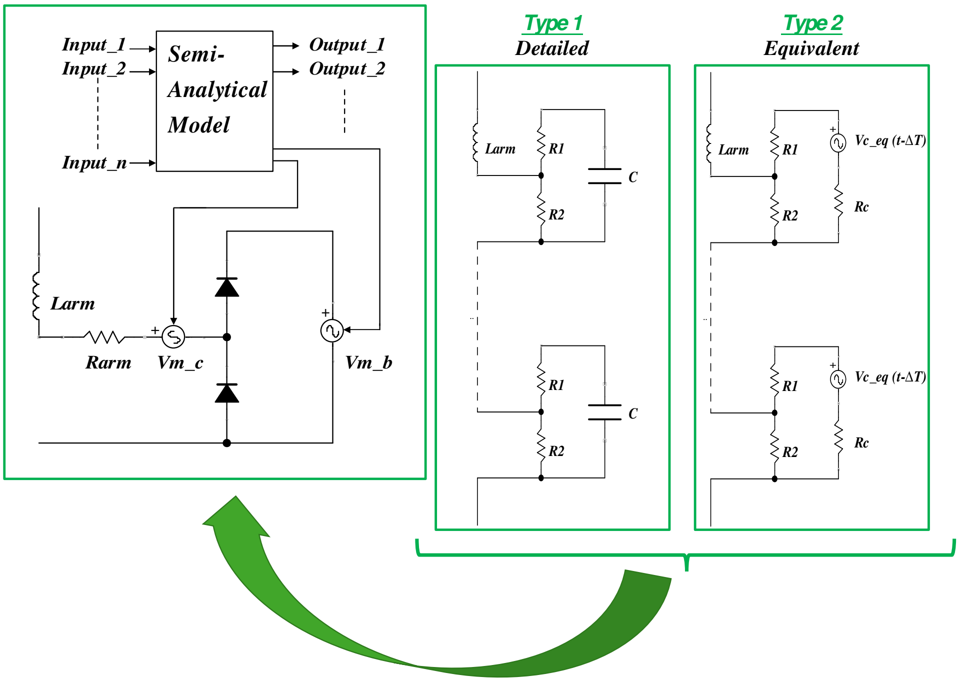

Fig. 3. Proposed MMC model for full order MMC types

5.1 Type 2: Full Order Equivalent Model.

As explained in section 2, the variation of the SM capacitor voltages is given by the trapezoidal integration rule and Thevenin Equivalent Circuit. The semi-analytical can be written as it follows:

$$
\begin{gathered}
For\ i = 1,2,3\ldots,N \\
R_{1_i} = [R_{on}\,u_{g_i} + R_{off}(1-u_{g_i})](1-u_{bloc_i}) \\
R_{2_i} = [R_{off}\,u_{g_i} + R_{on}(1-u_{g_i})](1-u_{bloc_i}) \\
i_{c_{sm_i}} = i_{arm}u_{g_i}(1-u_{bloc_i}) + i_c u_{bloc_i} \\
V_{c\_eq_i}(t) = R_c i_{c_{sm_i}} + V_{c\_eq_i}(t-\Delta T) \quad with \\
R_c = \frac{\Delta T}{2C} \\
R_{theq_i} = \frac{R_{2_i} * (R_{1_i} + R_c)}{R_{2_i} + R_{1_i} + R_c} \\
v_{theq_i}(t) = V_{c\_eq_i}(t)\frac{R_{2_i}}{R_{2_i} + R_{1_i} + R_c} \\
v_{c_{arm}} = \sum_{i=1}^{N} V_{c_{sm_i}} \\
v_{m_c} = \sum_{i=1}^{N}\left(R_{theq_i} i_{arm} + v_{theq_i}\right)(1-u_{bloc_i}) \\
v_{m_b} = \sum_{i=1}^{N} V_{c_{sm_i}} u_{bloc_i}
\end{gathered}
\tag{5}
$$

In contrast to the detailed model, the semi-analytical model needs more inputs: Time Step ΔT and $V_{c\_eq}(t-\Delta T)$ the previous SM voltages. For the outputs, they are same as the detailed model since both are full order models.

6. Models validation

To validate the proposed MMC models, some simulations with test cases are carried out in Matlab-Simulink. The proposed models are compared with the *Benchmark model* (Detailed MMC based on circuit models). A point to point HVDC connection based on MMC is used to perform this comparison. Two symmetric monopolar MMCs are connected via a DC cables as shown in *Fig. 4*. To simplify the study, a simple *PI* model is used for cables. The used parameters for simulations are presented in *Table 1*. To ensure grid stability and power transfer between the stations, one station has to be controlled in active power control mode and the second one has to be controlled in DC voltage control mode. The used control for the stations is presented [13].

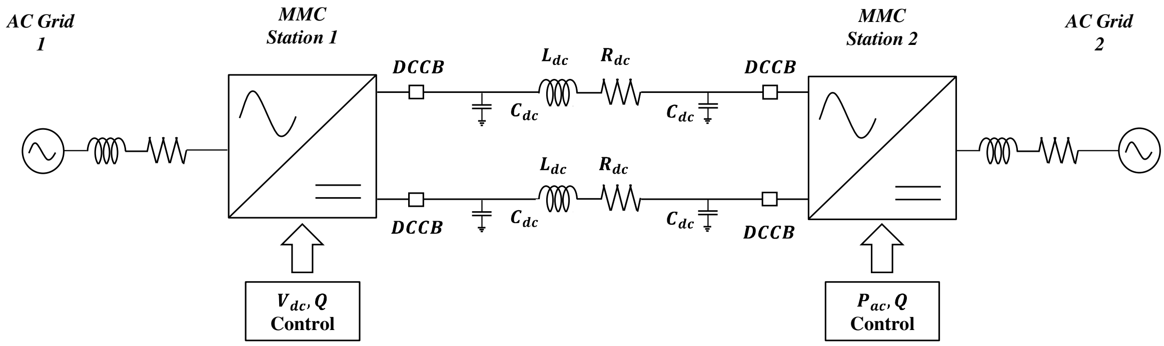

Fig. 4. Simulation circuit

Table 1: Simulation Parameters

Nominal power (MW)	*1000*	Resistance of the grid reactor [p.u]	*0.005*
AC nominal voltage (kV)	*320*	Arm resistance [p.u]	*0.01*
DC nominal voltage (kV)	*640*	Arm inductance [p.u]	*0.15*
Number of SM	*400*	Electrostatic Constant [p.u]	*0.04*
Inductance of the grid reactor [p.u]	*0.18*	Capacitor Cable [μF]	*48.4*

6.1 Test case for normal operation.

A step change in active power reference at 0.1[s] for MMC station 2 and reactive power reference at 0.3[s] for MMC station 1 are simulated. The results (Active and reactive powers for station 1) are presented in *Fig. 5*. They show the validity of all models. The variation of active and reactive power is the same for all models in steady state as well as in transients.

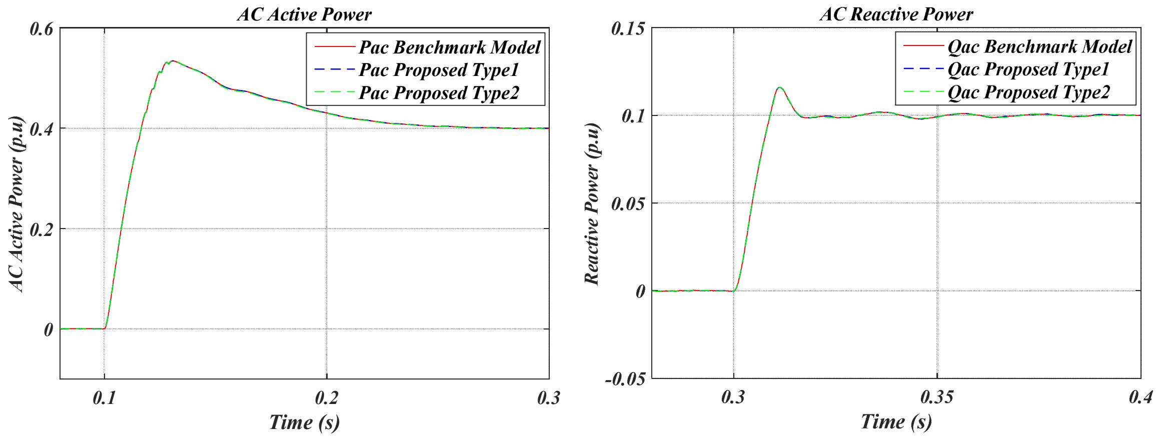

Fig. 5. MMC 1: Active power variation (Left), Reactive power variation (Right)

As demonstrated in [14], the distributed capacitors in MMC can behave as an additional energy storage if it is appropriately controlled. This property allows to change arm energy levels during MMC operation. This degree of freedom is tested with the proposed models for MMC 1.

For this, a step change in energy sum (sum of upper and low arm energies) and energy difference (difference between low and upper arm energies) references at 0.5[s] and 0.7[s] are tested. The arm energies for phase 1 are duplicated in *Fig. 6*. The results show the accuracy and validity of all models.

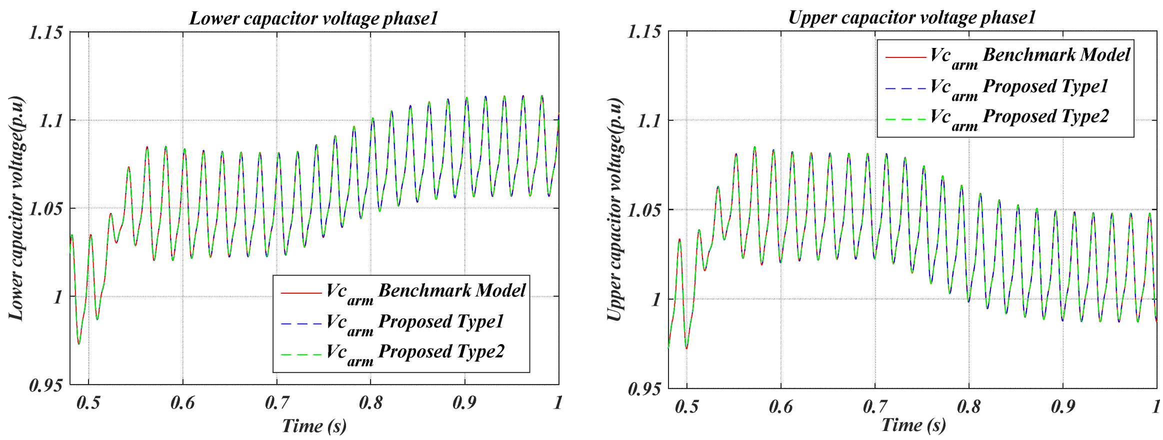

Fig. 6. MMC 1: Lower capacitor voltages (Left), Upper capacitor voltages (Right)

6.2 Test case in fault conditions.

To check the blocking state of MMC, the following test case is carried out. A pole to pole DC fault is applied at 0.1[s]. The MMC control is equipped with a protection controller to block the MMC when a fault is detected. The controller measures the arm currents instantly and if one of the currents exceeds *2 p.u*, it sends instantaneously a blocking signal to block the arm.

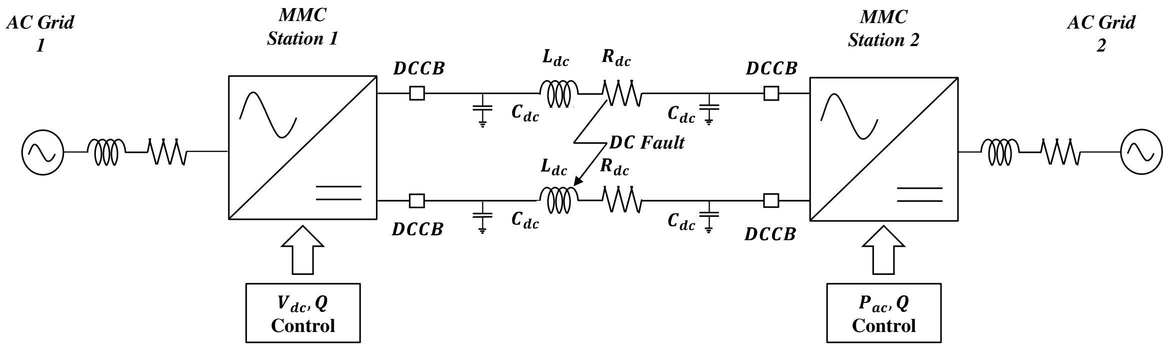

Fig. 7. Simulation circuit for fault condition

From the results presented in *Fig. 8*, it can be noticed that the blocking state is well represented by the proposed models. Just after the fault, when the current exceeds *2 p.u*, the protection controller blocks the converter and the MMC becomes a diode bridge converter. These results can be confirmed by the variation of upper capacitor voltage *Fig. 9*.

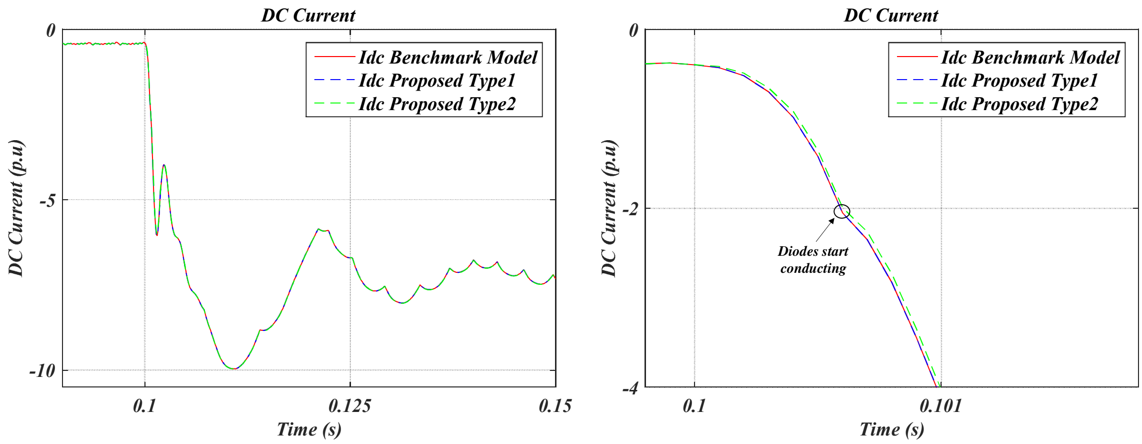

Fig. 8. DC current variation in MMC 1 (Left), Zoom on DC current fault (Right)

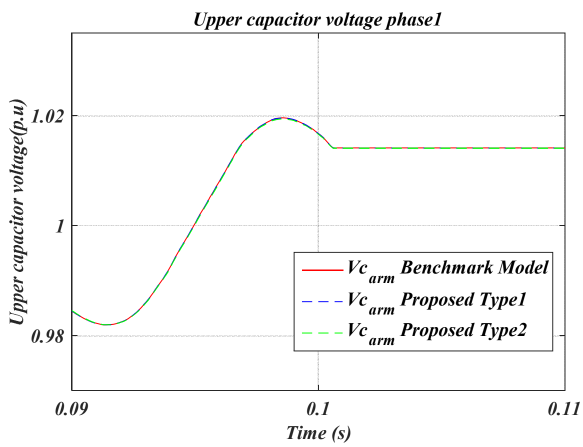

Fig. 8. Upper capacitor voltages in MMC 1 for DC fault condition

The simulation time for MMC models with different MMC levels is presented in *Table 2*. The simulations were performed on a computer with a 3.5 GHz Intel Core XeonE5-1650V3 processor. As we can see, even with 400 SM, the simulation time is 20 time faster than to the benchmark model. It is more accelerated with proposed type 2 since it contains less state variables. These results show that by using the proposed models, it will be possible to simulate, with accuracy, HVDC systems containing MMC converters on EMT-type simulation programs.

Table 3: Simulation time of MMC models for 1 s effective time

	Benchmark model	*Proposed Type 1*	*Proposed Type 2*
400 SMs MMC	*2100 s*	*87 s*	*60 s*
100 SMs MMC	*308 s*	*41 s*	*37 s*
50 SMs MMC	*183 s*	*35 s*	*32 s*

7. Conclusions

A novel full order MMC models have been proposed based on semi-analytical arm models. The accuracy of proposed models has been tested in off-line simulation environment. The results show the validity of all models in normal operations as well as for blocking state when diodes are conducting.

The proposed work leads to accelerate the simulation time and to have a unique model for controlled and blocked states instead of the previous solution. This advantage will facilitate the integration of MMC in HVDC systems in order to develop a protection algorithms or/and the stability analysis for such systems. The next step of this work will be to test these models in real time simulation environment.

References

[1] M. Petit, S. Bacha, X. Guillaud, H. Morel, D. Planson & B. Raison, Les réseaux HVDC multi-terminaux: des défis multiples en génie électrique, *Symposium de Génie Électrique,* July 2014.

[2] B. R. Andersen, L. Xu, P. J. Horton, & P. Cartwright, Topologies for VSC transmission, *Power Engineering Journal,* 16(3), 142-150, 2002.

[3] J. Dong, & P. Chen, Reliability Evaluation of Multi-terminals VSC-HVDC System, *Journal of Electrical Systems*, 11(3), 342-352, 2015.

[4] G. Agnihotri, Sonali Dasgupta, *Journal of Electrical Systems*, 7(3), 332-342, 2011.

[5] A. Lesnicar & R. Marquardt, An innovative modular multilevel converter topology suitable for a wide power range, *Power Tech Conference Proceedings*, Vol. 3, 2003.

[6] S.A. Zidi, S. Hadjeri, & M.k. Fellah, Regular paper Dynamic Performance of an HVDC Link, *Journal of Electrical Systems*, 1.3, 15-23, 2005.

[7] U. N. Gnanarathna, A. M. Gole, & R. P. Jayasinghe, Efficient modeling of modular multilevel HVDC converters (MMC) on electromagnetic transient simulation programs, *IEEE Transactions on Power Delivery*, 26(1), 316-324, 2011.

[8] H. Saad, S. Dennetière, J. Mahseredjian, P. Delarue, X. Guillaud, J. Peralta & S. Nguefeu, Modular multilevel converter models for electromagnetic transients, *IEEE Transactions on Power Delivery*, 29(3), 1481-1489, 2014.

[9] A. Zama, A Review of Modular Multi-Level Converter (MMC) Modeling for HVDC Application, *Journées des Jeunes chercheurs en Génie Electrique,* July, 2015.

[10] S. Dennetiere, H. Saad, B. Clerc, E. Ghahremani, W. Li, & J. Belanger, Validation of a MMC model in a real-time simulation platform for industrial HIL tests, *IEEE Power & Energy Society General Meeting,* pp. 1-5, July, 2015.

[11] S. Bacha, I. Munteanu & A. I. Bratcu, Power Electronic Converters Modeling and Control with case studies, *Springer*, 2013.

[12] H. Saad, J. Peralta, S. Dennetiere, J. Mahseredjian, , Jatskevich, J. A. Martinez, & A. Mehrizi-Sani, Dynamic averaged and simplified models for MMC-based HVDC transmission systems, *IEEE Transactions on Power Delivery,* 28(3), 1723-1730, 2013.

[13] G. Bergna, A. Garces, E. Berne, P. Egrot, A. Arzandé, J. C. Vannier & M. Molinas, A generalized power control approach in abc frame for modular multilevel converter hvdc links based on mathematical optimization, *IEEE Transactions on Power Delivery*, 29(1), 386-394, 2014.

[14] H. Saad, X. Guillaud, J. Mahseredjian, S. Dennetiere & S. Nguefeu, MMC Capacitor Voltage Decoupling and Balancing Controls, *IEEE Transactions on Power Delivery*, 30(2), 704-712, 2015.