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A Study of a New Methodology for 2-Type 3-Order Charge Pump PLLs

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We proposed a new methodology for 2-type 3-order Charge Pump-PLLs (CP-PLLs) utilizing loop gain optimization, for which PLL operation are divided into 2-modes, pull-in and lock modes. We derived a set of equations which ensure the stability of the PLLs by avoiding instability problem accompanied by charging the loop states in pull-in mode. The simulation results using MATLAB shows significant stability of a prototype PLL and verifies the great usefulness of the proposed method.

Keywords: PLLs, data communication, mobile receivers.

1. INTRODUCTION

Phase-Locked Loops (PLLs) have been widely used in high-speed data communication systems such as digital mobile receivers, Ethenet receivers, high-speed memory interfaces, and so on. This is because PLLs efficiently perform clock recovery and clock generation with relatively low cost. PLLs integrated in the systems above require both "fast catch-up before lock" and "low-jitter operation after lock" simultaneously. The fast catch-up together with low-jitter is particularly difficult to be realized because the increase in loop stability for low jitter degrades the lock time.

Conventional analog PLLs in clock recovery applications adopt a narrow-band loop filter to reduce output jitter at the cost of elongated locking time. In order to improve the locking-time characteristics, digital or hybrid analog/digital PLLs with digital swap loop-gain characteristics had been proposed [1-3]. Since complex digital building blocks are implemented in these PLLs, they usually suffer from high power dissipation, low operation speed and large die size. To address these issues, PLLs with simpler algorithms were presented [4-6]. On the other hand, we proposed a high speed switched-capacitor analog correlator with balanced charge pump circuit for wired CDMA bus interface [7,8].

In this paper, we attempt to design PLLs with analog control circuit. We describe a theory of a dynamic loop gain control method in pull-in mode where continuously charging loop states exist and their stable operation is guaranteed. Based on the theoretical approach we derived an equation which ensures the stability of the proposed CP (Charge Pump)-PLLs.

This paper consists of eight sections including the present section. Section 2 describes the proposed CP-PLL architecture and its operation. The way to optimize the loop gain is reffered in Section 3. Loop gain optimization theories regarding in both lock and pull-in modes are given in Section 4 and 5 respectively. Basic equations to design a proposed CP-PLL are drawn in Section 6. Section 7 shows the simulation result by MATLAB. Finally, conclusion are given in Section 8.

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2. PROPOSED CP-PLL

Ablock diagram of the prposed CP-PLL is shown in Fig. 1.

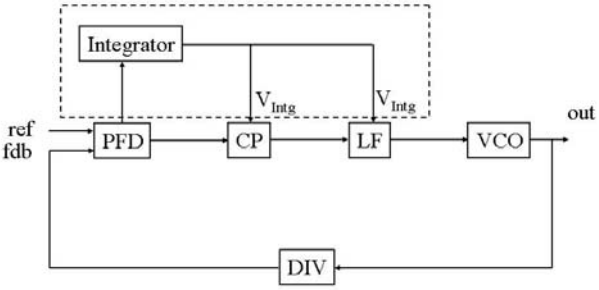

Fig. 1 Block diagram of the proposed CP-PLL

The proposed PLL consists of a normal CP(charge pump)-PLL and integrator which is enclosed with the broken line in Fig. 1. The role of the integrator is described next. During pull-in mode the integrator becomes active and generates the control voltage, V_{Intg}, while during lock mode, the integrator becomes inactive and V_{Intg} keeps low state. Both CP and LF are controlled with V_{Intg}. The operation of the proposed CP-PLL is as follows:

- Lock mode : operating as a conventional CP-PLL without the integrator
- Pull-in mode : operating as a proposed CP-PLL with the integrator

3. LOOP GAIN OPTIMIZING METHOD

The CP-PLL loop gain $G_{loop}(s)$ is given by [9],

$$G_{loop}(s) = \frac{I_{CP} K_{VCO}}{sN} F(s) \quad (1)$$

where I_{CP} is CP current, F(s) is the LF transfer function, K_{VCO} is the gain of the VCO, N is the frequency-multiplication number. The loop filter shown in Fig. 2 is used for the 2-type 3-order CP-PLL.

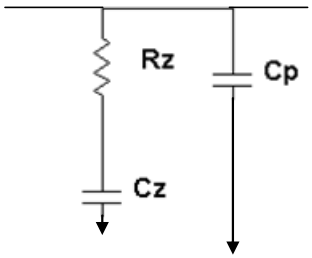

Fig. 2 Conventional low pass filter for PLL

The transfer function of this loop filter is given by

$$F(s) = \frac{1 + s\tau_z}{s\alpha_g\left(1 + s\tau_p\right)} F(s) \tag{2}$$

where,

$$\alpha_g = C_p + C_z,\ \tau_p = \frac{C_p C_z}{C_p + C_z} R_z,\ \tau_z = C_z R_z \tag{3}$$

Three parameters of the loop filter, α_g, τ_p, and τ_z, play an important role to optimize the system loop gain. Substituting Eq. (2) into Eq. (1), the loop gain, $G_{loop}(s)$ is given by

$$G_{loop}(s) = \frac{K(1 + s\tau_z)}{s^2\alpha_g(1 + s\tau_p)} F(s) \tag{4}$$

where

$$K = \frac{I_{CP} K_{VCO}}{N}$$

Figure 3 shows an optimized bode diagram of the 2-type 3-order CP-PLL.

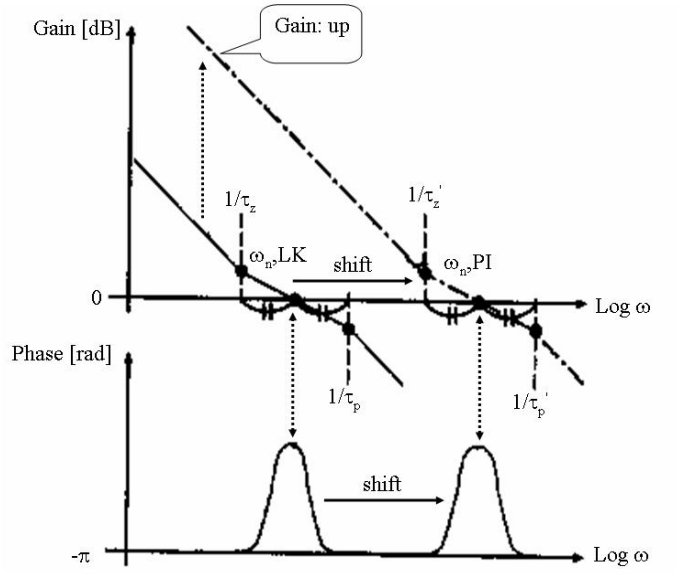

Fig. 3 Schematic illustration of the loop gain optimization

The solid lines in the figure illustrate the optimized loop gain characteristics in lock mode. During pull-in mode, however, I_{CP} and F(s) are dynamically changed whose roles are :

- I_{CP} : shifts the characteristics line towards higher gain region, that is, moves the loop natural frequency, ω_n, to higher frequency.

- F(s) : shifts the zero ($1/\tau_z$) and pole ($1/\tau_p$) of the loop gain towards higher frequency, that is, moves the phase characteristics line to higher frequency.

Figure 3 illustrates how the zero and pole together with natural frequency should be shifted based on the proposed method described above.

During pull-in mode a sufficient phase margin is necessary for the system stability. This can be realized with the system in which ω_n always stays in the frequency where the loop gain phase margin is maximum. Slight difference between ω_n and the frequency with the maximum phase margin gives rise to a sudden degradation in phase margin. This is because the maximum phase margin below 90 degree is inevitable due to their system structure and the side slopes of the loop gain phase charactesistics are quite steep. Based on the theoritical study of the system, ω_n shifting toward higher frequency region should precisely follow the shift of the loop gain phase, otherwise the system soon loses stability and becomes unstable, as shown in Fig. 4. So, it should be noted that carful design of the loop gain is important particularly during pull-in mode.

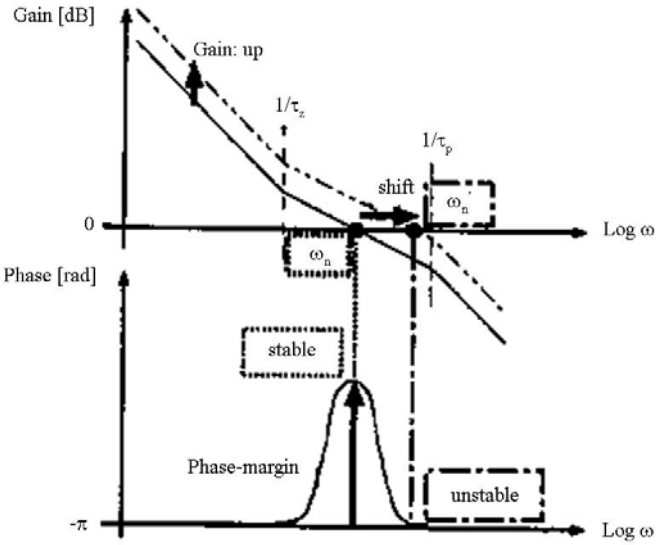

Fig. 4 Bode diagram of conventional 2-type 3-order CP-PLLs

4. LOOP GAIN OPTIMIZATION AT LOCK MODE

The frequency-domain characteristics of the loop gain is given by,

$$G_{loop}(\omega) = \frac{K}{j\omega} \frac{1 + j\omega\tau_z}{j\omega\alpha_g(1 + j\omega\tau_p)} \tag{5}$$

This gives a phase characteristics of [10]

$$\angle G_{loop}(\omega) = -\pi + \arctan\frac{\omega(\tau_z - \tau_p)}{1 + \omega^2\tau_z\tau_p} \tag{6}$$

The frequency providing maximum phase margin of $G_{loop}(\omega)$ can be derived from the following condition.

$$\frac{d}{d\omega}\arctan\frac{\omega(\tau_z-\tau_p)}{1+\omega^2\tau_z\tau_p}=0 \tag{7}$$

So, the phase margin becomes maximum at the frequency given by

$$\omega_n^2=\frac{1}{\tau_z\tau_p} \tag{8}$$

This is indicates that the loop nature frequency ω_n is the geometric mean of $1/\tau_z$ and $1/\tau_p$, as shown in Fig. 5.

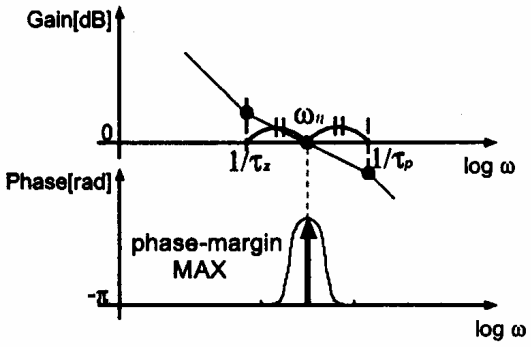

Fig. 5 Optimized loop gain and phase margin

In this optimized condition phase margin is given by

$$\phi_m=\arctan\frac{\omega(\tau_z-\tau_p)}{1+\omega^2\tau_z\tau_p}=\arctan\frac{C_z-\dfrac{C_pC_z}{C_p+C_z}}{\sqrt{C_z\dfrac{C_pC_z}{C_p+C_z}}} \tag{9}$$

For the derivation shown above, we used $\phi_m=\pi+\angle G_{loop}(\omega_n)$.

$|\ G_{loop}(\omega_n)|\ =1$ must be satisfied at the loop natural frequency, which leads to

$$\alpha_g=\frac{K}{\omega_n^2}(\tan\phi_m+\sec\phi_m) \tag{10}$$

The physical meanings of the loap gain parameters are as follows:

- τ_z, τ_p provide a desired phase margin.
- α_g controls the gain.

5. LOOP GAIN OPTIMIZATION AT PULL-IN MODE

The LF transfer function F(s) should be continuously changed, resulting in the shift of their pole ($1/\tau_p$) and zero ($1/\tau_z$), so that the phase of the loop gain can be suitable controlled. Figure 6 shows a proposed LF which meets this requirement.

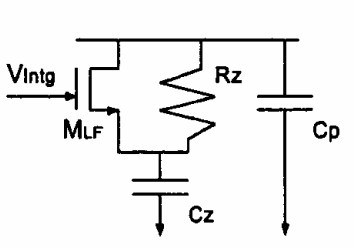

Fig. 6 Low pass filter for the proposed PLL

During lock mode a MOS (M_{LF}) is switched off so it acts as a conventional LF shown in Fig. 2, whereas during pull-in mode the integrator activates M_{LF} with V_{Intg}. The total resisitance, R_{var}, of R_z and M_{LF} connected in parallel varies according to the V_{ctrl}, so both $1/\tau_p$ and $1/\tau_z$ are shifted towards higher frequency. Based on small signal analysis, R_{var} is given by

$$R_{\text{var}} = \frac{R_z}{1+\beta_{LF}(V_{Intg}-V_{TH})R_z} \cong \frac{R_z}{\beta_{LF}(V_{Intg}-V_{TH})R_z} \tag{11}$$

where β_{LF} is the process transconductance of M_{LF} and V_{TH} is the threshold voltage of M_{LF}.

Three LF parameters during pull-in mode, , α_g', τ_p', and τ_z', are given by

$$\alpha_g^{'} = C_p + C_z = \alpha_g$$

$$\tau_p^{'} = \frac{C_p C_z}{C_p + C_z} R_{\text{var}} = \frac{C_p C_z}{C_p + C_z} \frac{R_z}{\beta_{LF}(V_{Intg}-V_{TH})R_z}$$

$$\tau_z^{'} = C_z R_{\text{var}} = C_z \frac{R_z}{\beta_{LF}(V_{Intg}-V_{TH})R_z}$$

Higher integrator output voltage V_{Intg} shifts the loop zero ($1/\tau_z'$) and pole ($1/\tau_p'$), in parrallel, towards higher frequency on the bode diagram, which should be kept in mind.

Now $\phi_{m,\,PI}$ means phase margin during pull-in mode and $\phi_{m,\,LK}$ represents phase margin during lock mode. For given capacitances, C_z and C_p, the following relationship can be drawn from Eq. (9).

$$\phi_{m,PI} = \phi_{m,LK} \tag{12}$$

This indicates that the maximum phase margin stays unchanged regardless of the loop states, such as lock or pull-in modes.

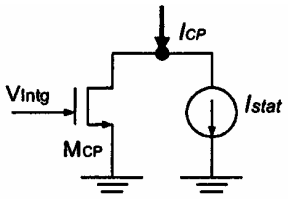

Fig. 7 Basic illustration of the proposed CP

Figure 7 shows a basic concept of the proposed CP. During lock mode constant current I_{stat} is pulled from the CP, while during pull-in mode both I_{stat} and current through an MOS (M_{CP}) driven by the output of the integrator, V_{Intg}, are drawn.

- lock mode : $I_{CP} = I_{stat}$
- pull-in mode $I_{CP} = I_{stat} + \beta_{CP}(V_{Intg} - V_{TH})^2$

where β_{CP} is the process transconductance of M_{CP}.

Optimization of the loop gain characteristics during pull-in mode can be carried out by using the gain-optimizing parameters, α_g and α_g'.

lock mode $\alpha_g = \frac{K_{LK}}{\omega_{n,LK}^2}(\tan\phi_{m,LK} + \sec\phi_{m,LK})$

pull - in mode $\alpha_g^{'} = \frac{K_{PI}}{\omega_{n,PI}^2}(\tan\phi_{m,PI} + \sec\phi_{m,PI})$

Using $\alpha_g = \alpha_g^{'}$ and $\phi_{m,PI} = \phi_{m,LK}$ we derived

$$\frac{\omega_{\mathrm{n,PI}}^2}{\omega_{\mathrm{n,LK}}^2} = \frac{K_{PI}}{K_{LK}} \tag{13}$$

6. BASIC EQUATIONS FOR PLL DESIGN

Equation for Loop Stability The useful equations for the system stability can be derived from Eq. (13). The loop natural frequency ω_n is given by

$$\frac{\omega_{\mathrm{n,PI}}^2}{\omega_{\mathrm{n,LK}}^2} = \frac{\dfrac{1}{\tau_z^{'}\tau_p^{'}}}{\dfrac{1}{\tau_z\tau_p}} = \{1 + \beta_{\mathrm{LF}}\mathrm{R_z}(\mathrm{V_{Intg}}\text{-}\mathrm{V_{TH}})\}^2 \tag{14}$$

The gain K is derived as

$$\frac{K_{\mathrm{PI}}}{K_{\mathrm{LK}}} = \frac{I_{CP,PI}}{I_{CP,LK}} = 1 + \frac{\beta_{\mathrm{CP}}(\mathrm{V_{Intg}}\text{-}\mathrm{V_{TH}})^2}{\mathrm{I_{stat}}} \tag{15}$$

Substituting Eq. (14) and Eq. (15) into Eq. (13), an extremely important equation to ensure the loop stability of the proposed CP-PLL is derived.

$$\beta_{CP} = \beta_{LF}^2 R_z^2 I_{stat} \tag{16}$$

Equation about Phase-Margin In this section the relationship between the desired phase margin ϕ_m and the ratio of capacitance size C_z/C_p is clarified.

Eliminating τ_p in two expressions, Eq. (8) and Eq. (9), gives a quadratic in τ_z,

$$\tau_z^2 - 2\frac{\tan\phi_m}{\omega_n}\tau_z - \frac{1}{\omega^2} = 0 \tag{17}$$

$$\tau_z = \frac{(\tan\phi_{\mathrm{m}} + \sec\phi_m)}{\omega_{\mathrm{n}}} = \frac{\Phi}{\omega_{\mathrm{n}}} \tag{18}$$

Where $\Phi = \tan\phi_{\mathrm{m}} + \sec\phi_m$. since $\tau_{\mathrm{p2}} = \frac{1}{\omega_n^2\tau_z}$

Then

$$\tau_{\mathrm{p}} = \frac{1}{\omega_n(\tan\phi_{\mathrm{m}} + \sec\phi_m)} = \frac{1}{\omega_n \Phi} \tag{19}$$

Eliminating ω_n in two equations, Eq. (18) and (19)

$$\frac{\tau_{\mathrm{p}}}{\tau_{\mathrm{z}}} = \Phi^2 \tag{20}$$

now using Eq. (3) and Eq. (4) gives us

$$\frac{\tau_{\mathrm{p}}}{\tau_{\mathrm{z}}} = \frac{C_p}{C_p + C_z} \tag{21}$$

with the solution

$$\Phi^2 = \frac{C_p}{C_p + C_z} \tag{22}$$

The equation below is carried out, by solving Eq. (20) and Eq. (21).

From Eq. (22) the relationship between ϕ_m and C_z/C_p is obtained as shown in Table 1.

Table 1 Relation between ϕ_m and C_z/C_p

ϕ_m[deg]	**C_z/C_p**
40	3.60
50	6.55
60	12.9
65	19.3
70	31.2
75	56.7

To design the proposed CP-PLL with desired phase margin Table 1 is quite helpful.

7. SIMULATION RESULTS

The proposed CP-PLL is simulated with MATLAB, in which Eq. (16) is hold among the physical parameters used. Table 2 shows the simulation results.

Table 2 Simulation results based on MATLAB

V_{Intg}[V]	below V_{TH}	1.5	2.0	3.0
ϕ_m[deg]	70	67	68	68
ω_n[rad/sec]	9.5×10^5	8.6×10^6	1.8×10^7	3.6×10^7

We used the following parameters:

$C_z = 100pF, \quad C_p = 3.2pF, \quad R_z = 60k\Omega,$

$K_{VCO} = 32MHz/V, \quad I_{stat} = 8.1\mu A, \quad N = 16,$

$\beta_{CP} = 500\mu A/V^2, \quad \beta_{LF} = 4500\mu A/V^2$

8. CONCLUSIONS

We proposed a new methodology for 2-type 3-order Charge Pump-PLLs (CP-PLLs) utilizing loop gain optimization, for which PLL operation are divided into 2-modes, pull-in and lock modes. From the theoretical study, we drived Eq. (16) which ensures the optimized stable operation of the CP-PLL. The MATLAB simulation results clearly reveal that the CP-PLL remains stable even in pull-in mode where the loop gain dynamically varies.

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