Reconfigurable ANPC converter PWM strategy for an improved junction temperature distribution

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***Abstract*— The three level Active Neutral Point Clamped (3L-ANPC) topology has been proposed to overcome the three level Neutral Point Clamped (3L-NPC) topology's main structural drawback of unequal loss distribution and the resulting asymmetrical junction temperature distribution among its power switches. According to several research works, this unbalanced distribution of losses and heat inside the converter can be reduced by using the appropriate control technique. Taking benefit of the conventional PWM strategies advantages, this paper proposes a reconfigurable carrier-based PWM control strategy for the 3L-ANPC converter. The proposed modulation technique aims to improve the thermal stress unbalance inside the converter and to reduce the converter total losses compared to existing ones. The effectiveness of the proposed algorithm is proved by PSIM simulation tests with a 60 kW 3L-ANPC converter.**

***Index Terms*-- NPC topology, ANPC topology, PWM strategy, power loss, junction temperature.**

1. INTRODUCTION

During last decades, multilevel converters provided compelling solutions to operate at high power rates thanks to original semiconductors switch and passive component connection ways [1], [2], [3]. Compared to conventional two level converters, the multilevel structures present the advantages of lower harmonic distortion, lower device voltage rating and higher efficiency [4], [5]. Numerous multilevel topologies have been proposed, and abundant modulation techniques and control have been developed in recent literature [6], [7], [8]... Some of these topologies have been introduced in industrial applications thanks to their inherent advantages, such as, the Cascaded H-Bridge (CHB) which was used in many possible instances for the broadcasting amplifier, industrial drive, and STATCOM applications… [9], [10], [11], the Flying Capacitor (FC) topology which is attractive for some applications such as high speed drives and test benches [11], [12], and the Modular Multilevel Converter (MMC) which is suitable for the applications in High Voltage Direct Current (HVDC) and STATCOM [13].

Among these multilevel topologies, the 3L-NPC is the most popular and most used in the field of high power medium/high voltage industrial applications [14], [15]. However, this topology presents some issues that attracted much research and development attention. For instance, the DC link capacitor voltage unbalance, that can be easily solved by using a dedicated Space Vector Pulse Width Modulation (SVPWM) as reported in [15]. Also, Adding clamp diode in series can efficiently reduce the unequal voltages they support when p is greater than 3, where p is the converter voltage level.

The 3L-NPC major drawback is the uneven distribution of power loss among its different power switches, which naturally leads to an unequal junction temperature distribution. This drawback limits the switching frequency and the maximum achievable power and reduces sensitively the converter dynamic performances, lifetime, and reliability [2], [15]. In 2001, the 3L-ANPC topology, a developed version of the 3L-NPC one, was introduced to overcome the issue of power loss and junction temperature unbalances inside the converter [15]. The main circuits of the 3L-NPC and 3L-ANPC converters are depicted in Fig. 1. The ANPC topology is a derivative of the NPC one where the clamp diodes of this later are substituted by bidirectional switches. Hence, the 3L-ANPC topology presents additional degrees of freedom, i.e. additional zero states and commutations can be achieved. These additional active switches allow a particular utilisation of both the upper and lower path of the neutral point regardless the output current direction. Based on the fact that the commutation from or to the zero states can determine the switching losses distribution, and the selection of the conduction paths can determine the distribution of the conduction losses during the zero states, numerous carrier-

based PWM strategies have been proposed for the 3L-ANPC converter [7], [8], [16]. A comparison study between four well-known carrier-based PWM strategies for the 3L-ANPC converter regarding the junction temperature distribution inside the converter has been reported in [7] and is summarised in this paper.

This paper proposes a reconfigurable carrier-based PWM strategy for the 3L-ANPC converter. Compared to the other existing strategies, the proposed control algorithm guarantees an even loss and junction temperature balancing, and it permits to reduce the converter total losses.

To start with, a brief introduction of the structure and the operating principle: switching states and commutation types, of the 3L-ANPC converter is presented, along with an analysis of its thermal behaviour in section 2. Moreover, a comparison between the most popular existing control strategies regarding the heat distribution among the converter switches is summarised in section 3. Finally, in section 4, the authors introduce the proposed control strategy of the 3L-ANPC converter. Simulation tests are also presented in this section to prove the effectiveness of the proposed strategy over the existing ones.

2. 3L-ANPC CONVERTER: TOPOLOGY, OPERATING PRINCIPLE, AND THERMAL BEHAVIOUR

Fig 1 illustrates the schematic of a single leg of a 3L-NPC and a 3L-ANPC converter.

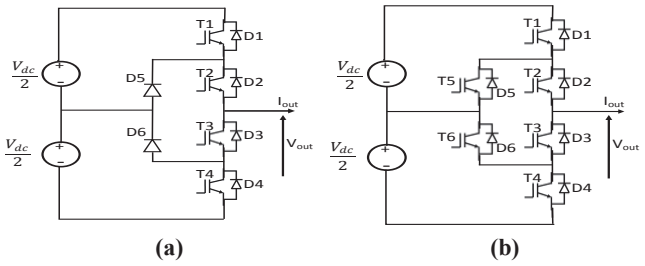

Fig. 1. One leg of a 3L-NPC converter (a) and a 3L-ANPC converter (b)

A. 3L-ANPC converter: topology and operating principle

The 3L-ANPC converter is derived from the NPC topology as shown if Fig 1. It consists of replacing the NPC clamp diodes by active switches providing more degrees of freedom and controllability. A single leg of the converter is made of 6 bidirectional switches, and each switch is composed of an IGBT (Ti) and its antiparallel diode (Di), where i=1..6. The switches are grouped in three commutation cells:

- cell1: (T1/D1) and (T5/D5)
- Cell2: (T2/D2) and (T3/D3)
- Cell3: (T4/D4) and (T6/D6)

Compared to the classical 3L-NPC structure, the 3L-ANPC converter features two extra configurations to clamp the neutral point. TABLE I shows the on state devices and the resulting output voltage during each switch state.

The resulting zero state configurations are designed: "z_1^u" and "z_2^u" if the neutral tap is clamped through the upper path of converter and "z_1^l" and "z_2^l" if the zero state is obtained through the lower path. The states "+" and " − " correspond to a direct connection of the converter output to the DC voltage supply.

TABLE I.
3L-ANPC CONVERTER SWITCHING STATES

CVS state	ON state device	Output voltage
" + "	T1, T2, T6	$+\frac{V_{dc}}{2}$
"z_1^u"	T2, T4, T5	0
"z_2^u"	T2, T5	0
"z_1^l"	T3, T6	0
"z_2^l"	T1, T3, T6	0
" − "	T3, T4, T5	$-\frac{V_{dc}}{2}$

TABLE II illustrates the most stressed converter devices during every commutation type.

TABLE II.
COMMUTATION TYPES AND MOST STRESSED DEVICES

Commutations	Phase current	Most stressed devices
"+" ↔ "z_2^u"	Positive	T1, D5
"+" ↔ "z_1^l"		T2, D3
"+" ↔ "z_2^l"		T1, D3
"z_1^u" ↔ "−"		T2, D3
"z_2^u" ↔ "−"		T2, D4
"z_1^l" ↔ "−"		D4, T6
"z_2^l" ↔ "−"		D4, T6
"+" ↔ "z_2^u"	Negative	D1, T5
"+" ↔ "z_1^l"		D2, T3
"+" ↔ "z_2^l"		D1, T3
"z_1^u" ↔ "−"		D2, T3
"z_2^u" ↔ "−"		D2, T4
"z_1^l" ↔ "−"		T4, D6
"z_2^l" ↔ "−"		T4, D6

The commutations from or to the zero states determine the switching losses distribution. According to TABLE II, all commutations occur between one active switch and one diode. Thereby even if more than two devices turn on or off, only one active switch and one diode experience significant switching losses. Moreover, the conduction losses distribution can be controlled by the selection of the upper or the lower path during the zero states, but they cannot be influenced in the positive "+" or the negative "−" state. As a result, the four zero states are the key influence factors of loss and junction temperature distribution inside the converter used in the PWM control strategies.

B. 3L-ANPC converter thermal behaviour

In power electronics application, the operating junction temperature T_j of a power device is a critical aspect which can be considered to increase the converter's efficiency and to reduce the costs. Indeed, the increase in the

operating junction temperature can permit to reduce the heat sink dimension or to increase the load current [17]. Thereby, a precise electro-thermal simulation technique is required to accurately estimate the junction temperatures and obviously the thermal behaviour inside the converter.

The instantaneous junction temperature in the junction j is calculated by (1). It depends on the device's power loss P_{tot}, the junction to case thermal impedance $Z_{thj\text{-}c}$, and the ambient temperature T_a.

$$T_j(t) = P_{tot}(t) \times Z_{thj-c}(t) + T_a(t) \quad (1)$$

Where:

$$Z_{thj-c}(t) = \sum_{i=1}^{4} R_{thi}\left(1 + e^{-\frac{t}{\tau_i}}\right) \quad (2)$$

Where R_{th} is the thermal resistance and $\tau = R_{th} \times C_{th}$ is the time constant, these parameters are provided in the manufacturer's datasheet.

The electro-thermal simulation technique used in this paper is the same one used in [7], as well as the method of the estimation of the power loss of each converter device. The calculated power losses are after that injected into an RC-based thermal model allowing the estimation of the junction temperature of every device. The thermal model elaboration and the T_j estimation technique are detailed in [7]. The estimated junction temperatures will serve later to describe the thermal behaviour of the 3L-ANPC converter depending on the employed control strategy.

3. 3L-ANPC PWM CONTROL STRATEGIES FOR JUNCTION TEMPERATURE BALANCING

Several PWM strategies have been proposed to control the 3L-ANPC converter. They are classified into two basic categories: the carrier–based strategy and the space vector modulation strategy [18]. This work concentrates on the carrier-based modulation technique.
In this section, the most known existing PWM strategies and their resulting thermal distribution are summarised.

A. Conventional PWM control strategies

Two well known PWM strategies called PWM_1 and PWM_2 were proposed for the 3L-ANPC converter control [7], [8], [14] ... These two strategies are based on the Phase Disposition PWM (PD-PWM) technique, i.e. they compare a sinusoidal reference voltage with two triangular carriers having the same frequency and same amplitude but vertically shifted.
In the case of the PWM_1, cell1 and cell3 are switching at high frequency; however cell2 switches at low frequency. The resulting switch states of this strategy are depicted in TABLE III. Fig 2 illustrates the junction temperature distribution by the PWM_1 among the IGBTs (T_j^{Ti}) and the diodes (T_j^{Di}), where $i = 1..6$, which are unequally distributed and the gap between the highest and the lowest temperature is about 24° C.

TABLE III.
SWITCHING STATES OF THE PWM_1

Output voltage	Switching states	On state devices
$-\frac{V_{dc}}{2}$	" − "	T3, T4
0	"z_2^l"	T1, T6
	"z_2^u"	T2, T5
$+\frac{V_{dc}}{2}$	" + "	T1, T2

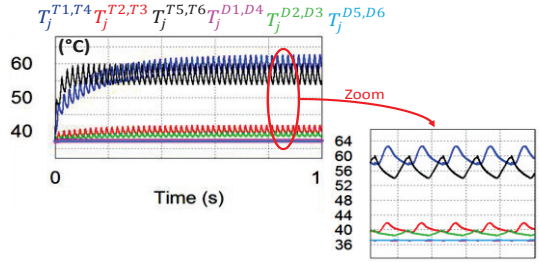

Fig. 2. Junction temperature distribution inside a 3L-ANPC converter by the PWM_1 (Vdc = 600V, f_s = 10kHz, RL load: R=1Ω, L=1mH, IGBT module: SKM50GB12T4)

In contrast to the PWM_1, for the PWM_2 cell2 switches at high frequency while the two others; cell1 and cell3 are switching at low frequency. The switching states and the involved devices are shown in TABLE IV.

TABLE IV.
SWITCHING STATES OF THE PWM_2

Output voltage	Switching states	On state devices
$-\frac{V_{dc}}{2}$	" − "	T3, T4, T5
0	"z_1^l"	T1, T3, T6
	"z_1^u"	T2, T4, T5
$+\frac{V_{dc}}{2}$	" + "	T1, T2, T6

As it can be observed in TABLE IV, the commutations taking place are "+" ↔ "z_1^l" and "z_1^u" ↔ "−". Thus the most stressed devices are inner ones: T2, T3, D2, and D3.

Fig 3 shows the junction temperature distribution by the PWM_2, which is also unequally distributed and the gap between the hottest and the coldest device is about 25 °C.

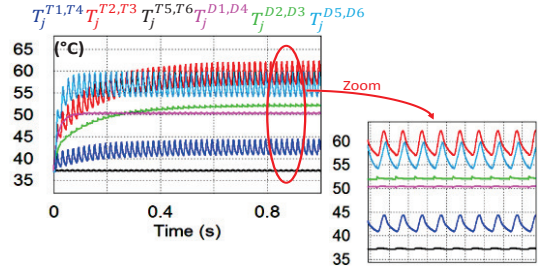

Fig. 3. Junction temperature distribution inside a 3L-ANPC converter by the PWM_2 (Vdc = 600V, f_s = 10kHz, RL load: R=1Ω, L=1mH, IGBT module: SKM50GB12T4)

According to the previous results depicted in Fig 2 and Fig 3, it's clearly observed that the PWM_1 and the PWM_2 do not take advantage of the additional degree of freedom of the ANPC topology. Thus the use of these strategies doesn't improve the thermal balancing among the 3L-

ANPC converter's devices, and the converter does not overcome the main drawback of the NPC topology.

B. Double frequency PWM strategy

This strategy named PWM_3 was proposed by Floricau in 2008 [14]. It's based on the Phase Opposition Disposition PWM (POD-PWM) technique. In fact, it compares a sinusoidal reference voltage with two triangular carriers with the same frequency and the same amplitude, but phase shifted on the horizontal axis with a half of the switching period. In comparison with the two previous strategies, this PWM strategy allows four different zero states in addition to the positive and negative switch states. The switching sequences are depicted in TABLE V.

TABLE V.
SWITCHING STATES OF THE PWM_3

Output voltage	Switching states	On state devices
$-\frac{V_{dc}}{2}$	" − "	T3, T4, T5
0	"z_1^l"	T3, T6
	"z_2^l"	T2, T4, T5
	"z_1^u"	T2, T5
	"z_2^u"	T1, T3, T6
$+\frac{V_{dc}}{2}$	" + "	T1, T2, T6

Additional commutation types from or to a zero state are possible in the case of the PWM_3 allowing better junction temperature distribution among the converter's power switches compared to PWM_1 and PWM_2. Fig 4 illustrates the junction temperature distribution by the PWM_3.

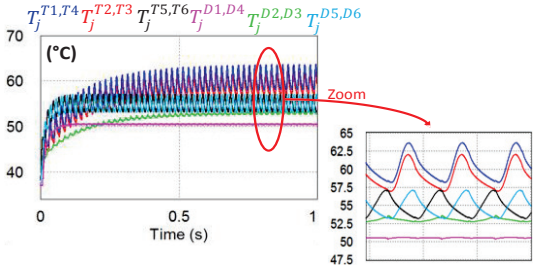

Fig. 4. Junction temperature distribution inside a 3L-ANPC converter by the PWM_3 (Vdc = 600V, f_s = 10kHz, RL load: R=1Ω, L=1mH, IGBT module: SKM50GB12T4)

The PWM_3 allows a better temperature distribution than either the PWM_1 or PWM_2 and the gap between the higher and the lower temperature is reduced to about 14°C. However, as shown in Fig 4, the two inverse diodes D1 and D4 still have lower junction temperatures than the other power devices.

C. PWM_4 strategy

The PWM_4 was proposed in 2013 by Zhang [8]. It allows four zero states: "z_1^l", "z_2^l", "z_1^u" and "z_2^u", and the states " − " and " + ". TABLE V resumes the switching states of this strategy, and Fig 5 shows how the junction temperatures of the converter's devices are distributed.

TABLE VI.
SWITCHING STATES OF THE PWM_4

Output voltage	Switching states	On state devices
$-\frac{V_{dc}}{2}$	" − "	T3, T4, T5
0	"z_1^l"	T1, T3, T6
	"z_2^l"	T3, T6
	"z_1^u"	T2, T4, T5
	"z_2^u"	T2, T5
$+\frac{V_{dc}}{2}$	" + "	T1, T2, T6

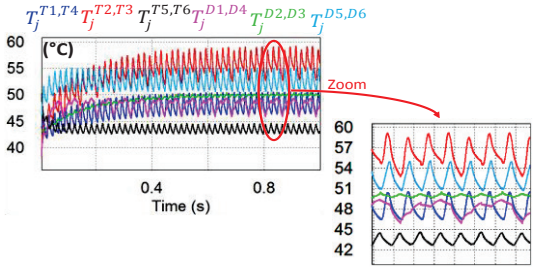

Fig. 5. Junction temperature distribution inside a 3L-ANPC converter by the PWM_4 (Vdc = 600V, f_s = 10kHz, RL load: R=1Ω, L=1mH, IGBT module: SKM50GB12T4)

The gap between the coldest and the hottest device in the case of the PWM_4 is about 14°C. This strategy guarantees hence a better temperature distribution than the conventional strategies, but it doesn't provide much better result than the PWM_3.

In this paper, a reconfigurable carrier-based PWM strategy is proposed to improve the thermal balancing among the considered converter's power devices.

4. PROPOSED PWM STRATEGY RECONFIGURATION

The proposed PWM strategy is a combination of the two conventional strategies: the PWM_1 and the PWM_2. The algorithm takes benefit from these two strategies advantages to balance the thermal distribution inside the 3L-ANPC converter. The flowchart of Fig 6 describes the digital control system of the proposed algorithm.

The proposed control technique is based on an active thermal balancing algorithm. In contrast to the control techniques previously mentioned, the proposed one generates the gate signals in function of the junction temperature distribution in order to release the overheated device. This algorithm consists of two main functional units: The on-line estimation of the power losses and the junction temperatures of all the converter devices (IGBTs and diodes) and the generation of the gate signals to the converter power switches. In this second unit, the gate signals are generated either by the PWM_1 or by the PWM_2 in function of the estimated junction temperature distribution.

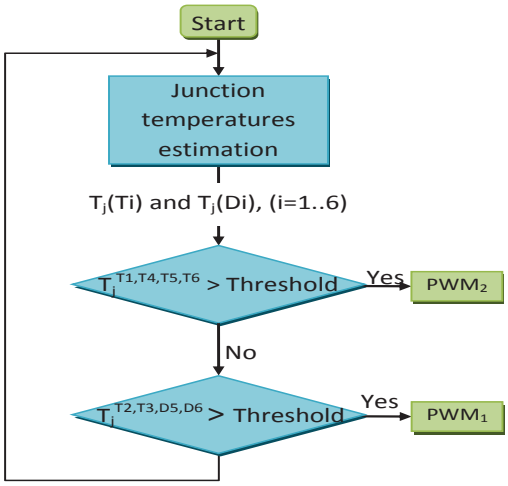

Fig. 6. Flowchart of the proposed PWM strategy

In a previous work, the two strategies PWM_1 and PWM_2 have been combined [19]. This combination consists of applying the switching sequences of the PWM_1 during 50% of the sinusoidal reference voltage period and during the rest 50% of the period the switching sequences of the PWM_2 are applied. The period of the application of the PWM_1 or the PWM_2 is arbitrary in this case, and the converter power losses and junction temperatures distribution are not considered. However, in the case of our proposed algorithm, the application of the switching sequences of the PWM_1 or PWM_2 depends on the junction temperature of the power devices. The principle of the proposed algorithm is explained below.

In the first functional unit, the power losses are firstly estimated. Then an RC Foster circuit-based thermal model of the 3L-ANPC is elaborated to estimate the junction temperatures of the six active switches $T_j(Ti)$ and their inverse diodes $T_j(Di)$, where $(i = 1..6)$. The thermal model's inputs are the total losses P_{tot} calculated by (3) of each power switch and the ambient temperature ($T_a = 25°C$).

$$P_{tot} = P_{sw} + P_{cond} \quad (3)$$

Where, P_{sw} and P_{cond} are respectively the switching losses and the conduction losses.

After that, in the second functional unit, and according to the junction temperature distribution inside the converter, the selection between the two strategies: PWM_1 or PWM_2 which will generate the converter switch control signals will be made. The proposed algorithm guarantees that the device with the highest junction temperature will be released and will not experience more switching losses.

As shown in Fig 2, the outer devices T1, T4, T5 and T6 are the most stressed devices in the case of the PWM_1 depending on the operating point. In the other case of the PWM_2, and as shown in Fig 3, T2, T3, D5 and D6 are the most stressed devices. Thus, the principle of the proposed algorithm is based on these two conclusions. In fact, it compares Tj(T1), Tj(T4), Tj(T5) and Tj(T6) to a threshold fixed to a 10% of the highest temperature. This threshold is chosen carefully since almost 60% of power electronics failures, are temperature induced [20], and this failure rate nearly doubles for every 10°C rise in operating temperature. Specifically, if one of these temperatures exceeds the threshold, the algorithm allows the PWM_2 to generate the gate signals to the converter. In the opposite case, if Tj(T2), Tj(T3), Tj(D5) or Tj(D6) exceeds the threshold, the algorithm switches to PWM_1 which will generate the control signals to the converter.

Fig 7 shows the waveforms of the converter output current and voltage in the case of the proposed PWM strategy.

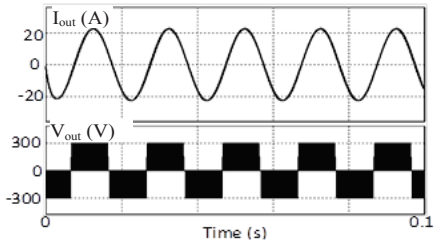

Fig. 7. Output current and voltage waveforms of 3L-ANPC converter with the proposed PWM, (Vdc = 600V, f_s = 10kHz, RL load: R=1Ω, L=1mH, IGBT module: SKM50GB12T4)

The junction temperatures redistribution using the proposed PWM strategy, are shown in Fig 8.

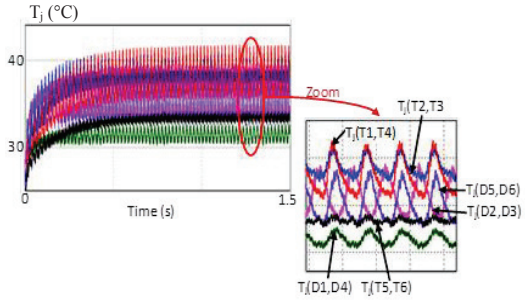

Fig. 8. Junction temperature distribution with the proposed PWM strategy (Vdc = 600V, f_s = 10kHz, RL load: R=1Ω, L=1mH, IGBT module: SKM50GB12T4)

According to Fig 8, the improved junction temperature balancing inside the 3L-ANPC converter can be clearly observed. In fact, the proposed control strategy can reduce the gap between the hottest and the coldest device less than 10 °C, which allows a better heat distribution among the converter's devices.

5. CONCLUSION

The power losses and thermal distribution among power converter devices are one of the critical issues to be considered in order to improve the performances, the service lifetime, the reliability and the cost of any conversion structure. This paper focuses on the junction temperature distribution in the 3L-ANPC topology according to the control strategies employed.

A reconfigurable PWM control strategy for a 3L-ANPC converter is proposed in this paper. This novel algorithm takes benefits from the conventional PWM strategies

named PWM_1 and PWM_2. The PWM_1 permits to release the inner switches of the converter while the PWM_2 releases the outer converter switches. According to the junction temperature distribution inside the converter, the proposed algorithm decides which PWM strategy will generate the gate signals to the power switches.

This method guarantees that the most stressed devices will not experience significant switching losses. Hence, the asymmetric loss and heat distribution will be evenly balanced, and the NPC major drawback is overcome. The effectiveness of this proposed algorithm is proved by PSIM simulation results.

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